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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ80
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/ez80f93az020sc

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Table 5. Clock Peripheral Power-Down Register 2; (CLK_PPD2 = 00DCh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Note: R/W = Read/Write; R = Read Only.								

Bit Position	Value	Description
7 PHI_OFF	1	PHI Clock output is disabled (output is high-impedance).
	0	PHI Clock output is enabled.
6	0	Reserved.
5 PRT5_OFF	1	System clock to PRT5 is powered down.
	0	System clock to PRT5 is powered up.
4 PRT4_OFF	1	System clock to PRT4 is powered down.
	0	System clock to PRT4 is powered up.
3 PRT3_OFF	1	System clock to PRT3 is powered down.
	0	System clock to PRT3 is powered up.
2 PRT2_OFF	1	System clock to PRT2 is powered down.
	0	System clock to PRT2 is powered up.
1 PRT1_OFF	1	System clock to PRT1 is powered down.
	0	System clock to PRT1 is powered up.
0 PRT0_OFF	1	System clock to PRT0 is powered down.
	0	System clock to PRT0 is powered up.

Signal timing for Motorola bus mode is displayed for a Read operation in Figure 17 and for a Write operation in Figure 18 on page 66. In these two figures, each Motorola bus mode state is 2 CPU system clock cycles in duration.

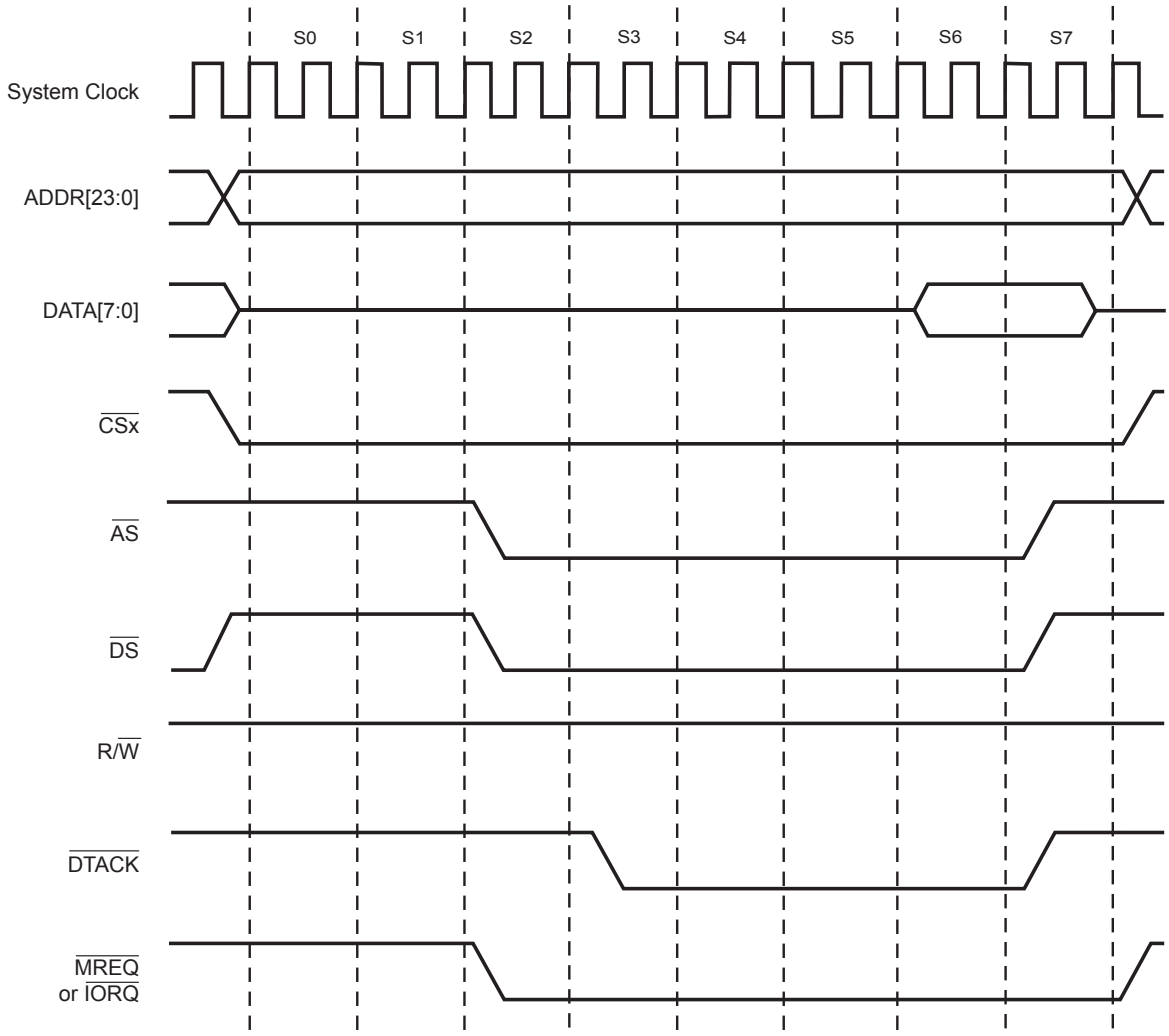

Figure 17. Example: Motorola Bus Mode Read Timing

If the NMI_OUT bit in the WDT_CTL register is set to 1, then upon time-out, the WDT asserts an NMI for CPU processing. The NMI_FLAG bit can be polled by the CPU to determine the source of the NMI event.

Watchdog Timer Registers

Watchdog Timer Control Register

The Watchdog Timer Control register, listed in Table 27, is an 8-bit Read/Write register used to enable the Watchdog Timer, set the time-out period, indicate the source of the most recent RESET, and select the required operation upon WDT time-out.

Table 27. Watchdog Timer Control Register; (WDT_CTL = 0093h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0/1	0	0	0	0	0
CPU Access	R/W	R/W	R	R/W	R/W	R	R/W	R/W
Note: R = Read only; R/W = Read/Write.								

Bit Position	Value	Description
7 WDT_EN	0	WDT is disabled.
	1	WDT is enabled. When enabled, the WDT cannot be disabled without a RESET.
6 NMI_OUT	0	WDT time-out resets the CPU.
	1	WDT time-out generates a nonmaskable interrupt (NMI) to the CPU.
5 RST_FLAG*	0	RESET caused by external full-chip reset or ZDI reset.
	1	RESET caused by WDT time-out. This flag is set by the WDT time-out, even if the NMI_OUT flag is set to 1. The CPU can poll this bit to determine the source of the RESET or NMI.
[4:3] WDT_CLK	00	WDT clock source is system clock.
	01	WDT clock source is Real-Time Clock source (32 kHz on-chip oscillator or 50/60 Hz input as set by RTC_CTRL[4]).
	10	Reserved.
	11	Reserved.
2	0	Reserved.

Note: *RST_FLAG is only cleared by a non-WDT RESET.

Bit Position	Value	Description
[1:0] WDT_PERIOD	00	WDT time-out period is 2^{27} clock cycles.
	01	WDT time-out period is 2^{25} clock cycles.
	10	WDT time-out period is 2^{22} clock cycles.
	11	WDT time-out period is 2^{18} clock cycles.

Note: *RST_FLAG is only cleared by a non-WDT RESET.

Watchdog Timer Reset Register

The Watchdog Timer Reset register, listed in Table 28, is an 8-bit Write Only register. The Watchdog Timer is reset when an A5h value followed by 5Ah is written to this register. Any amount of time can occur between the writing of the A5h value and the 5Ah value, so long as the WDT time-out does not occur prior to completion.

Table 28. Watchdog Timer Reset Register; (WDT_RR = 0094h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	W	W	W	W	W	W	W	W
Note: X = Undefined; W = Write only.								

Bit Position	Value	Description
[7:0] WDT_RR	A5h	The first Write value required to reset the WDT prior to a time-out.
	5Ah	The second Write value required to reset the WDT prior to a time-out. If an A5h, 5Ah sequence is written to WDT_RR, the WDT timer is reset to its initial count value, and counting resumes.

Table 34. Timer Data Register—High Byte(TMR0_DR_H = 0082h, TMR1_DR_H = 0085h, TMR2_DR_H = 0088h, TMR3_DR_H = 008Bh, TMR4_DR_H = 008Eh, or TMR5_DR_H = 0091h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R	R	R	R	R	R	R	R
Note: R = Read only.								

Bit Position	Value	Description
[7:0] TMRx_DR_H	00h–FFh	These bits represent the High byte of the 2-byte timer data value, {TMRx_DR_H[7:0], TMRx_DR_L[7:0]}. Bit 7 is bit 15 (msb) of the 16-bit timer data value. Bit 0 is bit 8 of the 16-bit timer data value.

Timer Reload Register—Low Byte

The Timer Reload Register—Low Byte, listed in Table 35, stores the least-significant byte (LSB) of the 2-byte timer reload value. In CONTINUOUS mode, the timer reload value is reloaded into the timer upon end-of-count. When RST_EN (TMRx_CTL[1]) is set to 1 to enable the automatic reload and restart function, the timer reload value is written to the timer on the next rising edge of the clock.

Note: *The Timer Data registers and Timer Reload registers share the same address space.*

Table 35. Timer Reload Register—Low Byte(TMR0_RR_L = 0081h, TMR1_RR_L = 0084h, TMR2_RR_L = 0087h, TMR3_RR_L = 008Ah, TMR4_RR_L = 008Dh, or TMR5_RR_L = 0090h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	W	W	W	W	W	W	W	W
Note: W = Write only.								

Bit Position	Value	Description
[7:0] TMRx_RR_L	00h–FFh	These bits represent the Low byte of the 2-byte timer reload value, {TMRx_RR_H[7:0], TMRx_RR_L[7:0]}. Bit 7 is bit 7 of the 16-bit timer reload value. Bit 0 is bit 0 (lsb) of the 16-bit timer reload value.

- Write values to the RTC alarm registers to set the appropriate alarm conditions
- Write to RTC_CTRL to clear the RTC_UNLOCK bit; clearing the RTC_UNLOCK bit resets and enables the clock divider

Real-Time Clock Registers

The Real-Time Clock registers are accessed via the address and data bus using I/O instructions. RTC_UNLOCK controls access to the RTC count registers. When unlocked (RTC_UNLOCK = 1), the RTC count is disabled and the count registers are Read/Write. When locked (RTC_UNLOCK = 0), the RTC count is enabled and the count registers are Read Only. The default, at RESET, is for the RTC to be locked.

Real-Time Clock Seconds Register

This register contains the current seconds count. The value in the RTC_SEC register is unchanged by a RESET. The current setting of BCD_EN determines whether the values in this register are binary (BCD_EN = 0) or binary-coded decimal (BCD_EN = 1). Access to this register is Read Only if the RTC is locked and Read/Write if the RTC is unlocked. See Table 38.

Table 38. Real-Time Clock Seconds Register; (RTC_SEC = 00E0h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Note: X = Unchanged by RESET; R/W* = Read Only if RTC locked, Read/Write if RTC unlocked.								

Binary-Coded-Decimal Operation (BCD_EN = 1)		
Bit Position	**Value**	**Description**
[7:4] TEN_SEC	0–5	The tens digit of the current seconds count.
[3:0] SEC	0–9	The ones digit of the current seconds count.

Binary Operation (BCD_EN = 0)		
Bit Position	**Value**	**Description**
[7:0] SEC	00h–3Bh	The current seconds count.

Real-Time Clock Alarm Minutes Register

This register contains the alarm minutes value. See Table 47.

Table 47. Real-Time Clock Alarm Minutes Register; (RTC_AMIN = 00E9h)

Bit	7	6	5	4	3	2	1	0
Reset	X	X	X	X	X	X	X	X
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Note: X = Unchanged by RESET; R/W = Read/Write.								

Binary-Coded-Decimal Operation (BCD_EN = 1)

Bit Position	Value	Description
[7:4] ATEN_MIN	0–5	The tens digit of the alarm minutes value.
[3:0] AMIN	0–9	The ones digit of the alarm minutes value.

Binary Operation (BCD_EN = 0)

Bit Position	Value	Description
[7:0] AMIN	00h–3Bh	The alarm minutes value.

Table 58. UART Interrupt Status Codes (Continued)

INSTS Value	Priority	Interrupt Type
001	Fifth	Transmit Buffer Empty
000	Lowest	Modem Status

UART FIFO Control Register

This register is used to monitor trigger levels, clear FIFO pointers, and enable or disable the FIFO. The UARTx_FCTL registers share the same I/O addresses as the UARTx_IIR registers. See Table 59.

Table 59. UART FIFO Control Registers(UART0_FCTL = 00C2h, UART1_FCTL = 00D2h)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	W	W	W	W	W	W	W	W
Note: W = Write only.								

Bit Position	Value	Description
[7:6] TRIG	00	Receive FIFO trigger level set to 1. Receive data interrupt is generated when there is 1 byte in the FIFO. Valid only if FIFO is enabled.
	01	Receive FIFO trigger level set to 4. Receive data interrupt is generated when there are 4 bytes in the FIFO. Valid only if FIFO is enabled.
	10	Receive FIFO trigger level set to 8. Receive data interrupt is generated when there are 8 bytes in the FIFO. Valid only if FIFO is enabled.
	11	Receive FIFO trigger level set to 14. Receive data interrupt is generated when there are 14 bytes in the FIFO. Valid only if FIFO is enabled.
[5:3]	000	Reserved.
2 CLRTXF	0	No effect.
	1	Clear the transmit FIFO and reset the transmit FIFO pointer. Valid only if the FIFO is enabled.

I2C Serial I/O Interface

I²C General Characteristics

The I²C serial I/O bus is a two-wire communication interface that can operate in four modes:

1. MASTER TRANSMIT
2. MASTER RECEIVE
3. SLAVE TRANSMIT
4. SLAVE RECEIVE

The I²C interface consists of the Serial Clock (SCL) and the Serial Data (SDA). Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via an external pull-up resistor. When the bus is free, both lines are High. The output stages of devices connected to the bus must be configured as open-drain outputs. Data on the I²C bus can be transferred at a rate of up to 100 kbps in STANDARD mode, or up to 400 kbps in FAST mode. One clock pulse is generated for each data bit transferred.

Clocking Overview

If another device on the I²C bus drives the clock line when the I²C is in MASTER mode, the I²C synchronizes its clock to the I²C bus clock. The High period of the clock is determined by the device that generates the shortest High clock period. The Low period of the clock is determined by the device that generates the longest Low clock period.

A slave may stretch the Low period of the clock to slow down the bus master. The Low period may also be stretched for handshaking purposes. This can be done after each bit transfer or each byte transfer. The I²C stretches the clock after each byte transfer until the IFLG bit in the I2C_CTL register is cleared.

Bus Arbitration Overview

In MASTER mode, the I²C checks that each transmitted logic 1 appears on the I²C bus as a logic 1. If another device on the bus overrules and pulls the SDA signal Low, arbitration is lost. If arbitration is lost during the transmission of a data byte or a Not-Acknowledge bit, the I²C returns to the idle state. If arbitration is lost during the transmission of an address, the I²C switches to SLAVE mode so that it can recognize its own slave address or the general call address.

Table 81. I²C Master Receive Status Codes (Continued)

Code	I²C State	Microcontroller Response	Next I²C Action
48h	Addr + R transmitted, ACK not received	For a 7-bit address: Set STA, clear IFLG	Transmit repeated START
		Or set STP, clear IFLG	Transmit STOP
		Or set STA & STP, clear IFLG	Transmit STOP then START
		For a 10-bit address: Write extended address byte to DATA, clear IFLG	Transmit extended address byte
38h	Arbitration lost	Clear IFLG	Return to idle
		Or set STA, clear IFLG	Transmit START when bus is free
68h	Arbitration lost, SLA+W received, ACK transmitted	Clear IFLG, clear AAK = 0	Receive data byte, transmit NACK
		Or clear IFLG, set AAK = 1	Receive data byte, transmit ACK
78h	Arbitration lost, General call addr received, ACK transmitted	Same as code 68h	Same as code 68h
B0h	Arbitration lost, SLA+R received, ACK transmitted	Write byte to DATA, clear IFLG, clear AAK = 0	Transmit last byte, receive ACK
		Or write byte to DATA, clear IFLG, set AAK = 1	Transmit data byte, receive ACK

R = Read bit; that is, the lsb is set to 1.

If 10-bit addressing is being used, the slave is first addressed using the full 10-bit address plus the Write bit. The master then issues a restart followed by the first part of the 10-bit address again, but with the Read bit. The status code then becomes `40h` or `48h`. It is the responsibility of the slave to remember that it had been selected prior to the restart.

If a repeated START condition is received, the status code is `10h` instead of `08h`.

After each data byte is received, the IFLG is set and one of the status codes listed in Table 82 is in the I2C_SR register.

Table 87. I²C Control Registers(I2C_CTL = 00CBh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Note: R/W = Read/Write; R = Read Only.								

Bit Position	Value	Description
7 IEN	0	I^2C interrupt is disabled.
	1	I^2C interrupt is enabled.
6 ENAB	0	The I^2C bus (SCL/SDA) is disabled and all inputs are ignored.
	1	The I^2C bus (SCL/SDA) is enabled.
5 STA	0	Master mode START condition is sent.
	1	Master mode start-transmit START condition on the bus.
4 STP	0	Master mode STOP condition is sent.
	1	Master mode stop-transmit STOP condition on the bus.
3 IFLG	0	I^2C interrupt flag is not set.
	1	I^2C interrupt flag is set.
2 AAK	0	Not Acknowledge.
	1	Acknowledge.
[1:0]	00	Reserved.

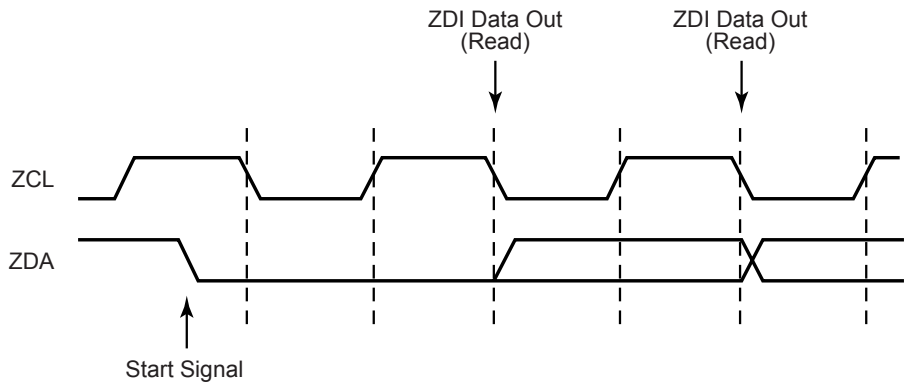

Figure 40.ZDI Read Timing

ZDI Single-Bit Byte Separator

Following each 8-bit ZDI data transfer, a single-bit byte separator is used. To initiate a new ZDI command, the single-bit byte separator must be High (logical 1) to allow for a new ZDI START command to be sent. For all other cases, the single-bit byte separator can be either Low (logical 0) or High (logical 1). When ZDI is configured to allow the CPU to accept external bus requests, the single-bit byte separator should be Low (logical 0) during all ZDI commands. This Low value indicates that ZDI is still operating and is not ready to relinquish the Bus. The CPU does not accept the external bus requests until the single-bit byte separator is a High (logical 1). For more information about accepting bus requests in ZDI DEBUG mode, see the Bus Requests During ZDI DEBUG Mode section on page 169.

ZDI Register Addressing

Following a START signal the ZDI master must output the ZDI register address. All data transfers with the ZDI block use special ZDI registers. The ZDI control registers that reside in the ZDI register address space should not be confused with the eZ80F92 device peripheral registers that reside in the I/O address space.

Many locations in the ZDI control register address space are shared by two registers, one for Read Only access and one for Write Only access. As an example, a Read from ZDI register address 00h returns the eZ80® Product ID Low Byte while a Write to this same location, 00h, stores the Low byte of one of the address match values used for generating BREAK points.

The format for a ZDI address is seven bits of address, followed by one bit for Read or Write control, and completed by a single-bit byte separator. The ZDI executes a Read or Write operation depending on the state of the R/$\overline{W}$ bit (0 = Write, 1 = Read). If no new START command is issued at completion of the Read or Write operation, the operation

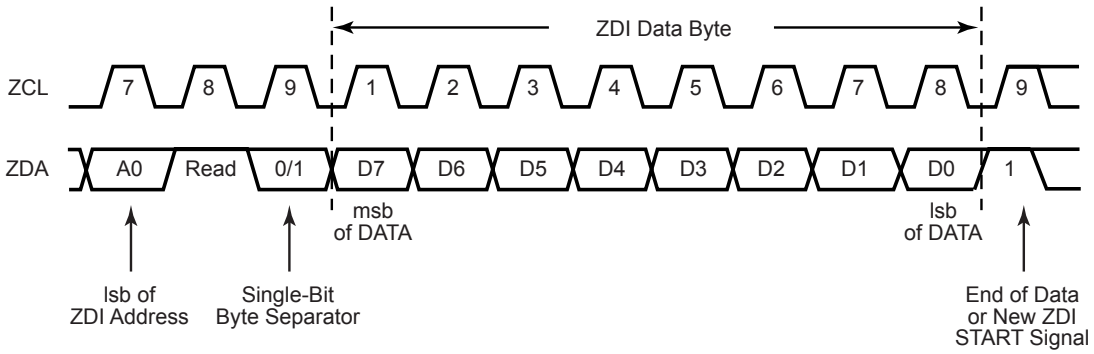

Figure 44.ZDI Single-Byte Data Read Timing

ZDI Block Read

A Block Read operation is initiated the same as a single-byte Read; however, the ZDI master continues to clock in the next byte from the ZDI slave as the ZDI slave continues to output data. The ZDI register address counter increments with each Read. If the ZDI register address reaches the end of the Read Only ZDI register address space (20h), the address stops incrementing. Figure 45 displays the ZDI's Block Read timing.

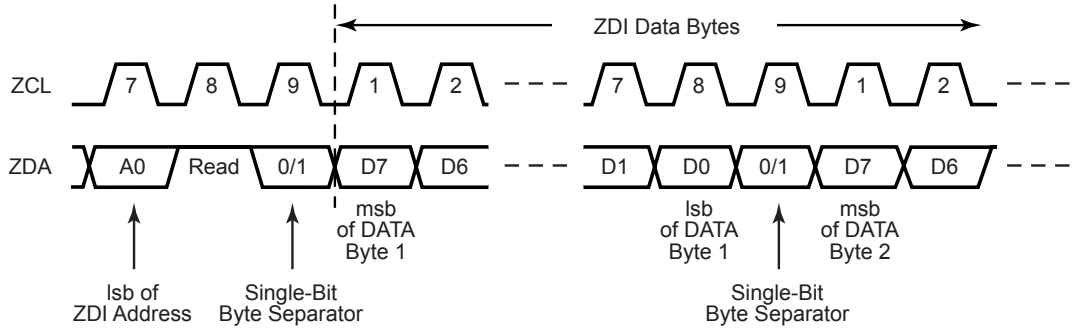

Figure 45.ZDI Block Data Read Timing

Operation of the eZ80F92 Device During ZDI Breakpoints

If the ZDI forces the CPU to BREAK, only the CPU suspends operation. The system clock continues to operate and drive other peripherals. Those peripherals that can operate autonomously from the CPU may continue to operate, if so enabled. For example, the Watchdog Timer and Programmable Reload Timers continue to count during a ZDI BREAK point.

When using the ZDI interface, any Write or Read operations of peripheral registers in the I/O address space produces the same effect as Read or Write operations using the CPU.

Table 96. ZDI BREAK Control Register(ZDI_BRK_CTL = 10h in the ZDI Write Only Register Address Space)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	W	W	W	W	W	W	W	W
Note: W = Write Only.								

Bit Position	Value	Description
7 brk_next	0	The ZDI BREAK on the next CPU instruction is disabled. Clearing this bit releases the CPU from its current BREAK condition.
	1	The ZDI BREAK on the next CPU instruction is enabled. The CPU can use multibyte Op Codes and multibyte operands. BREAK points only occur on the first Op Code in a multibyte Op Code instruction. If the ZCL pin is High and the ZDA pin is Low at the end of RESET, this bit is set to 1 and a BREAK occurs on the first instruction following the RESET. This bit is set automatically during ZDI BREAK on address match. A BREAK can also be forced by writing a 1 to this bit.
6 brk_addr3	0	The ZDI BREAK, upon matching BREAK address 3, is disabled.
	1	The ZDI BREAK, upon matching BREAK address 3, is enabled.
5 brk_addr2	0	The ZDI BREAK, upon matching BREAK address 2, is disabled.
	1	The ZDI BREAK, upon matching BREAK address 2, is enabled.
4 brk_addr1	0	The ZDI BREAK, upon matching BREAK address 1, is disabled.
	1	The ZDI BREAK, upon matching BREAK address 1, is enabled.
3 brk_addr0	0	The ZDI BREAK, upon matching BREAK address 0, is disabled.
	1	The ZDI BREAK, upon matching BREAK address 0, is enabled.

On-Chip Instrumentation

Introduction to On-Chip Instrumentation

On-Chip Instrumentation[1] (OCI™) for the eZ80® CPU core enables powerful debugging features. The OCI provides run control, memory and register visibility, complex break-points, and trace history features.

The OCI employs all of the functions of the ZDI as described in the Zilog Debug Interface section that starts on page 162. It also adds the following debug features:

- Control via a 4-pin Joint Test Action Group (JTAG)-standard port that conforms to the IEEE Standard 1149.1 (Test Access Port and Boundary Scan Architecture)[2]
- Complex break point trigger functions
- Break point enhancements, such as the ability to:
  - Define two break point addresses that form a range
  - Break on masked data values
  - Start or stop trace
  - Assert a trigger output signal
- Trace history buffer
- Software break point instruction

There are four sections to the OCI:

1. JTAG interface
2. ZDI debug control
3. Trace buffer memory
4. Complex triggers

OCI Activation

OCI features clock initialization circuitry so that external debug hardware can be detected during power-up. The external debugger must drive the OCI clock pin (TCK) Low at least two system clock cycles prior to the end of the RESET to activate the OCI block. If TCK is High at the end of the RESET, the OCI block shuts down so that it does not draw power in normal product operation. When the OCI is shut down, ZDI is enabled directly and can

1. On-Chip Instrumentation and OCI are trademarks of First Silicon Solutions, Inc.
2. The eZ80F92 does not contain the boundary scan register required for 1149.1 compliance.

be accessed via the clock (TCK) and data (TDI) pins. See the Zilog Debug Interface section on page 162 for more information about ZDI.

OCI Interface

There are five dedicated pins on the eZ80F92 device for the OCI interface. Four pins—TCK, TMS, TDI, and TDO—are required for IEEE Standard 1149.1-compliant JTAG ports. The TRIGOUT pin provides additional testability features. These five OCI pins are listed in Table 110.

Table 110. OCI Pins

Symbol	Name	Type	Description
TCK	Clock	Input	Asynchronous to the primary CPU system clock. The TCK period must be at least twice the system clock period. During RESET, this pin is sampled to select either OCI or ZDI DEBUG modes. If Low during RESET, the OCI is enabled. If High during RESET, the OCI is powered down and ZDI DEBUG mode is enabled. When ZDI DEBUG mode is active, this pin is the ZDI clock. On-chip pull-up ensures a default value of 1 (High).
TMS	Test Mode Select	Input	This serial test mode input controls JTAG mode selection. On-chip pull-up ensures a default value of 1 (High). The TMS signal is sampled on the rising edge of the TCK signal.
TDI	Data In	Input (OCI enabled)	Serial test data input. On-chip pull-up ensures a default value of 1 (High). This pin is input-only when the OCI is enabled. The input data is sampled on the rising edge of the TCK signal.
		I/O (OCI disabled)	When the OCI is disabled, this pin functions as the ZDA (ZDI Data) I/O pin.
TDO	Data Out	Output	The output data changes on the falling edge of the TCK signal.
TRIGOUT	Trigger Output	Output	Generates an active High trigger pulse when valid OCI trigger events occur. Output is tristate when no data is driven out.

Table 120. Flash Interrupt Control Register; (FLASH_IRQ=00FBh)

Bit	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0
CPU Access	R/W	R/W	R	R	R	R	R	R
Note: R/W = Read/Write, R = Read Only. Read resets bits [5] and [3:0].								

Bit Position	Value	Description
[7] DONE_IEN	0	Flash Erase/Row Program Done Interrupt is disabled
	1	Flash Erase/Row Program Done Interrupt is enabled
[6] ERR_IEN	0	Error Condition Interrupt is disabled
	1	Error Condition Interrupt is enabled
[5] DONE	0	Erase/Row Program Done Flag is not set
	1	Erase/Row Program Done Flag is set
[4]	0	Reserved
[3] WR_VIO	0	The Write Violation Error Flag is not set
	1	The Write Violation Error Flag is set
[2] RP_TMO	0	The Row Program Time-out Error Flag is not set
	1	The Row Program Time-out Error Flag is set
[1] PG_VIO	0	The Page Erase Violation Error Flag is not set
	1	The Page Erase Violation Error Flag is set
[0] MASS_VIO	0	The Mass Erase Violation Error Flag is not set
	1	The Mass Erase Violation Error Flag is set

Flash Page Select Register

The msb of this register is used to select whether all Flash access and Page Erases are directed to the 256-byte Information Page or to the main Flash memory array. When the main array is selected, the lower 7-bits (6 bits in the eZ80F93 device) are used to select one of the 128 pages for Page Erase or I/O Write operations.

To perform a Page Erase, the software must set the proper page value prior to setting the Page Erase bit in the Flash control register.

Table 151. External I/O Write Timing (Continued)

		Delay (ns)	
Parameter	**Abbreviation**	**Min**	**Max**
T_{10}	Clock Rise to $\overline{WR}$ Deassertion Delay*	1.6	6.5
	$\overline{WR}$ Deassertion to ADDR Hold Time	0.25	—
	$\overline{WR}$ Deassertion to DATA Hold Time	0.25	—
	$\overline{WR}$ Deassertion to $\overline{CSx}$ Hold Time	0.25	—
	$\overline{WR}$ Deassertion to $\overline{IORQ}$ Hold Time	0.25	—

Note: *At the conclusion of a Write cycle, deassertion of $\overline{WR}$ always occurs before any change to ADDR, DATA, $\overline{CSx}$, or $\overline{IORQ}$.

Wait State Timing for Read Operations

Figure 62 displays the extension of the memory access signals using a single WAIT state for a Read operation. This WAIT state is generated by setting CS_WAIT to 001h in the Chip Select Control Register.

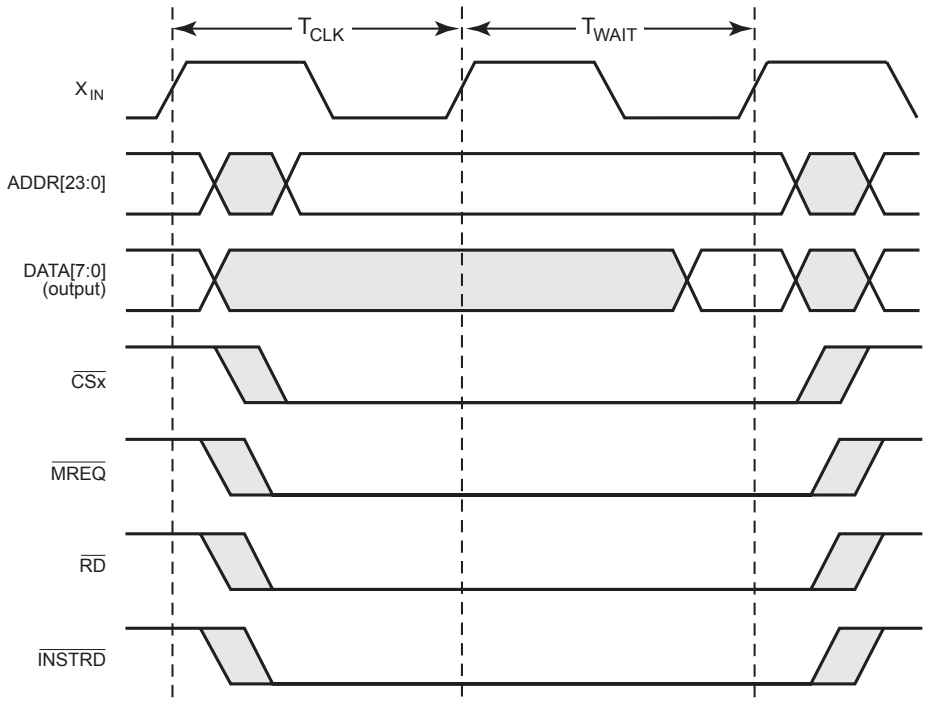

Figure 62.Wait State Timing for Read Operations

R

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