Lattice Semiconductor Corporation - ORT42G5-1BM484I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	204
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort42g5-1bm484i

Embedded Function Features

- High-speed SERDES with programmable serial data rates over the range 0.6 to 3.7 Gbps. Operation has been demonstrated on design tolerance devices at 3.7 Gbps across 26 in. of FR-4 backplane and at 3.125 Gbps across 40 in. of FR-4 backplane across temperature and voltage specifications.
- Asynchronous operation per receive channel with the receiver frequency tolerance based on one reference clock per block channels (separate PLL per channel).
- Ability to select full-rate or half-rate operation per transmit or receive channel by setting the appropriate control registers.
- Programmable one-half amplitude transmit mode for reduced power in chip-to-chip application.
- Transmit preemphasis (programmable) for improved receive data eye opening.
- 32-bit (8b/10b) or 40-bit (raw data) parallel internal bus for data processing in FPGA logic.
- Provides a 10 Gbps backplane interface to switch fabric. Also supports multiple port cards at 2.5 Gbps.
- 3.125 Gbps SERDES compliant with XAUI serial data specification for 10 G Ethernet applications with protection.
- IEEE 802.3ae compliant XAUI transceiver. Includes embedded IEEE 802.3ae-based XAUI link state machine.
- Compliant to FC-0 specification for 1 Gbps, 2Gbps, 10 Gbps (FC-XAUI) modes. Includes Fibre Channel link state machine.
- High-Speed Interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
- SERDES has low-power CML buffers. Support for 1.5V/1.8V I/Os. Allows use with optical transceiver, coaxial copper media, shielded twisted pair wiring or high-speed backplanes such as FR-4.
- Power down option of SERDES HSI receiver or transmitter on a per-channel basis.
- Automatic lock to reference clock in the absence of valid receive data.
- High-speed and low-speed loopback test modes.
- Requires no external component for clock recovery and frequency synthesis.
- SERDES characterization pins available to control/monitor the internal interface to one SERDES block (ORT82G5 only).
- SERDES HSI automatically recovers from loss-of-clock once its reference clock returns to normal operating state.
- Built-in boundary scan (IEEE ® 1149.1 and 1149.2 JTAG) for the programmable I/Os, not including the SERDES interface.
- FIFOs can align incoming data either across all eight channels (ORT82G5 only), across one or two groups of four channels, or across two or four groups of two channels. Alignment is done either using comma characters or by using the /A/ character in XAUI mode. Optionally, the alignment FIFOs can be bypassed for asynchronous operation between channels. (Each channel includes its own clock and frame pulse or comma detect.)
- Addition of two 4K x 36 dual-port RAMs with access to the programmable logic.
- The ORT82G5 is pinout compatible to the ORCA ORSO82G5 SONET backplane driver FPSC. The ORT42G5 is pin compatible to the ORSO42G5.

Additional Information

Contact your local Lattice representative for additional information regarding the ORCA Series 4 FPGA devices, or visit the Lattice web site at www.latticesemi.com.

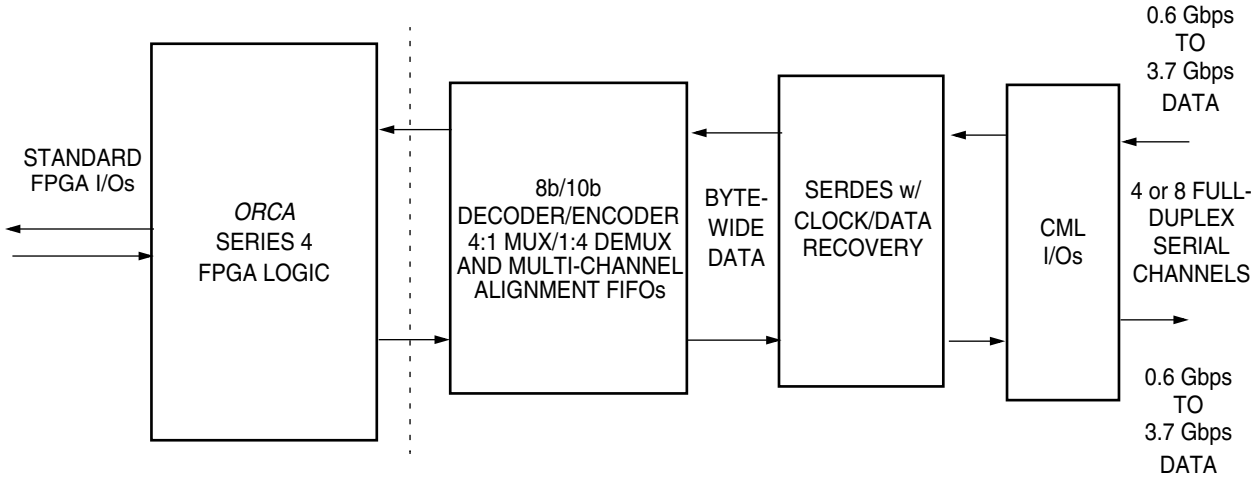
ORT42G5/ORT82G5 Overview

The ORT42G5 and ORT82G5 FPSCs provide high-speed backplane transceivers combined with FPGA logic. They are based on the 1.5V OR4E04 ORCA FPGA and have 36 x 36 arrays of Programmable Logic Cells (PLCs). The embedded core, which contains the backplane transceivers is attached to the right side of the device and is integrated directly into the FPGA array. A top level diagram of the basic chip configuration is shown in Figure 1.

Embedded Core Overview

The embedded core portions of the ORT42G5 and ORT82G5 contain respectively four or eight Clock and Data Recovery (CDR) macrocells and Serialize/Deserialize (SERDES) blocks and support 8b/10b (*IEEE* 802.3.2002) encoded serial links. It is intended for high-speed serial backplane data transmission. Figure 1 shows the ORT42G5 and ORT82G5 top level block diagram and the basic data flow. Boundary scan for the ORT42G5/ORT82G5 only includes programmable I/Os and does not include any of the embedded block I/Os.

Figure 1. ORT42G5/ORT82G5 Top Level Block Diagram



The serial channels can each operate at up to 3.7 Gbps (2.96 Gbps data rate) with a full-duplex synchronous interface with built-in clock recovery (CDR). The 8b/10b encoding provides guaranteed ones density for the CDR, byte alignment, and error detection. The core is also capable of frame synchronization and physical link monitoring and contains independent 4k x 36 RAM blocks. Overviews of the various blocks in the embedded core are presented in the following paragraphs.

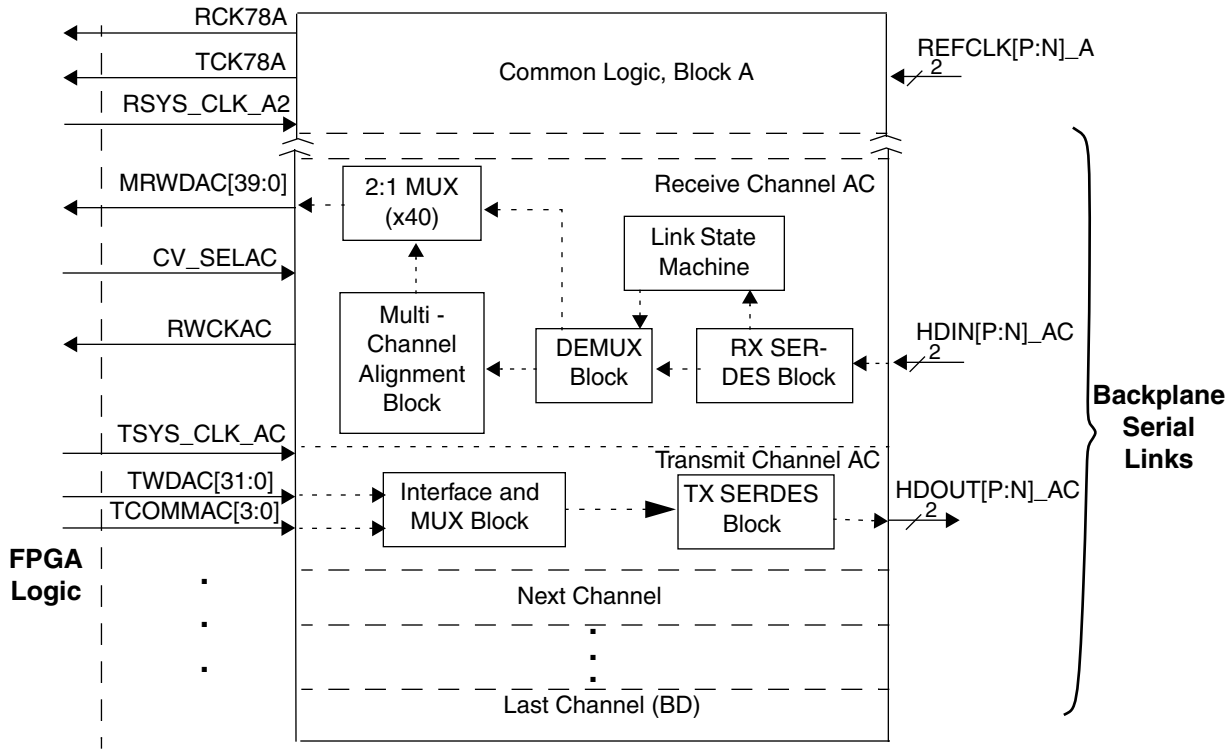
Serializer and Deserializer (SERDES)

The SERDES portion of the core contains two transceiver blocks for serial data transmission at a selectable data rate of 0.6 to 3.7 Gbps. Each SERDES channel features high-speed 8b/10b parallel I/O interfaces to other core blocks and high-speed CML interfaces to the serial links.

The SERDES circuitry consists of receiver, transmitter, and auxiliary functional blocks. The receiver accepts high-speed (up to 3.7 Gbps) serial data. Based on data transitions, the receiver locks an analog receive PLL for each channel to retime the data, then demultiplexes the data down to parallel bytes and an accompanying clock.

The transmitter operates in the reverse direction. Parallel bytes are multiplexed up to 3.7 Gbps serial data for off-chip communication. The transmitter generates the necessary 3.7 GHz clocks for operation from a lower speed reference clock.

Figure 2. Top Level Block Diagram, Embedded Core Logic (Channel AC)



The Embedded Core provides transceiver functionality for four or eight serial data channels and is organized into two blocks, each supporting two or four channels. Each channel is identified by both a block identifier [A:B] and a channel identifier [A:D]. In the ORT42G5 only the channel identifiers C and D are used. (This naming convention follows that of the ORT82G5).

The data channels can operate independently or they can be combined together (aligned) to achieve higher bit rates. The mode operation of the core is defined by a set of control registers, which can be written through the system bus interface. Also, the status of the core is stored in a set of status registers, which can be read through the system bus interface.

The transmitter section for each channel accepts 40 bits of data or 32 bits of data and eight control/status bits from the FPGA logic and optionally encodes the data using 8b/10b encoding. It also accepts the low-speed reference clock at the REFCLK input and uses this clock to synthesize the internal high-speed serial bit clock. The data is then serialized and the serialized data are available at the differential CML output terminated in 86 Ω to drive either an optical transmitter or coaxial media or circuit board/backplane.

The receiver section receives high-speed serial data at its differential CML input port. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. The retimed data are also deserialized and optionally 8b/10b decoded. The receiver also optionally recognizes the comma characters or code violations and aligns the bit stream to the proper word boundary. The resulting parallel data is optionally passed to the multi-channel alignment block before it is presented to the FPGA logic.

8b/10b Encoding and Decoding

In 8b/10b mode, the FPGA logic will receive/transmit 32 bits of data and 4 K_CTRL bits from/to the embedded core. In the transmit direction, four additional input bits force a negative disparity present state. The embedded core logic will encode the data to or decode the data from a 10-bit format according to the FC-PH ANSI X3.230:1994 standard (which is also the encoding used by the IEEE 802.3ae Ethernet standard). This encoding/decoding scheme also allows for the transmission of special characters and supports error detection.

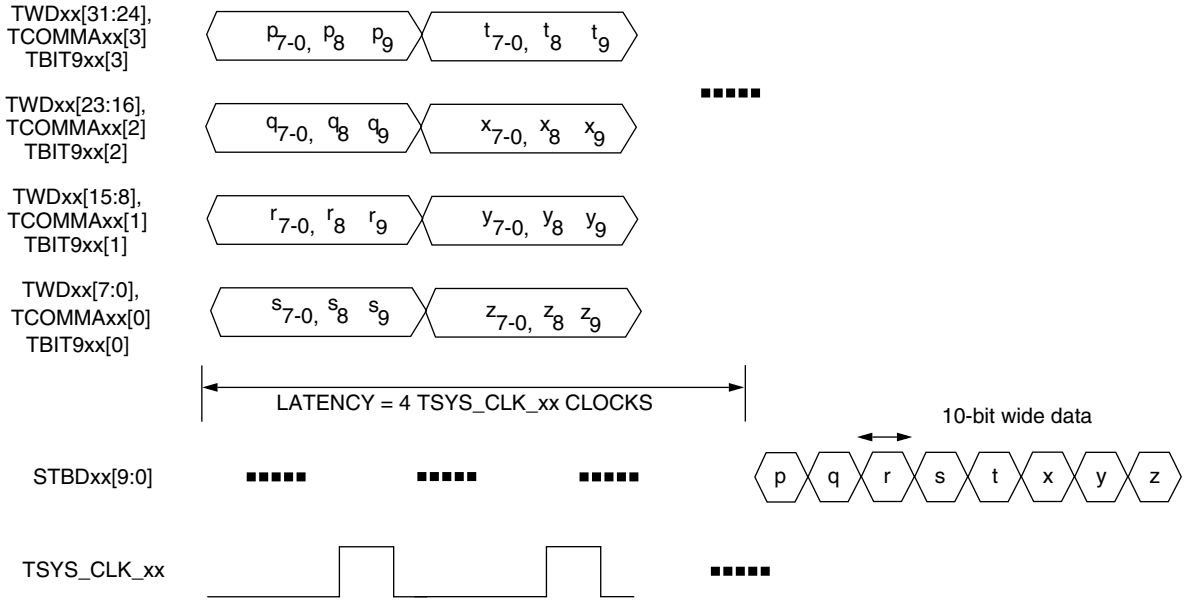
Embedded Core/FPGA Logic Interface and 4:1 Multiplexer

These blocks provide the data formatting and transmit data and clock signal transfers between the Embedded Core and the FPGA Logic. Control and status registers in the FPGA portion of the chip contain to control the transmit logic and record status. These bits are passed to the core using the FPGA System Bus and are described in later sections of this data sheet.

The low-speed transmit interface consists of a clock and 4 data bytes, each with an accompanying control bit. The data bytes are conveyed to the MUX via the TWDxx[31:0] ports (where xx represents the channel label [AA,...,BD] or [AC, AD, BC, BD]). The control bits are TCOMMAx[3:0] which define whether the input byte is to be interpreted as data or as a special character and TBIT9xx[3:0] which are used to force a negative disparity present state. The data and control signals are synchronized to the transmit clock, TSYS_CLK_xx. Both the data and control are strobed into the core on the rising edge of TSYS_CLK_xx. Note that each TBIT9xx[3:0] controls the disparity of the encoded version of its corresponding data byte. Setting bit TBIT9AC[3] to 1, for instance, will force the 8b/10b encoder to assess a current negative running disparity state. This will cause it to encode TWDAC[31:24] positively (more 1's than 0's). Setting TBIT9xx to 0 will leave the encoder free to alternate between positive and negative encoding to maintain a zero running disparity.

The MUX is responsible for taking 40 bits of data/control at the low-speed transmit interface and up-converting it to 10 bits of data/control at the SERDES transmit interface. The MUX has 2 clock domains - one based on the clock received from the SERDES block and a second that comes from the FPGA at 1/4 the frequency of the SERDES clock. The time sequence of interleaving data/control values is shown in Figure 4.

Figure 4. Transmit MUX Block Timing - Single Channel

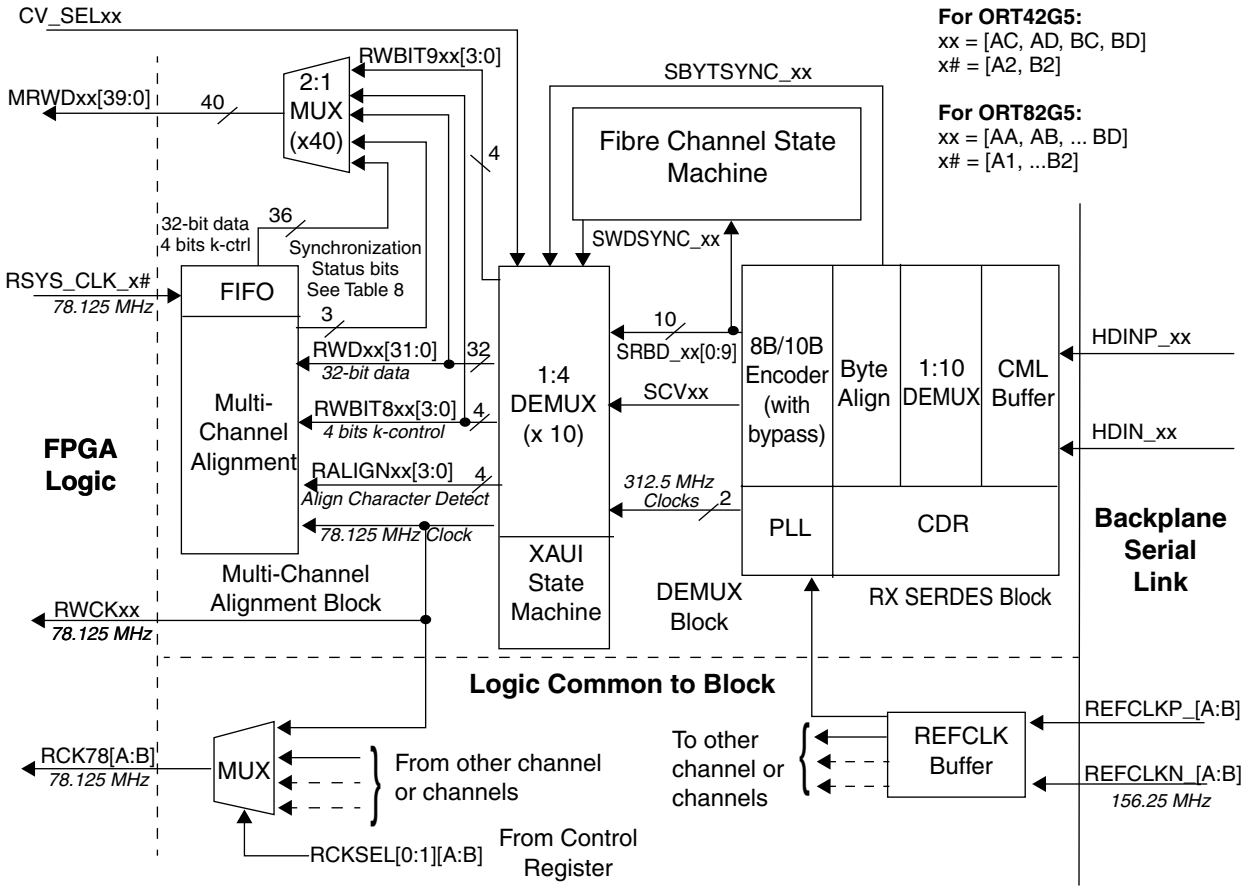


SERDES Block

The SERDES block accepts either 8-bit data to be encoded or 10-bit unencoded data at the parallel input port from the MUX/DEMUX block. It also accepts the reference clock at the REFCLK_[A:B] input and uses this clock to synthesize the internal high-speed serial bit clock.

The internal STBC311xx clock is derived from the reference clock. The frequency of this clock depends on the setting of the half-rate/full-rate control bit setting the mode of the SERDES and the frequency of the REFCLK_[A:B] and/or that of the high-speed serial data. A falling edge on the STBC311xx clock port will cause a new data character to be transferred into the SERDES block. The latency from the SERDES block input to the high-speed serial output is 5 STBC311xx clock cycles, as shown in Figure 5.

Figure 6. Basic Logic Blocks, Receive Path, Single Channel (Typical Reference Clock Frequency)



Each channel provides its own received clock, received data and K-character detect signals to the FPGA logic. Incoming data from multiple channels can be aligned using comma (/K/) characters or /A/ character (as specified either in Fibre Channel specifications or in IEEE 802.3ae for XAUI based interfaces). If the 8b/10b decoders are bypassed, then 40-bit data streams are passed to the FPGA logic. No channel alignment can be done in this 8b/10b bypass mode.

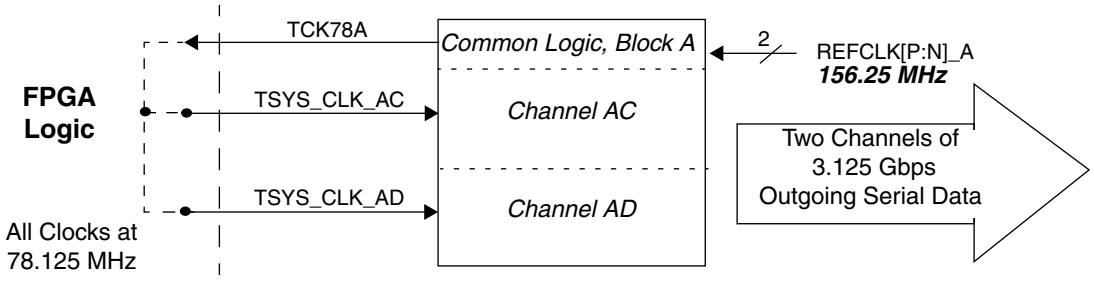
Detailed descriptions of data synchronization, of the SERDES, DEMUX and Multi-Channel Alignment blocks and of the Fibre Channel and XAUI state machines are given in following sections. Receive clock distribution is described in a later section of this data sheet.

Synchronization

The SERDES RX logic performs four levels of synchronization on the incoming serial data stream. Each level builds upon the previous, providing first bit, then byte (character), then channel (32-bit word), and finally multi-channel alignment. Each step is described functionally in the following paragraphs. The details of the logical implementations are described in subsequent sections.

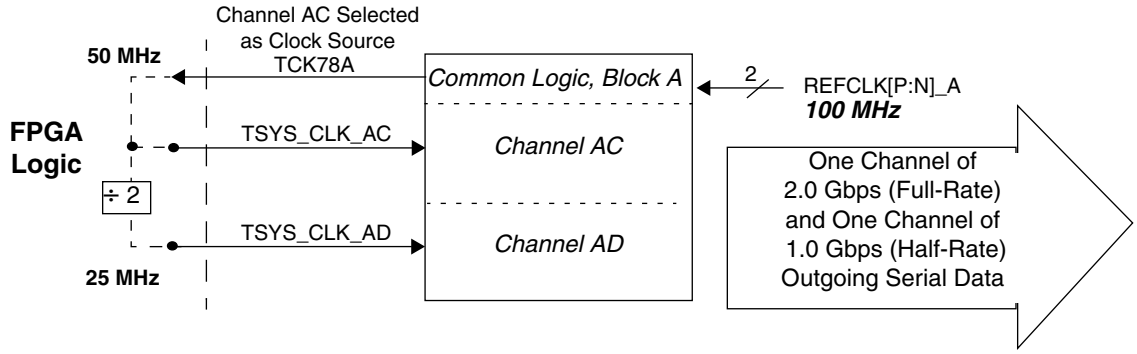
Bit alignment is the task of the Clock/Data Recovery (CDR) block. This block utilizes a PLL that locks to the transitions in the incoming high-speed serial data stream, and outputs the extracted clock as well as the data. If the PLL is unable to lock to the serial data stream, it instead locks to REFCLK[A:B] to stabilize the voltage-controlled oscillator (VCO), and periodically switches back to the serial data stream to again attempt synchronization. This process continues until a valid input data stream is detected and lock is achieved. The CDR can maintain lock on data as long as the input data stream contains an adequate data “eye” (i.e., jitter is within specification) and the maximum data stream run length is not exceeded.

Figure 18. Transmit Clocking for a Single Block (Similar Connections Would Be Used for Block B)



If the transmit line rate is mixed between half and full rate among the channels, then the scheme shown in Figure 19 can be used. The figure shows TSYS_CLK_AC being sourced by TCK78A and TSYS_CLK_AD being sourced by TCK78A/2 (the division is done in FPGA logic). Similar clocking would be used for Block B.

Figure 19. Mixed Rate Transmit Clocking for a Single Block (Similar Connections Would Be Used for Block B)



Receive Clock Source Selection and Recommended Clock Distribution

In the receive path, one clock per block of two channels, called RCK78[A:B], is sent to the FPGA logic. The control register bits RCKSEL[A:B] is used to select the clock source for these clocks. The selection of the source for RCK78[A:B] is controlled by this bit as shown in Table 15.

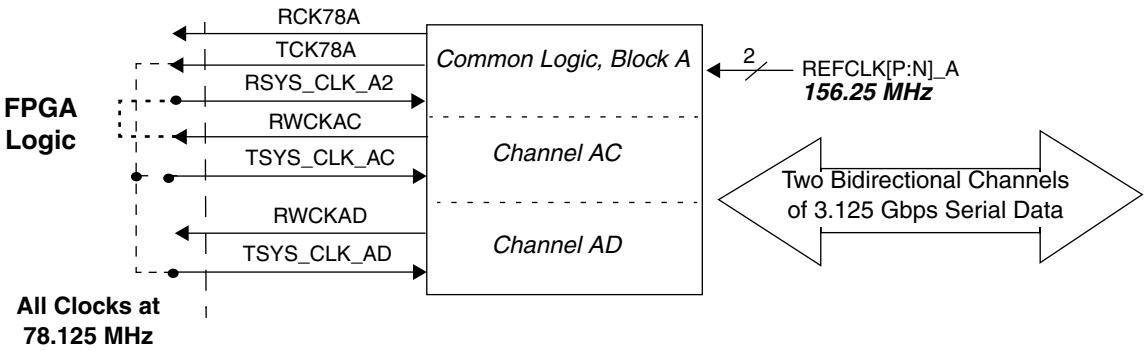
Table 15. RCK78[A:B] Source Selection

RCKSEL[A:B]	Clock Source
0	Channel C
1	Channel D

In the receive channel alignment bypass mode the data and recovered clocks for the four channels are independent. The data for each channel are synchronized to the recovered clock from that channel.

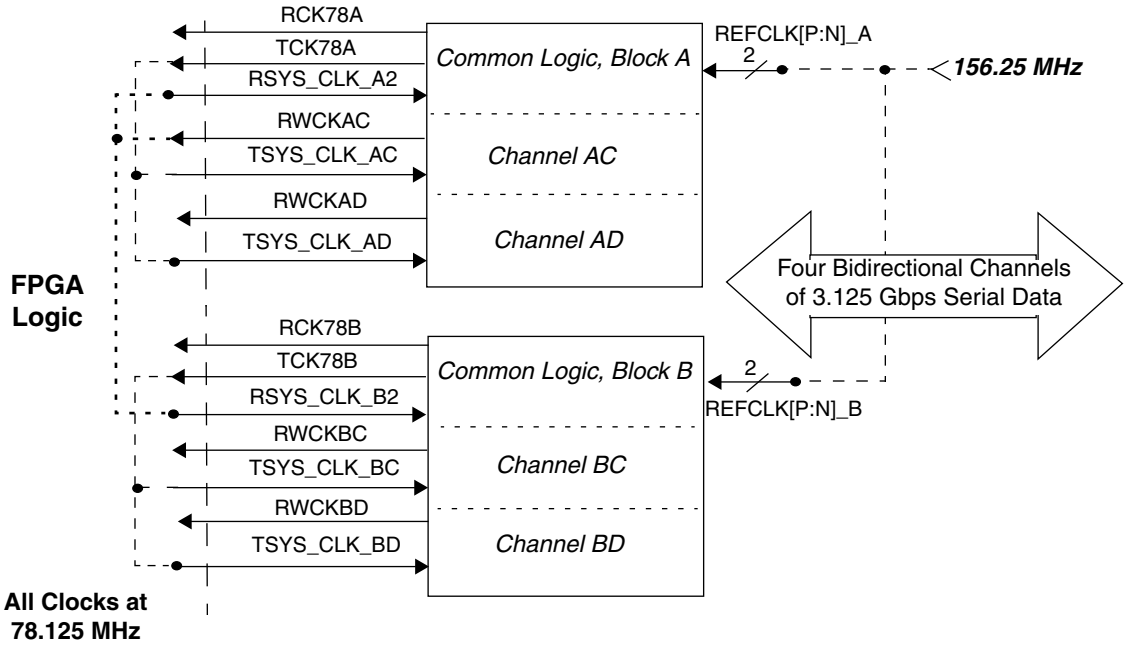
Figure 21 shows the recommended receive clocking for a single block.

Figure 22. Receive Clocking for a Dual Alignment in a Single Block (Similar Connections Would Be Used for Block B)



For quad alignment, either RCK78A or RCK78B can be used to source RSYS_CLK_[A:B]2 as shown in Figure 23.

Figure 23. Clocking for Quad Alignment



RSYS_CLK_[A:B][1:2]
These clocks are inputs to the SERDES quad block A and B respectively from the FPGA. These are used by each channel as the read clock to read received data from the alignment FIFO within the embedded core. Clocks RSYS_CLK_A[1:2] are used by channels in the SERDES quad block A and RSYS_CLK_B[1:2] by channels in the SERDES quad block B. To guarantee that there is no overflow in the alignment FIFO, it is an absolute requirement that the write and read clocks be frequency locked within 0 ppm. Examples of how to achieve this are shown in the later section on recommended board-level clocking.

TCK78[A:B]:
This is a muxed output from the core to the FPGA across the core-FPGA interface of one of the 4 transmit SERDES clocks per quad operating at up to 92.5 MHz in the embedded core. There is one clock output per SERDES quad block.

TSYS_CLK[AA,…BD]:
These clocks are inputs to the SERDES quad block A and B respectively from the FPGA. These are used by each channel to control the timing of the Transmit Data Path. To guarantee correct transmit operation theses clocks must be frequency locked within 0 ppm to TCK78[A:B].

Transmit and Receive Clock Rates

Table 16 shows the typical relationship between the data rates, the reference clock, the transmit TCK78[A:B] clock and the receive RCK78[A:B] clock. The selection of full-rate or half-rate for a given reference clock speed is set by bits in the transmit and receive control registers and can be set per channel.

Table 16. Transmit Data and Clock Rates

Data Rate	Reference Clock	TCK78[A: B] and RCK78[A:B] Clocks	Rate of Channel Selected as Clock Source
0.6 Gbps	60 MHz	15 MHz	Half
1.0 Gbps	100 MHz	25 MHz	Half
1.25 Gbps	125 MHz	31.25 MHz	Half
2.0 Gbps	100 MHz	50 MHz	Full
2.5 Gbps	125 MHz	62.5 MHz	Full
3.125 Gbps	156 MHz	78 MHz	Full
3.7 Gbps	185 MHz	92.5 MHz	Full

Besides taking in a TSYS_CLK_xx from the FPGA logic for each channel, the transmit path logic sends back a clock of the same frequency, but arbitrary phase. This clock, TCK78[A:B], is derived from the MUX block of one of the 4 channels in its SERDES quad. The MUX blocks provide the potential source for TCK78[A:B] by a divide-by-4 of the SERDES STBC311xs clock used in synchronizing the transmit data words in the STBC311xx clock domain. The STBC311xx clocks are internal to the core and are not brought across the core/FPGA interface.

The receiver section receives high-speed serial data at its differential CML input port and sends in to the Clock and Data Recovery (CDR) block. The CDR block then generates a recovered clock (RWCKxx) and retimes the data. Thus, the recovered receive clocks are asynchronous between channels.

Transmit Clock Source Selection

The TCKSEL[0:1][A:B] bits select the source channel of TCK78[A:B]. The selection of the source for TCK78[A:B] is controlled by these bits as shown in Table 17.

Test Modes

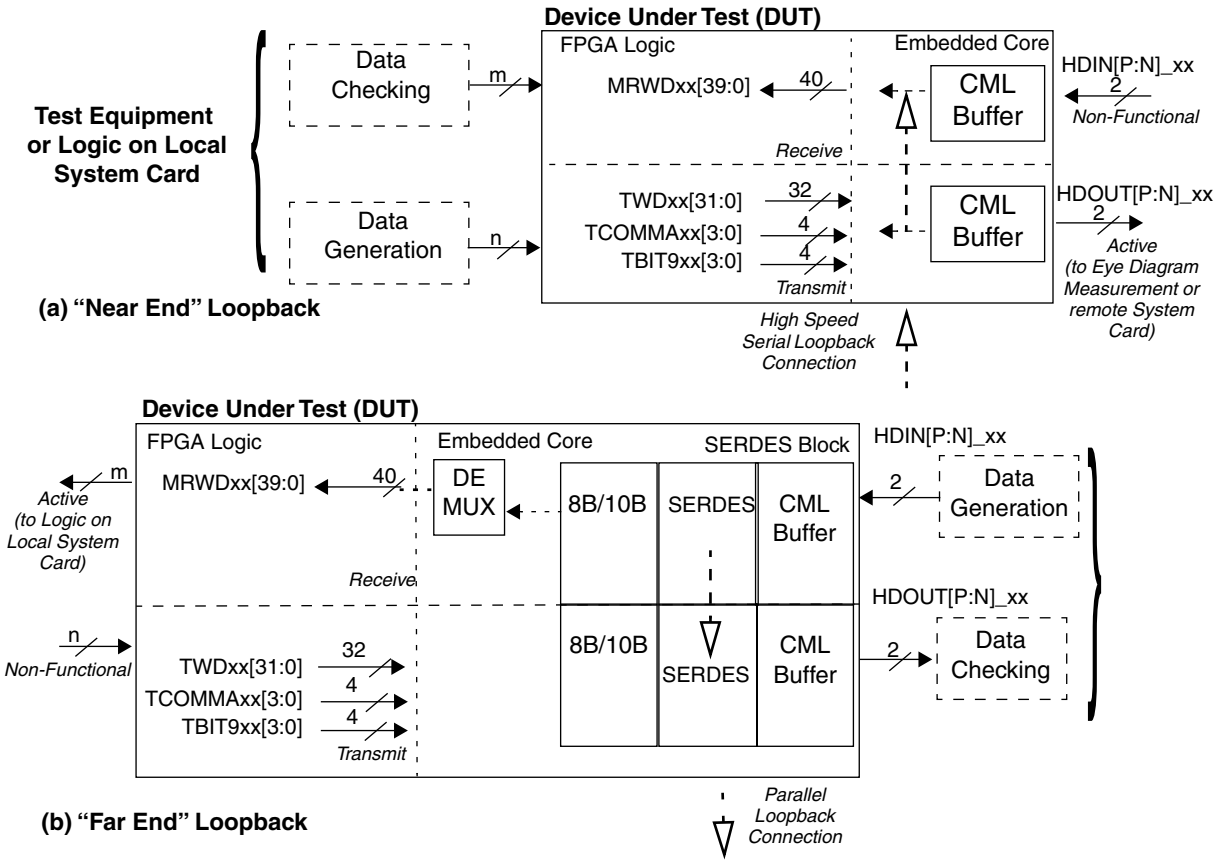
In addition to the operational logic described in the preceding sections, the Embedded Core contains logic to support various test modes - both for device validation and evaluation and for operating system level tests. The following sections discuss two of the test support logic blocks, supporting various loopback modes and SERDES characterization.

Loopback Testing

Loopback testing is performed by looping back (either internal to the Embedded Core, by configuring the FPGA logic or by external connections) transmitted data to the corresponding receiver inputs, or received data to the transmitter output. The loopback path may be either serial or parallel.

In general, loopback tests can be classified as “near end” or “far end.” In “near end” loopback (Figure 32(a)), data is generated and checked locally, i.e. by logic on, or connection of, test equipment to the same card as the FPSC. In “far end” loopback (Figure 32(b)), the generating and checking functions are performed remotely, either by test equipment or a remote system card.

Figure 32. “Near End” vs. “Far End” Loopback



The loopback mode can also be characterized by the physical location of the loopback connection. There are three possible loopback modes supported by the Embedded Core logic:

- High-speed serial loopback at the CML buffer interface (near end)
- Parallel loopback at the SERDES boundary (far end)

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Common Transmit and Receive Channel Configuration Registers (Read/Write), xx = [AC, AD, BC or BD]				
30022 - AC 30032 - AD 30122 - BC 30132 - BD	[0]	TXHR_xx	00	Transmit Half Rate Selection Bit, Channel xx. When TXHR_xx = 1, HDOUT_xx's baud rate = (REFCLK[A:B]*10) and TCK78[A:B] =(REFCLK[A:B]/4); when TXHR_xx=0, HDOUT_xx's baud rate = (REFCLK[A:B]*20) and TCK78[A:B]=(REFCLK[A:B]/2). TXHR_xx = 0 on device reset.
	[1]	PWRDNT_xx		Transmit Powerdown Control Bit, Channel xx. When PWRDNT_xx = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT_xx = 0 on device reset.
	[2]	PE0_xx		Transmit Preemphasis Selection Bit 0, Channel xx. PE0_xx and PE1_xx select one of three preemphasis settings for the transmit section. PEO_xx=PE1_xx = 0, Preemphasis is 0% PEO_xx=1, PE1_xx = 0 or PEO_xx=0, PE1_xx = 1, Preemphasis is 12.5% PEO_xx=PE1_xx = 1, Preemphasis is 25%. PEO_xx=PE1_xx = 0 on device reset.
	[3]	PE1_xx		
	[4]	HAMP_xx		Transmit Half Amplitude Selection Bit, Channel xx. When HAMP_xx = 1, the transmit output buffer voltage swing is limited to half its normal amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP_xx = 0 on device reset.
	[5]	Reserved		Reserved. Must be set to 0. Set to 0 on device reset.
	[6]	Reserved		Reserved
	[7]	8b10bT_xx		Transmit 8b/10b Encoder Enable Bit, Channel xx. When 8b10bT_xx = 1, the 8b/10b encoder in the transmit path is enabled. Otherwise, the data is passed unencoded. 8b10bT_xx = 0 on device reset.
30023 - AC 30033 - AD 30123 - BC 30133 - BD	[0]	RXHR_xx	20	Receive Half Rate Selection Bit, Channel xx. When RXHR_xx =1, HDIN_xx's baud rate = (REFCLK[A:B]*10) and RCK78[A:B]=(REFCLK[A:B]/4); when RXHR_xx=0, HDIN_xx's baud rate = (REFCLK[A:B]*20) and RCK78[A:B]=(REFCLK/2). RXHR_xx = 0 on device reset.
	[1]	PWRDNR_xx		Receiver Power Down Control Bit, Channel xx. When PWRDNR_xx = 1, sections of the receive hardware are powered down to conserve power. PWRDNR_xx = 0 on device reset.
	[2]	Reserved		Reserved. Set to 1 on device reset.
	[3]	8b10bR_xx		Receive 8b/10b Decoder Enable Bit, Channel xx. When 8b10bR = 1, the 8b/10b decoder in the receive path is enabled. Otherwise, the data is passed undecoded. 8b10bR_xx = 0 on device reset.
	[4]	LINKSM_xx		Link State Machine Enable Bit, Channel xx. When LINKSM_xx = 1, the receiver Fiber Channel link state machine is enabled. Otherwise, the Fibre Channel link state machine is disabled. Note: LINKSM_xx is ignored when XAUI_MODE_xx=1. LINKSM_xx = 0 on device reset.
	[5:7]	Not used		Not used.

Table 30. ORT82G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30805 - Ax 30905 - Bx	[0]xA [1]xB [2]xC [3]xD	DEMUXWAS_xx	00	Status of Word Alignment. When DEMUX_WAS_xx=1, word alignment is achieved for Channel xx. DEMUX_WAS_xx=0 on device reset.
	[4]xA [5]xB [6]xC [7]xD	CH248_SYNC_xx		Status of Channel Alignment. When CH248_SYNC_xx=1, multi-channel alignment is achieved for Channel xx. CH248_SYNC_xx=0 on device reset.
30814 - Ax 30914 - Bx	[0] xA & AB [1] xC & xD	SYNC2_[A:B][1:2] OVFL	00	Multi-Channel Overflow Status. When SYNC2_[A:B][1:2]OVFL=1, dual-channel synchronization FIFO overflow has occurred. SYNC2_[A:B][1:2]OVFL=0 on device reset.
	[2]	SYNC4_ [A:B]OVFL		Multi-Channel Overflow Status. When SYNC4_[A:B]OVFL=1, quad-channel synchronization FIFO overflow has occurred. SYNC4_[A:B]OVFL=0 on device reset.
	[3] xA & AB [4] xC & xD	SYNC2_[A:B][1:2] OOS		Multi-Channel Out-Of-Sync Status. When SYNC2_[A:B][1:2] OOS=1, dual-channel synchronization has failed. SYNC2_[A:B][1:2] OOS=0 on device reset.
	[5]	SYNC4_[A:B]_OOS		Multi-Channel Out-Of-Sync Status. When SYNC4_[A:B]_OOS=1, quad-channel synchronization has failed. SYNC4_[A:B]_OOS=0 on device reset.
	[6:7]	Reserved for future use.		
Common Control Registers (Read/Write)				
30A00	[0:1]	TCKSELA	00	Transmit Clock Select. Controls source of 78 MHz TCK78 for SERDES quad A 00 = Channel AA 10 = Channel AB 01 = Channel AC 11 = Channel AD
	[2:3	RCKSELA		Receive Clock Select. Controls source of 78 MHz RCK78 for SEDRES quad A 00 = Channel AA 10 = Channel AB 01 = Channel AC 11 = Channel AD
	[4:5]	TCKSELB		Transmit Clock Select. Controls source of 78 MHz TCK78 for SERDES quad B 00 = Channel BA 10 = Channel BB 01 = Channel BC 11 = Channel BD
	[6:7]	RCKSELB		Receive Clock Select. Controls source of 78 MHz RCK78 for SERDES quad B 00 = Channel BA 10 = Channel BB 01 = Channel BC 11 = Channel BD
30A01	[0:4]	—	00	Reserved for future use
	[5:7]	RX_FIFO_MIN		LSb's for the threshold for low address in RX_FIFOs. RX_FIFO_MIN, Bit 5 is LSb. Useful values for RX_FIFO_MIN [0:4] are 0 to 17(decimal).

Table 40. Pin Descriptions (Continued)

Symbol	I/O	Description
TDI, TCK, TMS	I	If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O if boundary scan is not used.[1]
RDY/$\overline{\text{BUSY}}$/RCLK	O	During configuration in asynchronous peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
	I/O	After configuration this pin is a user-programmable I/O pin.[1]
HDC	O	High During Configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
LDC	O	$\overline{\text{Low During Configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
INIT	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration. After configuration, this pin is a user-programmable I/O pin.[1]
$\overline{\text{CS0}}$, CS1	I	$\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, if MPI is not used, these pins are user-programmable I/O pins.[1]
$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$	I	$\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D[7:3] into a status output. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the MPI data transfer strobe. As a status indication, a high indicates ready, and a low indicates busy.
$\overline{\text{WR}}$/MPI_RW	I	$\overline{\text{WR}}$ is used in asynchronous peripheral mode. A low on $\overline{\text{WR}}$ transfers data on D[7:0] to the FPGA. In MPI mode, a high on MPI_RW allows a read from the data bus, while a low causes a write transfer to the FPGA.
	I/O	After configuration, if the MPI is not used, $\overline{\text{WR}}$/MPI_RW is a user-programmable I/O pin.[1]
PPC_A[14:31]	I	During MPI mode the PPC_A[14:31] are used as the address bus driven by the PowerPC bus master utilizing the least-significant bits of the PowerPC 32-bit address.
MPI_BURST	I	$\overline{\text{MPI\_BURST}}$ is driven low to indicate a burst transfer is in progress in MPI mode. Driven high indicates that the current transfer is not a burst.
MPI_BDIP	I	$\overline{\text{MPI\_BDIP}}$ is driven by the PowerPC processor in MPI mode. Assertion of this pin indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.
MPI_TSZ[0:1]	I	MPI_TSZ[0:1] signals are driven by the bus master in MPI mode to indicate the data transfer size for the transaction. Set 01 for byte, 10 for half-word, and 00 for word.
A[21:0]	O	During master parallel mode A[21:0] address the configuration EPROMs up to 4M bytes.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_ACK	O	In MPI mode this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]

This section describes device I/O signals to/from the embedded core.

Table 41. FPSC Function Pin Descriptions

Symbol	I/O	Description
Common Signals for Both SERDES Quad A and B		
PASB_RESETN	I	Active low reset for the embedded core. All non-SERDES specific registers (addresses 308***, 309***, 30A***) in the embedded core are not reset.[1]
PASB_TRISTN	I	Active low 3-state for embedded core output buffers.[1]
PASB_PDN	I	Active low power down of all SERDES blocks and associated I/Os.[1]
PASB_TESTCLK	I	Clock input for BIST and loopback test.[1]
PBIST_TEST_ENN	I	Selection of PASB_TESTCLK input for BIST test.[1]
PLOOP_TEST_ENN	I	Selection of PASB_TESTCLK input for loopback test.[1]
PMP_TESTCLK	I	Clock input for microprocessor in test mode.[1]
PMP_TESTCLK_ENN	I	Selection of PMP_TESTCLK in test mode.[1]
PSYS_DOBISTN	I	Input to start BIST test.[1]
PSYS_RSSIG_ALL	O	Output result of BIST test.
SERDES Quad A and B Pins		
REFCLKN_A	I	CML reference clock input—SERDES quad A.
REFCLKP_A	I	CML reference clock input—SERDES quad A.
REFCLKN_B	I	CML reference clock input—SERDES quad B.
REFCLKP_B	I	CML reference clock input—SERDES quad B.
REXT_A	—	Reference resistor – SERDES quad A.
REXT_B	—	Reference resistor – SERDES quad B.
REXTN_A	—	Reference resistor – SERDES quad -. A 3.32 K W ± 1% resistor must be connected across REXT_B and REXTN_B. This resistor should handle a current of 300 µA.
REXTN_B	—	Reference resistor – SERDES quad B. A 3.32 K Ω ± 1% resistor must be connected across REXT_B and REXTN_B. This register should handle a current of 300 µA
HDINN_AA (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad A, channel A.
HDINP_AA (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad A, channel A.
HDINN_AB (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad A, channel B.
HDINP_AB (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad A, channel B.
HDINN_AC	I	High-speed CML receive data input – SERDES quad A, channel C.
HDINP_AC	I	High-speed CML receive data input – SERDES quad A, channel C.
HDINN_AD	I	High-speed CML receive data input – SERDES quad A, channel D.
HDINP_AD	I	High-speed CML receive data input – SERDES quad A, channel D.
HDINN_BA (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad B, channel A.
HDINP_BA (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad B, channel A.
HDINN_BB (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad B, channel B.
HDINP_BB (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad B, channel B.
HDINN_BC	I	High-speed CML receive data input – SERDES quad B, channel C.
HDINP_BC	I	High-speed CML receive data input – SERDES quad B, channel C.
HDINN_BD	I	High-speed CML receive data input – SERDES quad B, channel D.
HDINP_BD	I	High-speed CML receive data input – SERDES quad B, channel D.
SERDES quad A and B Pins		
HDOUTN_AA (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad A, channel A.
HDOUTP_AA (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad A, channel A.
HDOUTN_AB (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad A, channel B.

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
E4	-	-	O	PRD_DATA	RD_DATA/TDO	-
C20	-	-	VDD15	VDD15	-	-
D3	-	-	I	PRESET_N	RESET_N	-
F5	-	-	I	PRD_CFG_N	RD_CFG_N	-
F4	-	-	I	PPRGRM_N	PRGRM_N	-
C2	0 (TL)	7	IO	PL2D	PLL_CK0C/HPPLL	L1C
C1	0 (TL)	7	IO	PL2C	PLL_CK0T/HPPLL	L1T
F3	0 (TL)	7	IO	PL3C	VREF_0_07	-
A1	-	-	VSS	VSS	-	-
D2	0 (TL)	7	IO	PL4D	D5	L2C
D1	0 (TL)	7	IO	PL4C	D6	L2T
E7	0 (TL)	-	VDDIO0	VDDIO0	-	-
E2	0 (TL)	8	IO	PL5D	HDC	L3C
E1	0 (TL)	8	IO	PL5C	LDC_N	L3T
G3	0 (TL)	8	IO	PL5A	-	-
G4	0 (TL)	9	IO	PL6C	D7	-
F2	0 (TL)	9	IO	PL7D	VREF_0_09	L4C
F1	0 (TL)	9	IO	PL7C	A17/PPC_A31	L4T
G2	0 (TL)	9	IO	PL8D	CS0_N	L5C
G1	0 (TL)	9	IO	PL8C	CS1	L5T
E8	0 (TL)	-	VDDIO0	VDDIO0	-	-
A2	-	-	VSS	VSS	-	-
H1	0 (TL)	10	IO	PL10D	INIT_N	L6C
H2	0 (TL)	10	IO	PL10C	DOUT	L6T
E5	-	-	VDD15	VDD15	-	-
H4	0 (TL)	10	IO	PL11D	VREF_0_10	-
H3	0 (TL)	10	IO	PL11C	A16/PPC_A30	-
J1	7 (CL)	1	IO	PL12D	A15/PPC_A29	L7C
J2	7 (CL)	1	IO	PL12C	A14/PPC_A28	L7T
J4	7 (CL)	1	IO	PL13C	D4	-
G7	-	-	VSS	VSS	-	-
J3	7 (CL)	2	IO	PL14D	RDY/BUSY_N/RCLK	-
K6	7 (CL)	-	VDDIO7	VDDIO7	-	-
K1	7 (CL)	2	IO	PL15D	A13/PPC_A27	L8C
K2	7 (CL)	2	IO	PL15C	A12/PPC_A26	L8T
K3	7 (CL)	3	IO	PL16C	-	-
K4	7 (CL)	3	IO	PL17D	A11/PPC_A25	-
G8	-	-	VSS	VSS	-	-
F8	-	-	VDD15	VDD15	-	-
K5	7 (CL)	4	IO	PL19D	RD_N/MPI_STRB_N	-
L1	7 (CL)	4	IO	PL20D	PLCK0C	L9C
L2	7 (CL)	4	IO	PL20C	PLCK0T	L9T
L6	7 (CL)	-	VDDIO7	VDDIO7	-	-
F9	-	-	VDD15	VDD15	-	-

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
V9	5 (BC)	1	IO	PB17A	-	-
W9	5 (BC)	1	IO	PB17C	-	L35T
Y9	5 (BC)	1	IO	PB17D	-	L35C
U9	5 (BC)	1	IO	PB18A	-	-
AA9	5 (BC)	1	IO	PB18C	VREF_5_01	L36T
AB9	5 (BC)	1	IO	PB18D	-	L36C
G16	-	-	VDD15	VDD15	-	-
H13	-	-	VSS	VSS	-	-
AB10	5 (BC)	2	IO	PB19A	-	L37T
AA10	5 (BC)	2	IO	PB19B	-	L37C
W10	5 (BC)	2	IO	PB19C	PBCK0T	L38T
Y10	5 (BC)	2	IO	PB19D	PBCK0C	L38C
V10	5 (BC)	2	IO	PB20A	-	-
U13	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB11	5 (BC)	2	IO	PB20C	VREF_5_02	L39T
AA11	5 (BC)	2	IO	PB20D	-	L39C
U10	5 (BC)	2	IO	PB21A	-	-
H6	-	-	VDD15	VDD15	-	-
Y11	5 (BC)	3	IO	PB21C	-	L40T
W11	5 (BC)	3	IO	PB21D	VREF_5_03	L40C
U11	5 (BC)	3	IO	PB22A	-	-
J7	-	-	VSS	VSS	-	-
AB12	5 (BC)	3	IO	PB22C	-	L41T
AA12	5 (BC)	3	IO	PB22D	-	L41C
U12	5 (BC)	3	IO	PB23A	-	-
Y12	5 (BC)	3	IO	PB23C	PBCK1T	L42T
W12	5 (BC)	3	IO	PB23D	PBCK1C	L42C
V11	5 (BC)	3	IO	PB24A	-	-
J8	-	-	VSS	VSS	-	-
AB13	5 (BC)	4	IO	PB24C	-	L43T
AA13	5 (BC)	4	IO	PB24D	-	L43C
V12	5 (BC)	4	IO	PB25A	-	-
U14	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB14	5 (BC)	4	IO	PB25C	-	L44T
AA14	5 (BC)	4	IO	PB25D	VREF_5_04	L44C
J9	-	-	VSS	VSS	-	-
Y13	5 (BC)	5	IO	PB26C	-	L45T
W13	5 (BC)	5	IO	PB26D	VREF_5_05	L45C
U15	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB15	5 (BC)	5	IO	PB27C	-	L46T
AA15	5 (BC)	5	IO	PB27D	-	L46C
AB16	5 (BC)	6	IO	PB28C	-	L47T
AA16	5 (BC)	6	IO	PB28D	VREF_5_06	L47C
H14	-	-	VDD15	VDD15	-	-

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
L11	-	-	VSS	VSS	-	-
N15	-	-	VDD15	VDD15	-	-
D10	1 (TC)	5	IO	PT18D	PTCK1C	L68C
C10	1 (TC)	5	IO	PT18C	PTCK1T	L68T
A12	1 (TC)	5	IO	PT17D	PTCK0C	L69C
B12	1 (TC)	5	IO	PT17C	PTCK0T	L69T
P6	-	-	VDD15	VDD15	-	-
A11	1 (TC)	5	IO	PT16D	VREF_1_05	L70C
B11	1 (TC)	5	IO	PT16C	-	L70T
L12	-	-	VSS	VSS	-	-
D9	1 (TC)	6	IO	PT15D	-	L71C
C9	1 (TC)	6	IO	PT15C	-	L71T
G15	1 (TC)	-	VDDIO1	VDDIO1	-	-
B10	1 (TC)	6	IO	PT14D	-	L72C
A10	1 (TC)	6	IO	PT14C	VREF_1_06	L72T
B9	0 (TL)	1	IO	PT13D	MPI_RTRY_N	L73C
A9	0 (TL)	1	IO	PT13C	MPI_ACK_N	L73T
D8	0 (TL)	1	IO	PT12D	M0	L74C
C8	0 (TL)	1	IO	PT12C	M1	L74T
A22	-	-	VSS	VSS	-	-
B8	0 (TL)	2	IO	PT12B	MPI_CLK	L75C
A8	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L75T
C7	0 (TL)	2	IO	PT11D	M2	L76C
D7	0 (TL)	2	IO	PT11C	M3	L76T
E9	0 (TL)	-	VDDIO0	VDDIO0	-	-
E6	0 (TL)	2	IO	PT11A	MPI_TEA_N	-
F6	-	-	VDD15	VDD15	-	-
B7	0 (TL)	3	IO	PT9D	VREF_0_03	L77C
A7	0 (TL)	3	IO	PT9C	-	L77T
A6	0 (TL)	3	IO	PT8D	D0	L78C
B6	0 (TL)	3	IO	PT8C	TMS	L78T
C6	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L79C
D6	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L79T
B1	-	-	VSS	VSS	-	-
A5	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L80C
B5	0 (TL)	4	IO	PT6C	D3	L80T
C5	0 (TL)	5	IO	PT5D	D1	L81C
D5	0 (TL)	5	IO	PT5C	D2	L81T
B2	-	-	VSS	VSS	-	-
A4	0 (TL)	5	IO	PT4D	TDI	L82C
B4	0 (TL)	5	IO	PT4C	TCK	L82T
E10	0 (TL)	-	VDDIO0	VDDIO0	-	-
B22	-	-	VSS	VSS	-	-
C4	0 (TL)	6	IO	PT2D	PLL_CK1C/PPLL	L83C

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
D4	0 (TL)	6	IO	PT2C	PLL_CK1T/PPLL	L83T
A3	-	-	O	PCFG_MPI_IRQ	CFG_IRQ_N/MPI_IRQ_N	-
B3	-	-	IO	PCCLK	CCLK	-
F7	-	-	VDD15	VDD15	-	-
C3	-	-	IO	PDONE	DONE	-
E3	-	-	VDD33	VDD33	-	-
P15	-	-	VDD15	VDD15	-	-
R6	-	-	VDD15	VDD15	-	-
R15	-	-	VDD15	VDD15	-	-
T4	-	-	VDD15	VDD15	-	-
W19	-	-	VDD15	VDD15	-	-
Y3	-	-	VDD15	VDD15	-	-
Y19	-	-	VDD15	VDD15	-	-
Y20	-	-	VDD15	VDD15	-	-
T15	-	-	VDD15	VDD15	-	-
T16	-	-	VDD15	VDD15	-	-
U4	-	-	VDD15	VDD15	-	-
T12	-	-	VDD15	VDD15	-	-
T13	-	-	VDD15	VDD15	-	-
T14	-	-	VDD15	VDD15	-	-
T6	-	-	VDD15	VDD15	-	-
T7	-	-	VDD15	VDD15	-	-
T10	-	-	VDD15	VDD15	-	-
T11	-	-	VDD15	VDD15	-	-
G5	0 (TL)	-	VDDIO0	VDDIO0	-	-
H5	0 (TL)	-	VDDIO0	VDDIO0	-	-
J5	0 (TL)	-	VDDIO0	VDDIO0	-	-
V17	5 (BC)	-	VDDIO5	VDDIO5	-	-
W17	5 (BC)	-	VDDIO5	VDDIO5	-	-
W18	5 (BC)	-	VDDIO5	VDDIO5	-	-
M6	7 (CL)	-	VDDIO7	VDDIO7	-	-
N6	7 (CL)	-	VDDIO7	VDDIO7	-	-
U5	-	-	VDD15	VDD15	-	-
U17	-	-	VDD15	VDD15	-	-
V5	-	-	VDD15	VDD15	-	-
V18	-	-	VDD15	VDD15	-	-
R18	-	-	VSS	VSS	-	-
R19	-	-	VSS	VSS	-	-
T19	-	-	VSS	VSS	-	-
U19	-	-	VSS	VSS	-	-
U20	-	-	VSS	VSS	-	-
V19	-	-	VSS	VSS	-	-
V20	-	-	VSS	VSS	-	-
W20	-	-	VSS	VSS	-	-

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AM12	6 (BL)	9	IO	PB12B	—	L28C_A0
AP12	6 (BL)	9	IO	PB12C	VREF_6_09	L29T_A0
AP13	6 (BL)	9	IO	PB12D	D25	L29C_A0
AM13	6 (BL)	9	IO	PB13A	—	L30T_D0
AN14	6 (BL)	9	IO	PB13B	—	L30C_D0
V17	—	—	VSS	VSS	—	—
AP14	6 (BL)	10	IO	PB13C	D26	L31T_A0
AP15	6 (BL)	10	IO	PB13D	D27	L31C_A0
AK13	6 (BL)	10	IO	PB14A	—	L32T_A0
AK14	6 (BL)	10	IO	PB14B	—	L32C_A0
AM14	6 (BL)	10	IO	PB14C	VREF_6_10	L33T_A0
AL14	6 (BL)	10	IO	PB14D	D28	L33C_A0
AP17	6 (BL)	11	IO	PB15A	—	L34T_A0
AP16	6 (BL)	11	IO	PB15B	—	L34C_A0
AM15	6 (BL)	11	IO	PB15C	D29	L35T_D0
AN16	6 (BL)	11	IO	PB15D	D30	L35C_D0
AM17	6 (BL)	11	IO	PB16A	—	L36T_A0
AM16	6 (BL)	11	IO	PB16B	—	L36C_A0
AP18	6 (BL)	11	IO	PB16C	VREF_6_11	L37T_A0
AP19	6 (BL)	11	IO	PB16D	D31	L37C_A0
AL16	5 (BC)	1	IO	PB17A	—	L1T_D0
AK15	5 (BC)	1	IO	PB17B	—	L1C_D0
N22	—	—	VSS	VSS	—	—
AN18	5 (BC)	1	IO	PB17C	—	L2T_A0
AN19	5 (BC)	1	IO	PB17D	—	L2C_A0
AP20	5 (BC)	1	IO	PB18A	—	L3T_A0
AP21	5 (BC)	1	IO	PB18B	—	L3C_A0
AL17	5 (BC)	1	IO	PB18C	VREF_5_01	L4T_D0
AK16	5 (BC)	1	IO	PB18D	—	L4C_D0
P13	—	—	VSS	VSS	—	—
AM19	5 (BC)	2	IO	PB19A	—	L5T_A0
AM18	5 (BC)	2	IO	PB19B	—	L5C_A0
P14	—	—	VSS	VSS	—	—
AN20	5 (BC)	2	IO	PB19C	PBCK0T	L6T_A0
AM20	5 (BC)	2	IO	PB19D	PBCK0C	L6C_A0
AK17	5 (BC)	2	IO	PB20A	—	L7T_D0
AL18	5 (BC)	2	IO	PB20B	—	L7C_D0
AL11	5 (BC)	—	VDDIO5	VDDIO5	—	—
AP22	5 (BC)	2	IO	PB20C	VREF_5_02	L8T_D0
AN21	5 (BC)	2	IO	PB20D	—	L8C_D0
AM22	5 (BC)	2	IO	PB21A	—	L9T_A0
AM21	5 (BC)	2	IO	PB21B	—	L9C_A0
AP23	5 (BC)	3	IO	PB21C	—	L10T_D0
AN22	5 (BC)	3	IO	PB21D	VREF_5_03	L10C_D0

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
B29	1 (TC)	8	IO	PT33D	—	L1C_A0
C29	1 (TC)	8	IO	PT33C	VREF_1_08	L1T_A0
B15	1 (TC)	—	VDDIO1	VDDIO1	—	—
E27	1 (TC)	8	IO	PT32D	—	L2C_A0
E26	1 (TC)	8	IO	PT32C	—	L2T_A0
AP34	—	—	Vss	Vss	—	—
A30	1 (TC)	8	IO	PT32B	—	—
A29	1 (TC)	9	IO	PT31D	—	L3C_D3
E25	1 (TC)	9	IO	PT31C	VREF_1_09	L3T_D3
B17	1 (TC)	—	VDDIO1	VDDIO1	—	—
E24	1 (TC)	9	IO	PT31A	—	—
B28	1 (TC)	9	IO	PT30D	—	L4C_A0
C28	1 (TC)	9	IO	PT30C	—	L4T_A0
B2	—	—	Vss	Vss	—	—
D28	1 (TC)	9	IO	PT30A	—	—
C27	1 (TC)	9	IO	PT29D	—	L5C_A0
D27	1 (TC)	9	IO	PT29C	—	L5T_A0
E23	1 (TC)	9	IO	PT29B	—	L6C_A0
E22	1 (TC)	9	IO	PT29A	—	L6T_A0
D26	1 (TC)	1	IO	PT28D	—	L7C_A0
D25	1 (TC)	1	IO	PT28C	—	L7T_A0
B33	—	—	Vss	Vss	—	—
D24	1 (TC)	1	IO	PT28B	—	L8C_A0
D23	1 (TC)	1	IO	PT28A	—	L8T_A0
C26	1 (TC)	1	IO	PT27D	VREF_1_01	L9C_A0
C25	1 (TC)	1	IO	PT27C	—	L9T_A0
D11	1 (TC)	—	VDDIO1	VDDIO1	—	—
E21	1 (TC)	1	IO	PT27B	—	L10C_A0
E20	1 (TC)	1	IO	PT27A	—	L10T_A0
D22	1 (TC)	2	IO	PT26D	—	L11C_A0
D21	1 (TC)	2	IO	PT26C	VREF_1_02	L11T_A0
E34	—	—	Vss	Vss	—	—
A28	1 (TC)	2	IO	PT26B	—	—
B26	1 (TC)	2	IO	PT25D	—	L12C_A0
B25	1 (TC)	2	IO	PT25C	—	L12T_A0
D13	1 (TC)	—	VDDIO1	VDDIO1	—	—
B27	1 (TC)	2	IO	PT25B	—	—
A27	1 (TC)	3	IO	PT24D	—	L13C_A0
A26	1 (TC)	3	IO	PT24C	VREF_1_03	L13T_A0
N13	—	—	Vss	Vss	—	—
C24	1 (TC)	3	IO	PT24B	—	—
C22	1 (TC)	3	IO	PT23D	—	L14C_A0
C23	1 (TC)	3	IO	PT23C	—	L14T_A0
D15	1 (TC)	—	VDDIO1	VDDIO1	—	—