Lattice Semiconductor Corporation - ORT42G5-2BM484C Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	204
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort42g5-2bm484c

Embedded Function Features

- High-speed SERDES with programmable serial data rates over the range 0.6 to 3.7 Gbps. Operation has been demonstrated on design tolerance devices at 3.7 Gbps across 26 in. of FR-4 backplane and at 3.125 Gbps across 40 in. of FR-4 backplane across temperature and voltage specifications.
- Asynchronous operation per receive channel with the receiver frequency tolerance based on one reference clock per block channels (separate PLL per channel).
- Ability to select full-rate or half-rate operation per transmit or receive channel by setting the appropriate control registers.
- Programmable one-half amplitude transmit mode for reduced power in chip-to-chip application.
- Transmit preemphasis (programmable) for improved receive data eye opening.
- 32-bit (8b/10b) or 40-bit (raw data) parallel internal bus for data processing in FPGA logic.
- Provides a 10 Gbps backplane interface to switch fabric. Also supports multiple port cards at 2.5 Gbps.
- 3.125 Gbps SERDES compliant with XAUI serial data specification for 10 G Ethernet applications with protection.
- IEEE 802.3ae compliant XAUI transceiver. Includes embedded IEEE 802.3ae-based XAUI link state machine.
- Compliant to FC-0 specification for 1 Gbps, 2Gbps, 10 Gbps (FC-XAUI) modes. Includes Fibre Channel link state machine.
- High-Speed Interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
- SERDES has low-power CML buffers. Support for 1.5V/1.8V I/Os. Allows use with optical transceiver, coaxial copper media, shielded twisted pair wiring or high-speed backplanes such as FR-4.
- Power down option of SERDES HSI receiver or transmitter on a per-channel basis.
- Automatic lock to reference clock in the absence of valid receive data.
- High-speed and low-speed loopback test modes.
- Requires no external component for clock recovery and frequency synthesis.
- SERDES characterization pins available to control/monitor the internal interface to one SERDES block (ORT82G5 only).
- SERDES HSI automatically recovers from loss-of-clock once its reference clock returns to normal operating state.
- Built-in boundary scan (IEEE ® 1149.1 and 1149.2 JTAG) for the programmable I/Os, not including the SERDES interface.
- FIFOs can align incoming data either across all eight channels (ORT82G5 only), across one or two groups of four channels, or across two or four groups of two channels. Alignment is done either using comma characters or by using the /A/ character in XAUI mode. Optionally, the alignment FIFOs can be bypassed for asynchronous operation between channels. (Each channel includes its own clock and frame pulse or comma detect.)
- Addition of two 4K x 36 dual-port RAMs with access to the programmable logic.
- The ORT82G5 is pinout compatible to the ORCA ORSO82G5 SONET backplane driver FPSC. The ORT42G5 is pin compatible to the ORSO42G5.

Following the definitions and conventions used in defining the 8b/10b coding rules, each valid coded character has a name corresponding to its 8-bit binary value:

- Dxx.y for data characters
- Kxx.y for special characters
- xx = the 5-bit input value, base 10, for bits ABCDE
- y = the 3-bit input value, base 10, for bits FGH

An 8b/10b encoder is designed to maintain a neutral average disparity. Disparity is the difference between the number of 1s and 0s in the encoded word. Neutral disparity indicates the number of 1s and 0s are equal. Positive disparity indicates more 1s than 0s. Negative disparity indicates more 0s than 1s. The average disparity determines the DC component of the signals on the serial line. Running disparity is a record of the cumulative disparity of every encoded word, and is tracked by the encoder.

In order to maintain neutral disparity, two different codings are defined for each data value. The 8b/10b encoder in the transmit path selects between (+) and (-) encoded word based on calculated disparity of the present data to maintain neutral disparity

In the receive path, the clock and data recovery blocks retime the incoming data and 8b/10b decoders generate 8-bit data based on the received 10-bit data. A sequence of valid 8b/10b coded characters has a maximum run length of 5 bits (i.e., 5 consecutive ones or 5 consecutive zeros before a mandatory bit transition). This assures adequate transitions for robust clock recovery.

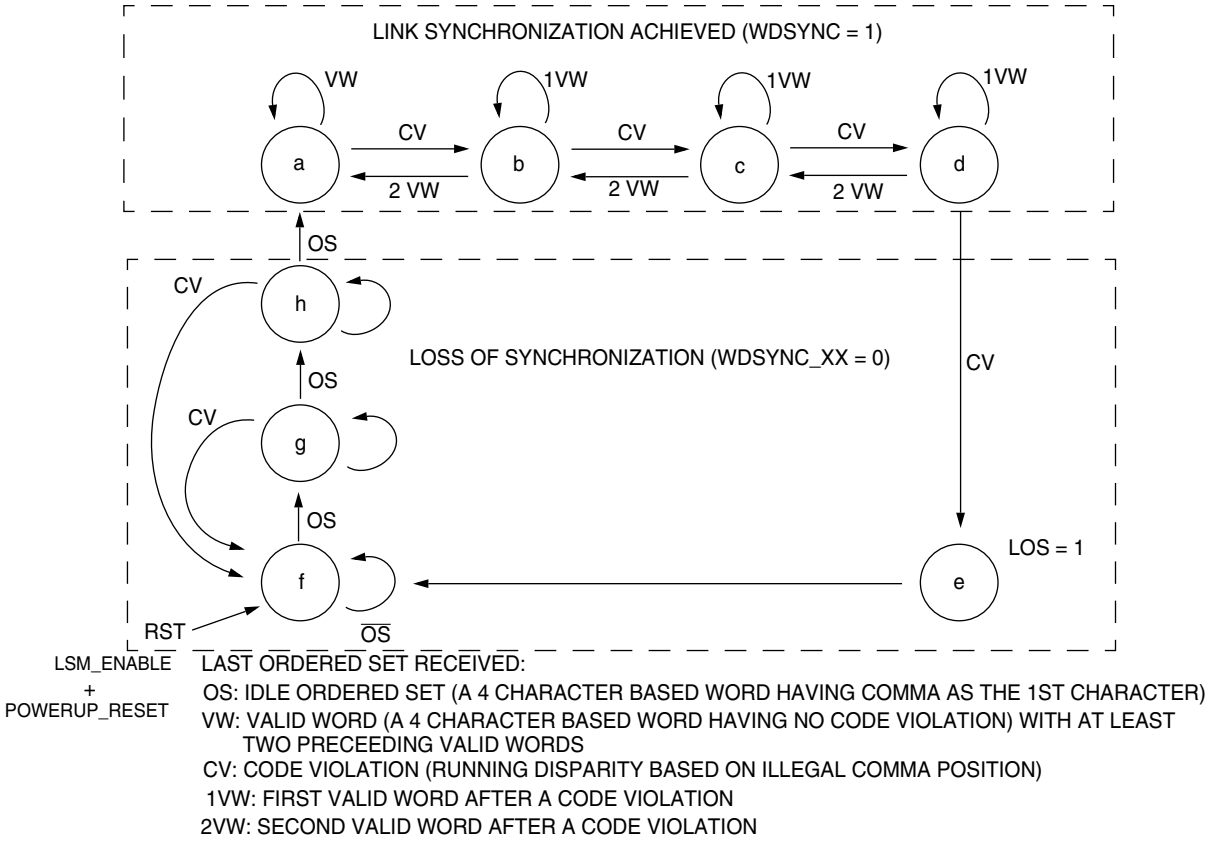
The recovered data is aligned on a 10-bit boundaries by detecting and aligning to special characters in the incoming data stream. Data is word aligned using the comma (/K/) character. A comma character is a special character that contains a unique pattern (0011111 or its complement 1100000) in the 10-bit space that makes it useful for delimiting word boundaries. The special characters K28.1, K28.5 and K28.7 contain this comma sequence and are treated as valid comma characters by the SERDES.

The following table shows all of the valid special characters. All of the special characters are made available to the FPGA logic; however only the comma characters are used by the SERDES logic. The different codings that are possible for each data value are shown as encoded word (+) and encoded word (-). The table also illustrates the 8b/10b bit labeling convention. The bit positions of the 8-bit characters are labeled as H,G,F,E,D,C,B and A and the bit positions of the 10-bit encoded characters are labeled as a, b, c, d, e, i, f, g, h, and j. The encoded words are transmitted serially with bit ‘a’ transmitted first and bit ‘j’ transmitted last.

Table 2. Valid Special Characters

K Character	HGF EDCBA 765 43210	K Control	Encoded Word (–) abcdei fghj	Encoded Word (+) abcdei fghj
K28.0	000 11100	1	001111 0100	110000 1011
K28.1 /comma/	001 11100	1	001111 1001	110000 0110
K28.2	010 11100	1	001111 0101	110000 1010
K28.3 /A/	011 11100	1	001111 0011	110000 1100
K28.4	100 11100	1	001111 0010	110000 1101
K28.5 /comma/	101 11100	1	001111 1010	110000 0101
K28.6	110 11100	1	001111 0110	110000 1001
K28.7 /comma/	111 11100	1	001111 1000	110000 0111
K23.7	111 10111	1	111010 1000	000101 0111
K27.7	111 11011	1	110110 1000	001001 0111
K29.7	111 11101	1	101110 1000	010001 0111
K30.7	111 11110	1	011110 1000	100001 0111

Figure 9. Fibre Channel Link State Machine State Diagram



XAUI Link Synchronization Function

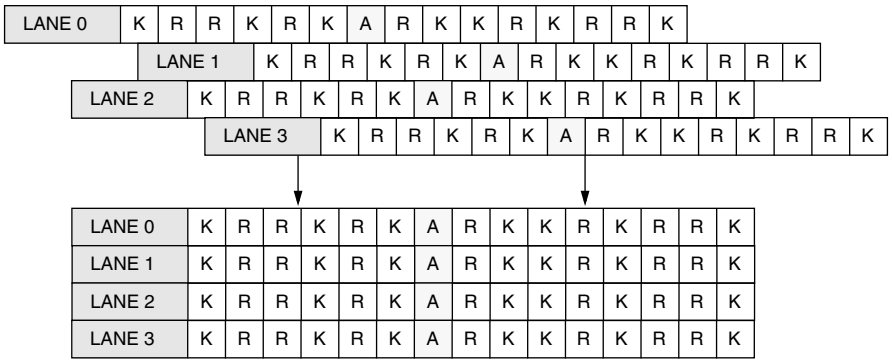
For each lane, the receive section of the XAUI link state machine incorporates a synchronization state machine that monitors the status of the 10-bit alignment. A 10-bit alignment is done in the SERDES based on a comma character such as K28.5. A comma (0011111 or its complement 1100000) is a unique pattern in the 10-bit space that cannot appear across the boundary between any two valid 10-bit code-groups. This property makes the comma useful for delimiting code-groups in a serial stream.This mechanism incorporates a hysteresis to prevent false synchronization and loss of synchronization due to infrequent bit errors. For each lane, the sync_complete signal is disabled until the lane achieves synchronization. The synchronization state diagram is shown in Figure 10. This state machine is modeled after draft *IEEE* 802.3ae, version 2.1 but will also operate with version 4.1 implementations. Table 4 and Table 5 describe the state variables used in Figure 10. The XAUI state machine does not have any control over the SERDES byte aligner. It is the user's responsibility to control the byte aligner through software access of register map addresses 30800 and 30900.

Note that it takes four idle ordered sets (e.g. K28.5, Dxx.y, Dxx.y, Dxx.y) to bring the state machine from a loss_of_sync to a synch_acq'd_1 state. When back-to-back commas are used instead, it takes a total of five commas to achieve the same result as with idle ordered sets.

Table 4. XAUI Link Synchronization State Diagram – Functions

Function	Description
sync_complete	Indication that alignment code-group alignment has been established at the boundary indicated by the most recently received comma.
cg_comma	Indication that a valid code-group, with correct running disparity, containing a comma has been received.
cg_good	Indication that a valid code-group with the correct running disparity has been received.
cg_bad	Indication that an invalid code-group has been received.
no_comma	Indication that comma timer has expired. The timer is initialized upon receipt of a comma.

Figure 16. Deskew Lanes by Aligning /A/ Columns



Mixing Half-rate, Full-rate Modes

When channel alignment is enabled, all receive channels within an alignment group should be configured at the same rate. For example, in the ORT82G5 channels AA, AB, can be configured for twin alignment and full-rate mode, while channels AC, AD that form an alignment group can be configured for half-rate mode. In block alignment mode, each receive block can be configured in either half or full-rate mode.

When channel alignment is disabled within a block, any receive channel within the block can be used in half-rate or full-rate mode. The clocking strategy for half-rate mode in both scenarios (channel alignment enabled or disabled) is described in the Reference Clocks and Internal Clock Distribution sections later in this data sheet.

Multi-channel Alignment Configuration

ORT42G5 Configuration

At startup, the legacy SERDES channel logic must be powered down and removed from any multi-channel alignment groups:

- Setting bit 1 to one in registers at locations 30002, 30012, 30102, 30112, 30003, 30013, 30103 and 30113 powers down the legacy logic. (Note that the reset value for these bits is 0.)
- Setting bits 4 and 5 to zero (reset condition) in the register at locations 30810 and 30910 removes the legacy logic from any alignment group.

Register settings for multi-channel alignment are shown in Table 6.

Table 6. Multichannel Alignment Modes

Register Bits FMPU_SYNMODE_[A:B][0:7]	Mode
00000000	No multichannel alignment.
00001010	Twin channel alignment.
00001111	Four channel alignment.

To align two channels in SERDES A:

- FMPU_SYNMODE_A = 00001010 (Register Location 30811)

To align two channels in SERDES B:

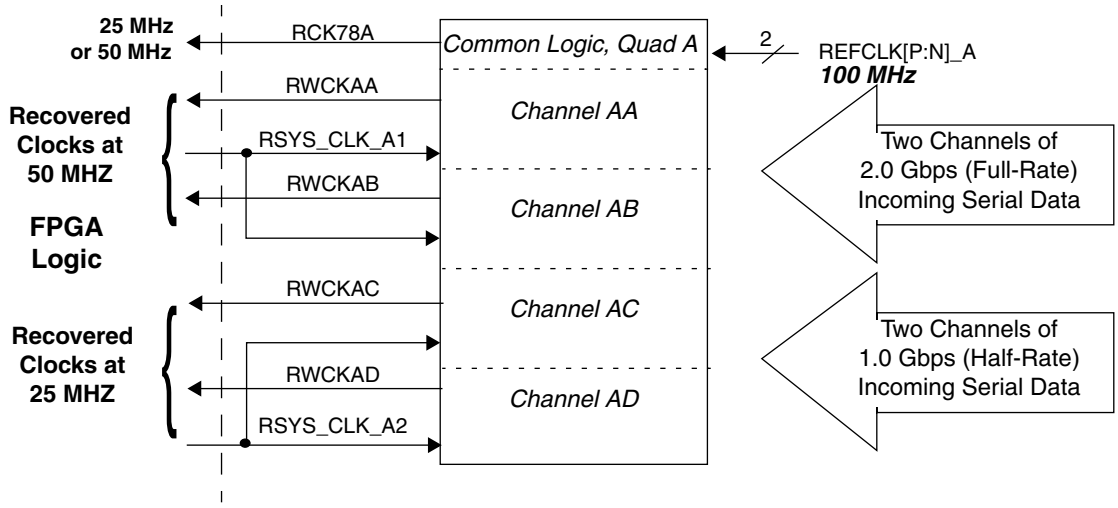
- FMPU_SYNMODE_B = 00001010 (Register Location 30911)

To align all four channels:

- FMPU_SYNMODE_A = 00001111 (Register Location 30811)

The receive channel alignment bypass mode allows mixing of half and full line rates among the channels, as shown in Figure 28. The figure shows channel pair AA and AB configured in full rate mode at 2.0 Gbps. Channel pair AC and AD are configured in half-rate mode at 1.0 Gbps.

Figure 28. Receive Clocking for Mixed Line Rates



As noted in the caption of Figure 28, each quad can be configured in any line rate (0.6 to 3.7 Gbps), since each quad has its own reference clock input pins. The receive alignment FIFO per channel cannot be used in this mode.

Multi-Channel Alignment Clocking Strategies for the ORT82G5

The data on the eight channels (four per SERDES quad) in the ORT82G5 can be independent of each other or can be synchronized in several ways. For example, two channels within a SERDES can be aligned together; channel A and B and/or channel C and D. Alternatively, all four channels in a SERDES quad can be aligned together to form a communication channel with a bandwidth of 10 Gbps. Finally, the alignment can be extended across both SERDES quads to align all eight channels. Individual channels within an alignment group can be disabled (i.e., powered down) without disrupting other channels. Clocking strategies for these various modes are described in the following paragraphs.

For dual alignment both twins within a quad can be sourced by clocks that are different from the other channels, however each pair of SERDES must have the same clock. The channel pair AA and AB is driven on the low speed side by RSYS_CLK_A1 and the channel pair AC and AD are driven on the low speed side by RSYS_CLK_A2. Either RWCKAA or RWCKAB can be connected to RSYS_CLK_A1 and either RWCKAC or RWCKAD can be connected to RSYS_CLK_A2. A clocking example for dual alignment is shown in Figure 29.

Start Up Sequence for the ORT42G5

The following sequence is required by the ORT42G5 device. For information required for simulation that may be different than this sequence, see the ORT42G5 Design Kit.

1. Initiate a hardware reset by making PASB_RESETN low. Keep this low during FPGA configuration of the device. The device will be ready for operation 3 ms after the low to high transition of PASB_RESETN.

2. At startup, the legacy SERDES channel logic must be powered down and removed from any multi-channel alignment groups:

   - Setting bit 1 to one in registers at locations 30002, 30012, 30102, 30112, 30003, 30013, 30103 and 30113 powers down the legacy logic. (Note that the reset value for these bits is 0.)
   - Setting bits 4 and 5 to zero (reset condition) in the register at locations 30810 and 30910 removes the legacy logic from any alignment group.

3. Configure the following SERDES internal and external registers. Note that after device initialization, all alarm and status bits should be read once to clear them. A subsequent read will provide the valid state.

   Set the following bits in register 30800:
   – Bits LCKREFN_[AC and AD] to 1, which implies lock to data.
   – Bits ENBYSYNC_[AC and AD] to 1 which enables dynamic alignment to comma.

   Set the following bits in register 30801:
   – Bits LOOPENB_[AC and AD] to 1 if high-speed serial loopback is desired.

   Set the following bits in register 30900:
   – Bits LCKREFN_[BC and BD] to 1 which implies lock to data.
   – Bits ENBYSYNC_[BC and BD] to 1 which enables dynamic alignment to comma.

   Set the following bits in register 30901:
   – Bits LOOPENB_[BC and BD] to 1 if high-speed serial loopback is desired.

   Set the following bits in registers 30022, 30032, 30122, 30132:
   – TXHR set to 1 if TX half-rate is desired.
   – 8b10bT set to 1 if 8b10b encoding is desired.

   Set the following bits in registers 30023, 30033, 30123, 30133:
   – RXHR Set to 1 if RX half-rate is desired.
   – 8b10bR set to 1 if 8b10b decoding is desired.
   – LINKSM set to 1 if the Fibre Channel state machine is desired.

   Assert GSWRST bit by writing 1's to both SERDES blocks. Deassert GSWRST bit by writing 0's to both SERDES blocks. Wait 3 ms. If higher speed serial loopback has been selected, the receive PLLs will use this time to lock to the new serial data.

   Monitor the following alarm bits in registers 30020, 30030, 30120, 30130:
   – LKI, PLL lock indicator. 1 indicates that PLL has achieved lock.

4. If 8b/10b mode is enabled, enable link synchronization by periodically sending the following sequence three times:
   – K28.5 D21.4 D21.5 D21.5 or any other idle ordered set (starting with a /comma/) in FC mode.
   – /comma/ characters for the XAUI state machine and /A/ characters for word and channel alignment in XAUI mode.

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Common Transmit and Receive Channel Configuration Registers (Read/Write), xx = [AC, AD, BC or BD]				
30024 - AC 30034 - AD 30124 - BC 30134 - BD	[0]	Reserved	See Bit Desc.	Reserved, must be 0. Set to 0 on device reset.
	[1]	MASK_xx		Transmit and Receive Alarm Mask Bit, Channel xx. When MASK_xx = 1, the transmit and receive alarms of a channel are prevented from generating an interrupt (i.e., they are masked or disabled). The MASK_xx bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK_xx = 1 on device reset.
	[2]	SWRST_xx		Transmit and Receive Software Reset Bit, Channel xx. When SWRST_ss = 1, this bit provides the same function as the hardware reset, except that all configuration register settings are unaltered. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. SWRST = 0 on device reset.
	[3:6]	Not used		Not used
	[7]	TESTEN_xx		Transmit and Receive Test Enable Bit, Channel xx. When TESTEN_xx = 1, the transmit and receive sections are placed in test mode. The TestMode_[A:B][4:0] bits in the Global Control Registers specify the particular test, and must also be set. Note: When the global test enable bit GTESTEN_[A:B] = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN_[A:B] = 1, all channels in a block are set to test mode regardless of their TESTEN setting. TESTEN_xx = 0 on device reset.
SERDES Global Control Registers (Read Write) - Act on Both Channels in SERDES Block A or SERDES Block B.				
30005 - A 30105 - B	[0]	Reserved	See Bit Desc.	Reserved, must be 0. Set to 0 on device reset.
	[1]	GMASK_[A:B]		Global Mask. When GMASK_[A:B] = 1, the transmit and receive alarms of both channels in the SERDES block are prevented from generating an interrupt (i.e., they are masked or disabled). The GMASK_[A:B] bit overrides the individual MASK_xx bits. GMASK_[A:B] = 1 on device reset.
	[2]	GSWRST_[A:B]		Software reset bit. The GSWRST_[A:B] bit provides the same function as the hardware reset for the transmit and receive sections of both channels, except that the device configuration settings are not affected when GSWRST_[A:B] is asserted. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. The GSWRST_[A:B] bit overrides the individual SWRST_xx bits. GSWRST_[A:B] = 0 on device reset.
	[3]	GPWRDNT_[A:B]		Powerdown Transmit Function. When GPWRDNT_[A:B] = 1, sections of the transmit hardware for both channels are powered down to conserve power. The GPWRDNT_[A:B] bit overrides the individual PWRDNT_xx bits. GPWRDNT_[A:B] = 0 on device reset.
	[4]	GPWRDNR_[A:B]		Powerdown Receive Function. When GPWRDNR_[A:B] = 1, sections of the receive hardware for both channels are powered down to conserve power. The GPWRDNR_[A:B] bit overrides the individual PWRDNR_xx bits. GPWRDNR_[A:B] = 0 on device reset.
	[5]	Reserved		Reserved, 1 on device reset.
	[6]	Not used		Not used
	[7]	GTESTEN_[A:B]		Test Enable Control. When GTESTEN_[A:B] = 1, the transmit and receive sections of both channels are placed in test mode. The GTESTEN_[A:B] bit overrides the individual TESTEN_xx bits. GTESTEN_[A:B] = 0 on device reset.
30006 - A 30106 - B	[0:4]	TestMode[A:B]	00	Test Mode - See Test Mode section for settings
	[5]	Not used		Not used
	[6:7]	Reserved		Reserved

Table 30. ORT82G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Global Control Registers (Read Write) Act on all Four Channels in SERDES Quad A or SERDES Quad B.				
30005 - A 30105 - B	[0]	Reserved	See bit descrip.	Reserved, must be set to 0. Set to 0 on device reset.
	[1]	GMASK_[A:B]		Global Mask. When GMASK_[A:B] = 1, the transmit and receive alarms of all channels in the SERDES quad are prevented from generating an interrupt (i.e., they are masked or disabled). The GMASK_[A:B] bit overrides the individual MASK_xx bits. GMASK_[A:B] = 1 on device reset.
	[2]	GSWRST_[A:B]		Software reset bit. The GSWRST_[A:B] bit provides the same function as the hardware reset for the transmit and receive sections of all four channels, except that the device configuration settings are not affected when GSWRST_[A:B] is asserted. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. The GSWRST_[A:B] bit overrides the individual SWRST_xx bits. GSWRST_[A:B] = 0 on device reset.
	[3]	GPWRDNT_[A:B]		Powerdown Transmit Function. When GPWRDNT_[A:B] = 1, sections of the transmit hardware for all four channels of are powered down to conserve power. The GPWRDNT_[A:B] bit overrides the individual PWRDNT_xx bits. GPWRDNT_[A:B] = 0 on device reset.
	[4]	GPWRDNR_[A:B]		Powerdown Receive Function. When GPWRDNR_[A:B] = 1, sections of the receive hardware for all four channels are powered down to conserve power. The GPWRDNR_[A:B] bit overrides the individual PWRDNR_xx bits. GPWRDNR_[A:B] = 0 on device reset.
	[5]	Reserved		Reserved, 1 on device reset.
	[6]	Not used		Not used. 0 on reset.
	[7]	GTESTEN_[A:B]		Test Enable Control. When GTESTEN_[A:B] = 1, the transmit and receive sections of all four channels are placed in test mode. The GTESTEN_[A:B] bit overrides the individual TESTEN_xx bits. GTESTEN_[A:B] = 0 on device reset.
30006 - A 30106 - B	[0:4]	TestMode[A:B]	00	TestMode - See Test Mode section for settings
	[5]	Not used		Not used
	[6:7]	Reserved		Reserved
Control Registers (Read/Write), xx=[AA,...,BD]				
30800 - Ax 30900 - Bx	[0]xA [1]xB [2]xC [3]xD	ENBYSYNC_xx	00	ENBYSYNC_xx = 1 Enables Receiver Byte Synchronization for Channel xx. ENBYSYNC_xx = 0 on device reset.
	[4]xA [5]xB [6]xC [7]xD	LCKREFN_xx		LCKREFN_xx = 0 Locks the receiver PLL to ref reference clock for Channel xx. LCKREFN_xx =1 = Locks the receiver to data for Channel xx. NOTE: When LCKREFN_xx = 0, the corresponding LKI_xx bit is also 0. LCKREFN_xx = 0 on device reset.
30801 - Ax 30901 - Bx	[0]xA [1]xB [2]xC [3]xD	LOOPENB_xx		Enable Loopback Mode for Channel xx. When LOOPEN_xx=1, the transmitter high-speed output is looped back to the receiver high-speed input. This mode is similar to high-speed loopback mode enabled by TESTMODE_xx except that LOOPEN_xx disables the high-speed serial output. LOOPEN_xx=0 on device reset.
	[4]xA [5]xB [6]xC [7]xD	NOWDALIGN_xx		Word Align Disable Bit. When NOWDALIGN_xx=1, receiver word alignment is disabled for Channel xx. NOWDALIGN_xx=0 on device reset.

Table 30. ORT82G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30810 - Ax 30910 - Bx	[0]xA [1]xB [2]xC [3]xD	DOWDALIGN_xx	00	Word Realign Bit. When DOWDALIGN_xx transitions from 0 to 1, the receiver realigns on the next comma character for Channel xx. NOWDALIGN_xx=0 on device reset.
	[4]xA [5]xB [6]xC [7]xD	FMPU_STR_EN_xx		Enable multi-channel alignment for Channel xx. When FMPU_STR_EN_xx=1, the corresponding channel participates in multi-channel alignment. FMPU_STR_EN_xx=0 on device reset.
30811 - Ax 30911 - Bx	[0:1] xA [2:3] xB [4:5] xC [6:7] xD	FMPU_SYNMODE_xx[0:1]	00	Sync mode for xx 00 = No channel alignment 10 = Twin channel alignment 01 = Quad channel alignment 11 = Eight channel alignment
30820 - Ax 30920 - Bx	[0]xA [1]xB [2]xC [3]xD	FMPU_RESYNC1_xx	00	Resync a Single Channel. When FMPU_RESYNC1_xx transitions from 0 to 1, the corresponding channel is resynchronized (the write and read pointers are reset). FMPU_STR_EN_xx=0 on device reset.
	[4] xA & xB [5] xC & xD	FMPU_RESYNC2_x[1:2]		Resync a Pair of Channels. When FMPU_RESYNC2_[A:B][1:2] transitions from a 0 to a 1, the corresponding channel pair is resynchronized. FFMPU_RESYNC2_[A:B][1:2]=0 on device reset.
	[6]	FMPU_RESYNC4[A:B]		Resync a Four-Channel Group. When FMPU_RESYNC4[A:B] transitions from a 0 to a 1, the corresponding four-channel group is resynchronized. FMPU_RESYNC4[A:B]=0 on device reset.
	[7]	XAUI_MODE[A:B]		Controls use of XAUI link state machine in place of Fibre-Channel state machine. When XAUI_MODE[A:B]=1, all four channels in the SERDES quad enable their XAUI link state machines. (LINKSM_xx bits are ignored). XAUI_MODE[A:B]=0 on device reset.
30821 - A 30921 - B	[0]	NOCHALGN [A:B]	00	Bypass channel alignment. NOCHALGN [A:B] =1 causes bypassing of multi-channel alignment FIFOs for the corresponding SERDES quad. NOCHALGN [A:B] =0 on device reset.
	[1:7]	Reserved for future use.		
30933	[0:3]	Reserved for future use.		
	[4:5]	SCHAR_CHAN[0:1]	00	Select channel to test 00 = Channel BA 10 = Channel BB 01 =Channel BC 11 = Channel BD
	[6]	SCHAR_TXSEL		1=Select TX option 0=Select RX option
	[7]	SCHAR_ENA		1=Enable Characterization of SERDES B
Status Registers (Read Only), xx=[AA,...,BD]				
30804 - Ax 30904 - Bx	[0:1] xA [2:3] xB [4:5] xC [6:7] xD	XAUISTAT_xx[0:1]	00	XAUI Status Register. Status of XAUI link state machine for Channel xx 00 – No synchronization. 10 – Synchronization done. 11 – Not used. 01 – no_comma (see XAUI state machine) and at least one CV detected XAUISTAT_xx[0:1] = 00 on device reset.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

The ORCA Series 4 FPSCs include circuitry designed to protect the chips from damaging substrate injection currents and to prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_{STG}	– 65	150	°C
Power Supply Voltage with Respect to Ground	V_{DD33}	– 0.3	4.2	V
	V_{DDIO}	– 0.3	4.2	V
	V_{DD15}, V_{DD_ANA}, V_{DDGB}	—	2.0	V
Input Signal with Respect to Ground	V_{IN}	V_{SS} – 0.3	V_{DD}IO + 0.3	V
Signal Applied to High-impedance Output	—	V_{SS} – 0.3	V_{DD}IO + 0.3	V
Maximum Package Body (Soldering) Temperature	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage with Respect to Ground[1]	V_{DD33}	3.0	3.6	V
	V_{DD15}	1.425	1.575	V
Input Voltages	V_{IN}	V_{SS} – 0.3	V_{DDIO} + 0.3	V
Junction Temperature	T_J	– 40	125	°C
SERDES Supply Voltage	V_{DD_ANA}, V_{DDGB}	1.425	1.575	V
SERDES CML I/O Supply Voltage	V_{DDIB}, V_{DDOB}	1.425	1.89	V

1. For FPGA Recommended Operating Conditions and Electrical Characteristics, see the Recommended Operating Conditions and Electrical Characteristics tables in the ORCA Series 4 FPGA data sheet (OR4E04) and the ORCA Series 4 I/O Buffer Technical Note. FPSC Standby Currents (IDDSB15 and IDDSB33) are tested with the Embedded Core in the powered down state.

SERDES Electrical and Timing Characteristics

Table 31. Absolute Maximum Ratings

Parameter	Conditions	Max.[1]	Units
ORT82G5 Power Dissipation	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 1.25 Gbit/s	195	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 2.50 Gbit/s	210	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 3.125 Gbit/s	225	mW
	8b/10b Encoder/Decoder (per Channel)	50	mW
ORT42G5 Power Dissipation	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 1.25 Gbit/s	265	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 2.50 Gbit/s	275	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 3.125 Gbit/s	295	mW
	8b/10b Encoder/Decoder (per Channel)	50	mW

1. With all channels operating, 1.575V supply.

High Speed Data Receiver

Table 35 specifies receiver parameters measured on devices with worst case process parameters and over the full range of operation conditions.

Table 35. External Data Input Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Input Data					
Stream of Nontransitions	8b/10b encode/decode off	—	—	72	Bits
Sensitivity (differential), worst-case[1]	3.125 Gbps	80	—	—	mVp-p
Input Levels[2]	—	V_{SS} - 0.3	—	V_{DD_ANA} + 0.3	V
Internal Buffer Resistance (Each input to VDDIB)	—	40	50	60	Ω
PLL Lock Time[3]	—	—	—	Note 2	—

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., T_A = 0ºC to 85ºC, 1.425V to 1.575V supply.
2. Input level min + (input peak to peak swing)/2 ≤ common mode input voltage ≤ input level max - (input peak to peak swing)/2
3. The ORT42G5 and ORT82G5 SERDES receiver performs four levels of synchronization on the incoming serial data stream, providing first bit, then byte (character), then channel (32-bit word), and finally optional multi-channel alignment as described in TN1025. The PLL Lock Time is the time required for the CDR PLL to lock to the transitions in the incoming high-speed serial data stream. If the PLL is unable to lock to the serial data stream, it instead locks to REFCLK to stabilize the voltage-controlled oscillator (VCO), and periodically switches back to the serial data stream to again attempt synchronization.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have recently modified specifications to indicate tolerance levels for different jitter types as they relate to specific protocols (e.g XAUI, FC, Infiniband etc.). Sinusoidal jitter is considered to be a worst case jitter type. Table 36 shows receiver specifications with 10 MHz sinusoidal jitter injection. XAUI specific jitter tolerance measurements were measured in a separate experiment detailed in technical note TN1032, *SERDES Test Chip Jitter,* and are not reflected in these results.

Table 36. Receiver Sinusoidal Jitter Tolerance Specifications

Parameter	Conditions	Max.	Unit
Input Data			
Jitter Tolerance @3.125Gbps, Typical	600 mV diff eye[1]	0.75	UIP-P
Jitter Tolerance @3.125Gbps, Worst case	600 mV diff eye[1]	0.65	UIP-P
Jitter Tolerance @2.5Gbps,Typical	600 mV diff eye[1]	0.79	UIP-P
Jitter Tolerance @2.5Gbps, Worst case	600 mV diff eye[1]	0.67	UIP-P

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., T_A = 0ºC to 85ºC, 1.425V to 1.575V supply. Jitter measured with a Wavecrest SIA-3000.

Pin Descriptions

This section describes the pins found on the Series 4 FPGAs. Any pin not described in this table is a user-programmable I/O. During configuration, the user-programmable I/Os are 3-stated with an internal pull-up resistor. If any pin is not used (or not bonded to a package pin), it is also 3-stated with an internal pull-up resistor after configuration. The pin descriptions in Table and throughout this data sheet show active-low signals with an overscore. The package pinout tables that follow, show this as a signal ending with _N. For example $\overline{\text{LDC}}$ and LDC_N are equivalent.

Table 40. Pin Descriptions

Symbol	I/O	Description
Dedicated Pins		
VDD33	—	3.3V positive power supply. This power supply is used for 3.3V configuration RAMs and internal PLLs. When using PLLs, this power supply should be well isolated from all other power supplies on the board for proper operation.
VDD15	—	1.5V positive power supply for internal logic.
VDDIO	—	Positive power supply used by I/O banks.
VSS	—	Ground.
PTEMP	I	Temperature sensing diode pin. Dedicated input.
$\overline{\text{RESET}}$	I	During configuration, $\overline{\text{RESET}}$ forces the restart of configuration and a pull-up is enabled. After configuration, $\overline{\text{RESET}}$ can be used as a general FPGA input or as a direct input, which causes all PLC latches/FFs to be asynchronously set/reset.
CCLK	O	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in.
	I	In the slave or readback after configuration, CCLK is input synchronous with the data on DIN or D[7:0]. CCLK is an output for daisy-chain operation when the lead device is in master, peripheral, or system bus modes.
DONE	I	As an input, a low level on DONE delays FPGA start-up after configuration.[1]
	O	As an active-high, open-drain output, a high level on this signal indicates that configuration is complete. DONE has an optional pull-up resistor.
PRGRM	I	$\overline{\text{PRGRM}}$ is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up.
RD_CFG	I	This pin must be held high during device initialization until the $\overline{\text{INIT}}$ pin goes high. This pin always has an active pull-up. During configuration, $\overline{\text{RD\_CFG}}$ is an active-low input that activates the TS_ALL function and 3-states all of the I/O. After configuration, $\overline{\text{RD\_CFG}}$ can be selected (via a bit stream option) to activate the TS_ALL function as described above, or, if readback is enabled via a bit stream option, a high-to-low transition on $\overline{\text{RD\_CFG}}$ will initiate readback of the configuration data, including PFU output states, starting with frame address 0.
RD_DATA/TDO	O	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary-scan, TDO is test data out.
$\overline{\text{CFG\_IRQ}}$/MPI_IRQ	O	During JTAG, slave, master, and asynchronous peripheral configuration assertion on this $\overline{\text{CFG\_IRQ}}$ (active-low) indicates an error or errors for block RAM or FPSC initialization. MPI active-low interrupt request output, when the MPI is used.
LVDS_R	—	Reference resistor connection for controlled impedance termination of Series 4 FPGA LVDS inputs.
Special-Purpose Pins		
M[3:0]	I	During powerup and initialization, M0—M3 are used to select the configuration mode with their values latched on the rising edge of $\overline{\text{INIT}}$. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O.[1]
PLL_CK[0:7][TC]	I	Semi-dedicated PLL clock pins. During configuration they are 3-stated with a pull up.
	I/O	These pins are user-programmable I/O pins if not used by PLLs after configuration.
P[TBLR]CLK[1:0][TC]	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.
	I/O	After configuration these pins are user programmable I/O, if not used for clock inputs.

Table 41. FPSC Function Pin Descriptions (Continued)

Symbol	I/O	Description
HDOUTP_AB (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad A, channel B.
HDOUTN_AC	O	High-speed CML transmit data output – SERDES quad A, channel C.
HDOUTP_AC	O	High-speed CML transmit data output – SERDES quad A, channel C.
HDOUTN_AD	O	High-speed CML transmit data output – SERDES quad A, channel D.
HDOUTP_AD	O	High-speed CML transmit data output – SERDES quad A, channel D.
HDOUTN_BA (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad B, channel A.
HDOUTP_BA (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad B, channel A.
HDOUTN_BB (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad B, channel B.
HDOUTP_BB (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad B, channel B.
HDOUTN_BC	O	High-speed CML transmit data output – SERDES quad B, channel C.
HDOUTP_BC	O	High-speed CML transmit data output – SERDES quad B, channel C.
HDOUTN_BD	O	High-speed CML transmit data output – SERDES quad B, channel D.
HDOUTP_BD	O	High-speed CML transmit data output – SERDES quad B, channel D.
Power and Ground		
VDDIB_AA (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_AB (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_AC	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_AD	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_BA (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_BB (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_BC	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_BD	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDOB_AA (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_AB (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_AC	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_AD	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_BA (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_BB (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_BC	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_BD	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDGB_A	—	1.5V guard band power supply.
VDDGB_B	—	1.5V guard band power supply.
VDD_ANA	—	1.5V power supply for SERDES analog receive and transmit circuitry.

1. Should be externally connected on board to 3.3V pull-up resistor.

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
T22	-	-	I	HDINP_BC	-	HSP_2
J19	-	-	VDD_ANA	VDD_ANA	-	-
F20	-	-	VSS	VSS	-	-
K16	-	-	VDD_ANA	VDD_ANA	-	-
R20	-	-	VDDOB	VDDOB_BC	-	-
R21	-	-	O	HDOUTN_BC	-	HSN_3
G19	-	-	VSS	VSS	-	-
R22	-	-	O	HDOUTP_BC	-	HSP_3
P21	-	-	VDDOB	VDDOB_BC	-	-
H16	-	-	VSS	VSS	-	-
P22	-	-	VDDIB	VDDIB_BD	-	-
K17	-	-	VDD_ANA	VDD_ANA	-	-
N22	-	-	I	HDINN_BD	-	HSN_4
H17	-	-	VSS	VSS	-	-
N21	-	-	I	HDINP_BD	-	HSP_4
K18	-	-	VDD_ANA	VDD_ANA	-	-
H18	-	-	VSS	VSS	-	-
K19	-	-	VDD_ANA	VDD_ANA	-	-
P20	-	-	VDDOB	VDDOB_BD	-	-
M22	-	-	O	HDOUTN_BD	-	HSN_5
H19	-	-	VSS	VSS	-	-
M21	-	-	O	HDOUTP_BD	-	HSP_5
N20	-	-	VDDOB	VDDOB_BD	-	-
L16	-	-	VSS	VSS	-	-
L17	-	-	VSS	VSS	-	-
M20	-	-	VDDOB	VDDOB_AD	-	-
L22	-	-	O	HDOUTP_AD	-	HSP_6
L18	-	-	VSS	VSS	-	-
L21	-	-	O	HDOUTN_AD	-	HSN_6
L20	-	-	VDDOB	VDDOB_AD	-	-
N16	-	-	VDD_ANA	VDD_ANA	-	-
L19	-	-	VSS	VSS	-	-
N17	-	-	VDD_ANA	VDD_ANA	-	-
K22	-	-	I	HDINP_AD	-	HSP_7
M16	-	-	VSS	VSS	-	-
K21	-	-	I	HDINN_AD	-	HSN_7
N18	-	-	VDD_ANA	VDD_ANA	-	-
K20	-	-	VDDIB	VDDIB_AD	-	-
M17	-	-	VSS	VSS	-	-
J20	-	-	VDDOB	VDDOB_AC	-	-
J21	-	-	O	HDOUTP_AC	-	HSP_8
M18	-	-	VSS	VSS	-	-
J22	-	-	O	HDOUTN_AC	-	HSN_8
H20	-	-	VDDOB	VDDOB_AC	-	-

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
Y21	-	-	VSS	VSS	-	-
Y22	-	-	VSS	VSS	-	-
L13	-	-	VSS	VSS	-	-
L14	-	-	VSS	VSS	-	-
M8	-	-	VSS	VSS	-	-
M9	-	-	VSS	VSS	-	-
M10	-	-	VSS	VSS	-	-
M11	-	-	VSS	VSS	-	-
M12	-	-	VSS	VSS	-	-
M13	-	-	VSS	VSS	-	-
M14	-	-	VSS	VSS	-	-
N8	-	-	VSS	VSS	-	-
N9	-	-	VSS	VSS	-	-
N10	-	-	VSS	VSS	-	-
N11	-	-	VSS	VSS	-	-
N12	-	-	VSS	VSS	-	-
N13	-	-	VSS	VSS	-	-
N14	-	-	VSS	VSS	-	-
P7	-	-	VSS	VSS	-	-
P8	-	-	VSS	VSS	-	-
P9	-	-	VSS	VSS	-	-
P10	-	-	VSS	VSS	-	-
P11	-	-	VSS	VSS	-	-
P12	-	-	VSS	VSS	-	-
P13	-	-	VSS	VSS	-	-
P14	-	-	VSS	VSS	-	-
R7	-	-	VSS	VSS	-	-
R8	-	-	VSS	VSS	-	-
R9	-	-	VSS	VSS	-	-
R10	-	-	VSS	VSS	-	-
R11	-	-	VSS	VSS	-	-
R12	-	-	VSS	VSS	-	-
R13	-	-	VSS	VSS	-	-
R14	-	-	VSS	VSS	-	-
AA1	-	-	VSS	VSS	-	-
AA19	-	-	VSS	VSS	-	-
AA20	-	-	VSS	VSS	-	-
AA21	-	-	VSS	VSS	-	-
AA22	-	-	VSS	VSS	-	-
AB1	-	-	VSS	VSS	-	-
AB19	-	-	VSS	VSS	-	-
AB20	-	-	VSS	VSS	-	-
AB21	-	-	VSS	VSS	-	-
AB22	-	-	VSS	VSS	-	-

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AL19	5 (BC)	3	IO	PB22A	—	L11T_D0
AK18	5 (BC)	3	IO	PB22B	—	L11C_D0
P15	—	—	VSS	VSS	—	—
AP24	5 (BC)	3	IO	PB22C	—	L12T_D0
AN23	5 (BC)	3	IO	PB22D	—	L12C_D0
AP25	5 (BC)	3	IO	PB23A	—	L13T_A0
AP26	5 (BC)	3	IO	PB23B	—	L13C_A0
AL13	5 (BC)	—	VDDIO5	VDDIO5	—	—
AL20	5 (BC)	3	IO	PB23C	PBCK1T	L14T_D0
AK19	5 (BC)	3	IO	PB23D	PBCK1C	L14C_D0
AK20	5 (BC)	3	IO	PB24A	—	L15T_D0
AL21	5 (BC)	3	IO	PB24B	—	L15C_D0
P20	—	—	VSS	VSS	—	—
AN24	5 (BC)	4	IO	PB24C	—	L16T_D0
AM23	5 (BC)	4	IO	PB24D	—	L16C_D0
AN26	5 (BC)	4	IO	PB25A	—	L17T_A0
AN25	5 (BC)	4	IO	PB25B	—	L17C_A0
AL15	5 (BC)	—	VDDIO5	VDDIO5	—	—
AK21	5 (BC)	4	IO	PB25C	—	L18T_D0
AL22	5 (BC)	4	IO	PB25D	VREF_5_04	L18C_D0
AM24	5 (BC)	4	IO	PB26A	—	L19T_D0
AL23	5 (BC)	4	IO	PB26B	—	L19C_D0
P21	—	—	VSS	VSS	—	—
AP27	5 (BC)	5	IO	PB26C	—	L20T_A0
AN27	5 (BC)	5	IO	PB26D	VREF_5_05	L20C_A0
AL24	5 (BC)	5	IO	PB27A	—	L21T_D0
AM25	5 (BC)	5	IO	PB27B	—	L21C_D0
AN13	5 (BC)	—	VDDIO5	VDDIO5	—	—
AP28	5 (BC)	5	IO	PB27C	—	L22T_A0
AP29	5 (BC)	5	IO	PB27D	—	L22C_A0
AN29	5 (BC)	6	IO	PB28B	—	—
P22	—	—	VSS	VSS	—	—
AM27	5 (BC)	6	IO	PB28C	—	L23T_D0
AN28	5 (BC)	6	IO	PB28D	VREF_5_06	L23C_D0
AM26	5 (BC)	6	IO	PB29B	—	—
AK22	5 (BC)	6	IO	PB29C	—	L24T_A0
AK23	5 (BC)	6	IO	PB29D	—	L24C_A0
AL25	5 (BC)	7	IO	PB30B	—	—
R13	—	—	VSS	VSS	—	—
AP30	5 (BC)	7	IO	PB30C	—	L25T_A0
AP31	5 (BC)	7	IO	PB30D	—	L25C_A0
AK24	5 (BC)	7	IO	PB31B	—	—
AN15	5 (BC)	—	VDDIO5	VDDIO5	—	—
AM29	5 (BC)	7	IO	PB31C	VREF_5_07	L26T_A0

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AM28	5 (BC)	7	IO	PB31D	—	L26C_A0
AN30	5 (BC)	7	IO	PB32B	—	—
R14	—	—	VSS	VSS	—	—
AK25	5 (BC)	7	IO	PB32C	—	L27T_D0
AL26	5 (BC)	7	IO	PB32D	—	L27C_D0
AN17	5 (BC)	—	VDDIO5	VDDIO5	—	—
AL27	5 (BC)	8	IO	PB33C	—	L28T_A0
AL28	5 (BC)	8	IO	PB33D	VREF_5_08	L28C_A0
AN31	5 (BC)	8	IO	PB34B	—	—
R15	—	—	VSS	VSS	—	—
AK26	5 (BC)	8	IO	PB34D	—	—
AM30	5 (BC)	9	IO	PB35B	—	—
AL29	5 (BC)	9	IO	PB35D	VREF_5_09	—
AK27	5 (BC)	9	IO	PB36B	—	—
R20	—	—	VSS	VSS	—	—
AL30	5 (BC)	9	IO	PB36C	—	L29T_D0
AK29	5 (BC)	9	IO	PB36D	—	L29C_D0
AK28	—	—	VDD33	VDD33	—	—
AA16	—	—	VDD15	VDD15	—	—
AP32	—	—	IO	PSCHAR_LDIO9	—	—
AP33	—	—	IO	PSCHAR_LDIO8	—	—
AN32	—	—	IO	PSCHAR_LDIO7	—	—
AM31	—	—	IO	PSCHAR_LDIO6	—	—
AA17	—	—	VDD15	VDD15	—	—
AM32	—	—	VDD33	VDD33	—	—
AL31	—	—	IO	PSCHAR_LDIO5	—	—
AM33	—	—	IO	PSCHAR_LDIO4	—	—
AA18	—	—	VDD15	VDD15	—	—
AK30	—	—	IO	PSCHAR_LDIO3	—	—
AL32	—	—	IO	PSCHAR_LDIO2	—	—
AA19	—	—	VDD15	VDD15	—	—
AB16	—	—	VDD15	VDD15	—	—
AK31	—	—	VDD33	VDD33	—	—
AJ30	—	—	IO	PSCHAR_LDIO1	—	—
AK33	—	—	IO	PSCHAR_LDIO0	—	—
AK34	—	—	IO	PSCHAR_CKIO1	—	—
AJ31	—	—	IO	PSCHAR_CKIO0	—	—
AJ33	—	—	IO	PSCHAR_XCK	—	—
AJ34	—	—	IO	PSCHAR_WDSYNC	—	—
AH30	—	—	IO	PSCHAR_CV	—	—
AH31	—	—	IO	PSCHAR_BYTSYNC	—	—
AH32	—	—	O	ATMOUT_B (no connect)	—	—
AH33	—	—	VSS	VSS	—	—
AH34	—	—	VDDGB_B	VDDGB_B	—	—

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
B24	1 (TC)	3	IO	PT23B	—	—
D20	1 (TC)	3	IO	PT22D	—	L15C_A0
D19	1 (TC)	3	IO	PT22C	—	L15T_A0
N14	—	—	Vss	Vss	—	—
E19	1 (TC)	3	IO	PT22B	—	L16C_A0
E18	1 (TC)	3	IO	PT22A	—	L16T_A0
C21	1 (TC)	4	IO	PT21D	—	L17C_A0
C20	1 (TC)	4	IO	PT21C	—	L17T_A0
A25	1 (TC)	4	IO	PT21B	—	L18C_A0
A24	1 (TC)	4	IO	PT21A	—	L18T_A0
B23	1 (TC)	4	IO	PT20D	—	L19C_A0
A23	1 (TC)	4	IO	PT20C	—	L19T_A0
N15	—	—	Vss	Vss	—	—
E17	1 (TC)	4	IO	PT20B	—	L20C_A0
E16	1 (TC)	4	IO	PT20A	—	L20T_A0
B22	1 (TC)	4	IO	PT19D	—	L21C_A0
B21	1 (TC)	4	IO	PT19C	VREF_1_04	L21T_A0
C18	1 (TC)	4	IO	PT19B	—	L22C_A0
C19	1 (TC)	4	IO	PT19A	—	L22T_A0
N20	—	—	Vss	Vss	—	—
A22	1 (TC)	5	IO	PT18D	PTCK1C	L23C_A0
A21	1 (TC)	5	IO	PT18C	PTCK1T	L23T_A0
N21	—	—	Vss	Vss	—	—
D17	1 (TC)	5	IO	PT18B	—	L24C_A0
D18	1 (TC)	5	IO	PT18A	—	L24T_A0
B20	1 (TC)	5	IO	PT17D	PTCK0C	L25C_A0
B19	1 (TC)	5	IO	PT17C	PTCK0T	L25T_A0
A20	1 (TC)	5	IO	PT17B	—	L26C_A0
A19	1 (TC)	5	IO	PT17A	—	L26T_A0
A18	1 (TC)	5	IO	PT16D	VREF_1_05	L27C_A0
B18	1 (TC)	5	IO	PT16C	—	L27T_A0
Y21	—	—	Vss	Vss	—	—
C17	1 (TC)	5	IO	PT16B	—	L28C_D0
D16	1 (TC)	5	IO	PT16A	—	L28T_D0
A17	1 (TC)	6	IO	PT15D	—	L29C_D0
B16	1 (TC)	6	IO	PT15C	—	L29T_D0
E15	1 (TC)	6	IO	PT15B	—	L30C_A0
E14	1 (TC)	6	IO	PT15A	—	L30T_A0
A16	1 (TC)	6	IO	PT14D	—	L31C_A0
A15	1 (TC)	6	IO	PT14C	VREF_1_06	L31T_A0
Y22	—	—	Vss	Vss	—	—
D14	1 (TC)	6	IO	PT14B	—	—
C16	0 (TL)	1	IO	PT13D	MPI_RTRY_N	L1C_A0
C15	0 (TL)	1	IO	PT13C	MPI_ACK_N	L1T_A0

where T_C is the case temperature at top dead center, T_J is the junction temperature, and Q is the chip power. During the Θ_{JA} measurements described above, besides the other parameters measured, an additional temperature reading, T_C, is made with a thermocouple attached at top-dead-center of the case. ψ_{JC} is also expressed in units of °C/W.

Θ_{JC}

This is the thermal resistance from junction to case. It is most often used when attaching a heat sink to the top of the package. It is defined by:

$$\Theta_{JC} = \frac{T_J - T_C}{Q} \quad (3)$$

The parameters in this equation have been defined above. However, the measurements are performed with the case of the part pressed against a water-cooled heat sink to draw most of the heat generated by the chip out the top of the package. It is this difference in the measurement process that differentiates Θ_{JC} from ψ_{JC}. Θ_{JC} is a true thermal resistance and is expressed in units of °C/W.

Θ_{JB}

This is the thermal resistance from junction to board. It is defined by:

$$\Theta_{JB} = \frac{T_J - T_B}{Q} \quad (4)$$

where T_B is the temperature of the board adjacent to a lead measured with a thermocouple. The other parameters on the right-hand side have been defined above. This is considered a true thermal resistance, and the measurement is made with a water-cooled heat sink pressed against the board to draw most of the heat out of the leads. Note that Θ_{JB} is expressed in units of °C/W and that this parameter and the way it is measured are still being discussed by the JEDEC committee.

FPSC Maximum Junction Temperature

Once the power dissipated by the FPSC has been determined, the maximum junction temperature of the FPSC can be found. This is needed to determine if speed derating of the device from the 85 °C junction temperature used in all of the delay tables is needed. Using the maximum ambient temperature, T_{Amax}, and the power dissipated by the device, Q (expressed in °C), the maximum junction temperature is approximated by:

$$T_{Jmax} = T_{Amax} + (Q \cdot \Theta_{JB}) \quad (5)$$

Package Thermal Characteristics

The thermal characteristics of the 484-ball PBGAM (fpBGA with heat spreader) used for the ORT42G5, the 680-ball PBGAM (fpBGA with heat spreader) and the 680-ball fpBGA used for the ORT82G5 are available in the Thermal Management section of the Lattice web site at www.latticesemi.com.

Heat Sink Vendors for BGA Packages

The estimated worst-case power requirements for the ORT42G5 and ORT82G5 are in the 3 W to 5 W range. Consequently, for most applications an external heat sink will be required. Table 46 lists, in alphabetical order, heat sink vendors who advertise heat sinks aimed at the BGA market.

Industrial[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT42G5	ORT42G5-2BM484I	2	PBGAM	484	I
	ORT42G5-1BM484I	1	PBGAM	484	I
ORT82G5	ORT82G5-2F680I	2	PBGAM (No Heat Spreader)	680	I
	ORT82G5-1F680I	1	PBGAM (No Heat Spreader)	680	I
	ORT82G5-2BM680I[2]	2	PBGAM (With Heat Spreader)	680	I
	ORT82G5-1BM680I[2]	1	PBGAM (With Heat Spreader)	680	I

1. For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only.
2. BM680 package was converted to F680 via PCN#09A-08.

Lead-Free Packaging

Commercial[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT42G5	ORT42G5-3BMN484C	3	Lead-Free PBGAM	484	C
	ORT42G5-2BMN484C	2	Lead-Free PBGAM	484	C
	ORT42G5-1BMN484C	1	Lead-Free PBGAM	484	C
ORT82G5	ORT82G5-3FN680C	3	Lead-Free FPGA (No Heat Spreader)[2]	680	C
	ORT82G5-2FN680C	2	Lead-Free FPGA (No Heat Spreader)[2]	680	C
	ORT82G5-1FN680C	1	Lead-Free FPGA (No Heat Spreader)[2]	680	C

1. For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster.
2. Refer to the Thermal Management document at www.latticesemi.com for Θ_{JA} and Θ_{JC} information.

Industrial[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT42G5	ORT42G5-2BMN484I	2	Lead-Free PBGAM	484	I
	ORT42G5-1BMN484I	1	Lead-Free PBGAM	484	I
ORT82G5	ORT82G5-2FN680I	2	Lead-Free FPGA (No Heat Spreader)[2]	680	I
	ORT82G5-1FN680I	1	Lead-Free FPGA (No Heat Spreader)[2]	680	I

1. For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster.
2. Refer to the Thermal Management document at www.latticesemi.com for Θ_{JA} and Θ_{JC} information.