Lattice Semiconductor Corporation - ORT42G5-2BM484I Datasheet

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Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	204
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort42g5-2bm484i

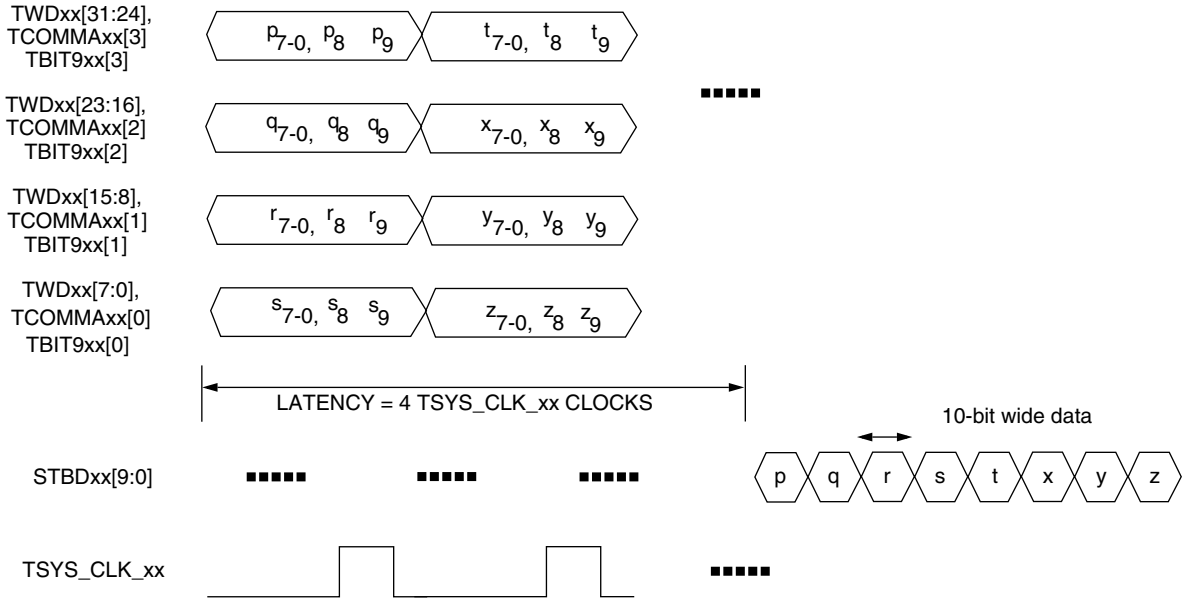
Embedded Core/FPGA Logic Interface and 4:1 Multiplexer

These blocks provide the data formatting and transmit data and clock signal transfers between the Embedded Core and the FPGA Logic. Control and status registers in the FPGA portion of the chip contain to control the transmit logic and record status. These bits are passed to the core using the FPGA System Bus and are described in later sections of this data sheet.

The low-speed transmit interface consists of a clock and 4 data bytes, each with an accompanying control bit. The data bytes are conveyed to the MUX via the TWDxx[31:0] ports (where xx represents the channel label [AA,...,BD] or [AC, AD, BC, BD]). The control bits are TCOMMAx[3:0] which define whether the input byte is to be interpreted as data or as a special character and TBIT9xx[3:0] which are used to force a negative disparity present state. The data and control signals are synchronized to the transmit clock, TSYS_CLK_xx. Both the data and control are strobed into the core on the rising edge of TSYS_CLK_xx. Note that each TBIT9xx[3:0] controls the disparity of the encoded version of its corresponding data byte. Setting bit TBIT9AC[3] to 1, for instance, will force the 8b/10b encoder to assess a current negative running disparity state. This will cause it to encode TWDAC[31:24] positively (more 1's than 0's). Setting TBIT9xx to 0 will leave the encoder free to alternate between positive and negative encoding to maintain a zero running disparity.

The MUX is responsible for taking 40 bits of data/control at the low-speed transmit interface and up-converting it to 10 bits of data/control at the SERDES transmit interface. The MUX has 2 clock domains - one based on the clock received from the SERDES block and a second that comes from the FPGA at 1/4 the frequency of the SERDES clock. The time sequence of interleaving data/control values is shown in Figure 4.

Figure 4. Transmit MUX Block Timing - Single Channel



SERDES Block

The SERDES block accepts either 8-bit data to be encoded or 10-bit unencoded data at the parallel input port from the MUX/DEMUX block. It also accepts the reference clock at the REFCLK_[A:B] input and uses this clock to synthesize the internal high-speed serial bit clock.

The internal STBC311xx clock is derived from the reference clock. The frequency of this clock depends on the setting of the half-rate/full-rate control bit setting the mode of the SERDES and the frequency of the REFCLK_[A:B] and/or that of the high-speed serial data. A falling edge on the STBC311xx clock port will cause a new data character to be transferred into the SERDES block. The latency from the SERDES block input to the high-speed serial output is 5 STBC311xx clock cycles, as shown in Figure 5.

Since this effect is predictable for a given type of PCB material, it is possible to compensate for this effect in two ways - transmitter preemphasis and receiver equalization. Each of these techniques boosts the high frequency components of the signal but transmit preemphasis is preferred due to the ease of implementation and the better power utilization. It also gives a better signal-to-noise ratio because receiver equalization amplifies both the signal and the noise at the receiver

Applying too much preemphasis when it is not required, for example when driving a short backplane path, will also degrade the data eye opening at the receiver. In the ORT42G5 and ORT82G5 the degree of transmit preemphasis can be programmed with a two-bit control from the microprocessor interface as shown in Table 3. The high-pass transfer function of the preemphasis circuit is given by the following equation, where the value of a is shown in Table 3.

$$H(z) = (1 - az^{-1}) \quad (1)$$

Table 3. Preemphasis Settings

PE1	PE0	Amount of Preemphasis (a)
0	0	0% (No Preemphasis)
0	1	12.5%
1	0	12.5%
1	1	25%

Receive Path (Backplane to FPGA) Logic

The receiver section receives high-speed serial data at the external differential CML input pins. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. Therefore the receive clocks are asynchronous between channels. The retimed data are deserialized and presented as an 8-bit decoded or a 10-bit unencoded parallel data on the output port. The receiver also optionally recognizes comma characters, detects code violations and aligns the bit stream to the proper word boundary.

As shown in Figure 6, the basic blocks in the receive path include:

Receive SERDES Block

- CML input buffer
- Receive PLL
- 1:10 demultiplexer (DEMUX)
- Clock and Data Recovery (CDR) section
- 10b/8b decoder
- 1:4 demultiplexer and Embedded Core/FPGA interface
- 1:4 DEMUX
- Low speed parallel Embedded Core/FPGA logic interface
- Multi-channel alignment logic

Bit alignment times fall into two categories: realignment when the input serial data stream experiences an abrupt phase change (as may occur when protection switching is performed between two paths having different delays), and alignment from a no-signal condition. Realignment is very quick, since the PLL's VCO is already locked on frequency and only needs to adapt to the new phase. This re-alignment has been observed to require no more than one microsecond when REFCLK[A:B] = 156.25 MHz.

Alignment from a no-signal condition has two components. First, there is the re-acquisition to the data's frequency and phase. The time required for re-acquisition to the data's frequency is minimized by logic that periodically switches the PLL to lock to the REFCLK[A:B] when it fails to lock on the serial data stream, thus limiting the VCO's frequency wander. Second, there is the time spent while the PLL is locking to REFCLK[A:B], which can be from zero to a maximum value, depending on when the serial data stream becomes valid in relation to the PLL's switching to/from REFCLK[A:B]. This alignment has been observed to require no more than 4 microseconds when REFCLK = 156.25 MHz.

Byte alignment occurs once valid bit alignment is achieved. The byte aligner looks for a particular 7-bit sequence (either 0011111 or its complement, 1100000) that, in data that has been 8b/10b encoded per Fibre Channel or IEEE 802.3ae specifications, only occurs in the comma (/K/) characters K28.1, K28.5 and K28.7. Byte alignment only occurs when the ENBYSYNC_xx signal for that channel is active high, and re-alignment occurs on each 7-bit sequence encountered. However, if ENBYSYNC_xx is asserted active high and no comma character is encountered, and then is brought inactive low, the channel will still perform one byte alignment operation on the next comma character. Byte alignment occurs immediately when an alignment sequence is detected, so the lock time is only one clock period.

Note: Each time the byte aligner performs an alignment, it also corrects the phase of the internal RBC_xx clock. This can result in the "stretching" of the clock by a half-phase in order to cause the output data to align with the rising edge of RBC_xx.

Word (32-bit) alignment can occur after the Fibre Channel (XAUI_MODE_xx = 0) or XAUI (XAUI_MODE_xx = 1) state machine has reached the in-synchronization state. In Fibre Channel mode, synchronization (WDSYNC_xx = 1) will occur after three ordered sets of data have been received in the absence of any code violations. After this, the next ordered set will cause the output data to be aligned such that the comma character is in the most significant byte. Thus, 32-bit word alignment has been achieved when four ordered sets have been detected. The time required is directly dependent on comma-character density.

Note: once word alignment is accomplished, no further alignment occurs unless and until WDSYNC_xx goes to zero and back to one again. Comma characters that are not located in the most significant byte position will not trigger further re-alignment while WDSYNC_xx is active. This behavior is as defined by the Fibre Channel specification. However, it means that, if the channel experiences an abrupt delay change (as could occur if an external MUX performs a protection switch between two links) and if the delay change is close enough to a full character or characters that not enough code violations are generated to cause loss of WDSYNC_xx, the channel could become misaligned and remain that way indefinitely. As mentioned above, this behavior is that defined by the Fibre Channel specification.

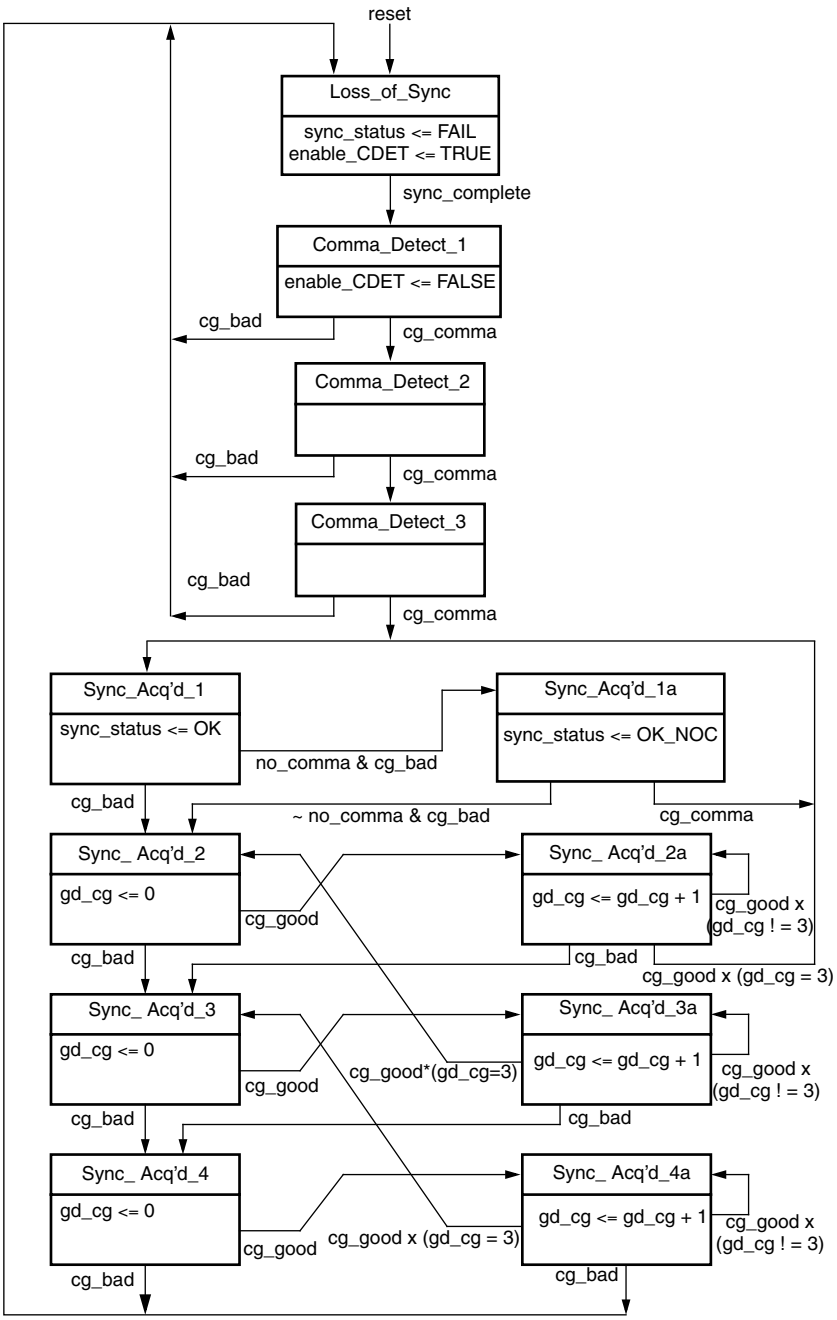
In XAUI mode, as the state diagram later in this data sheet indicates, three error-free code-groups containing commas must be detected before synchronization is declared.

Multi 2, 4 or 8 (ORT82G5 only) channel alignment (Lane alignment in XAUI mode) can be performed after 32-bit word alignment is complete. Multi-channel alignment is described in later sections of this data sheet.

Table 5. XAUI Link Synchronization State Diagram Notation – Variables

Variable	Description
sync_status	FAIL: Lane is not synchronized (correct 10-bit alignment has not been established). OK: Lane is synchronized. OK_NOC: Lane is synchronized but a comma character has not been detected in the past 200 code groups.
enable_CDET	TRUE: Align subsequent 10-bit words to the boundary indicated by the next received comma. FALSE: Maintain current 10-bit alignment.
gd_cg	Current number of consecutive cg_good indications.

Figure 10. XAUI Link Synchronization State Diagram



grammed to a value > 0. (Default value is 0.) Change the value to 0 and check the OVFL bit again.

If OOS and OVFL are 1, then rewrite a 1 to the appropriate resync registers. The resync operation requires a rising edge. Two writes are required to the resync bits: write a 0 and then write a 1.

ORT82G5 Alignment Sequence

1. Follow steps 1 and 2 in the start-up sequence described in a later section.

2. Initiate a SERDES software reset by setting the SWRST bit to 1 and then to 0. Note that any changes to the SERDES configuration bits should be followed by a software reset.

3. Wait for 3 ms. REFCLK should be toggling by this time. During this time, configure the following registers.

Set the following bits in registers 30820, 30920

- XAUI_MODE_xx-set to 1 for XAUI mode or keep the default value of 0 if the Fibre Channel state machine was selected.
- Enable channel alignment by setting FMPU_SYNMODE bits in registers 30811, 30911.
- FMPU_SYNMODE_xx. Set to appropriate values for 2, 4, or 8 alignment based on Table 7.
- Set RCLKSEL[A:B] and TCKSEL[A:B] bits in registers 30A00.
- RCKSEL[A:B] – Choose clock source for 78 MHz RCK78x (Table 18).
- TCKSEL[A:B] – Choose clock source for 78 MHz TCK78x (Table 17). Send data on serial links.

Monitor the following status/alarm bits:

- Monitor the following alarm bits in registers 30000, 30010, 30020, 30030, 30100, 30110, 30120, 30130.
- LKI-PLL_xx lock indicator. A 1 indicates that PLL has achieved lock.

Monitor the following status bits in registers 30804, 30904:

- XAUISTAT_xx - In XAUI mode, they should be 10.

Monitor the following status bits in registers 30805, 30905

- DEMUXWAS_xx-They should be 1 indicating word alignment is achieved.
- CH248_SYNCxx-They should be 1 indicating channel alignment. This is cleared by resync.

4. Write a 1 to the appropriate resync registers 30820, 30920 or 30A02. Note that this assumes that the previous value of the resync bits are 0. The resync operation requires a rising edge. Two writes are required to the resync bits: write a 0 and then write a 1. It is highly recommended to precede a resync with a word alignment, especially in situations where a disturbance in the receive SERDES path can cause misalignment of data and OOS indications without bringing the FC/XAUI state machine to a loss of synch state. A word alignment is achieved by writing a 0 and then a 1 to the appropriate DOWDALIGNxx bits in registers 30810/30910.

Check out-of-sync and FIFO overflow status in registers 30814 (Bank A).

- SYNC4_A_OOS, SYNC4_A_OVFL-by 4 alignment.
- SYNC2_A2_OOS, SYNC_A2_OVFL or SYNC2_A1_OOS, SYNC2_A1_OVFL-by 2 alignment.
- Check out-of-sync status in registers 30914 (Bank B).
- SYNC4_B_OOS, SYNC4_B_OVFL-by 4 alignment.
- SYNC_B2_OOS, SYNC2_B2_OVFL or SYNC2_B1_OOS, SYNC_B1_OVFL-by 2 alignment.
- Check out-of-sync status in register 30A03
- SYNC8_OOS, SYNC8_OVFL-by 8 alignment.
- If out-of-sync bit is 1, then rewrite a 1 to the appropriate resync registers and monitor the OOS bit again. If Out of Synchronization (OOS) bit is 0 but OVFL bit is 1, then check if the RX_FIFO_MIN value has been programmed to a value > 0. (Default value is 0.) Change the value to 0 and check the OVFL bit again. If OOS and OVFL are 1, then rewrite a 1 to the appropriate resync registers. The resync operation requires a rising edge. Two writes are required to the resync bits: write a 0 and then write a 1.

Embedded Core/FPGA Interface

This block provides the data formatting and receive data and clock signal transfers between the Embedded Core and the FPGA Logic. There are also control and status registers in the FPGA portion of the chip which contain bits to control the receive logic and to record status. These are described in later sections of this data sheet and communicate with the core using the System Bus.

The demultiplexed, receive word outputs to the FPGA are shown in Figure 6. These are each 40 bits wide. There are eight of these interfaces, one for each SERDES channel. Each consist of four groups of 10-bit data or four groups of decoded information depending on setting of 8b10bR_xx control register bits.

Each 10-bit group of decoded information includes 8 bits of data and a 1 bit K_CTRL indicator derived from the received data and a tenth bit of status information. The function of the tenth bit varies from group to group and includes code violation, Out of Synchronization (OOS) indicators and the CH24_SYNC24_xx and CH248_SYNC_xx status bits. CH24_SYNC or CH248_SYNC_xx indicates the status of multi-channel alignment of channel xx and are high when the count for the multi-channel alignment block reaches zero regardless of whether or not multi-channel alignment is successful. The mapping of the 10-bit groups to the MRWD_xx[39:0] bits output to the FPGA logic is summarized in Table 8. The various functions of the bits that vary from channel to channel, i.e., bits 29 and 19, are also described in Table 9 and Table 10.

Table 8. Definition of Bits of MRWDxx[39:0]

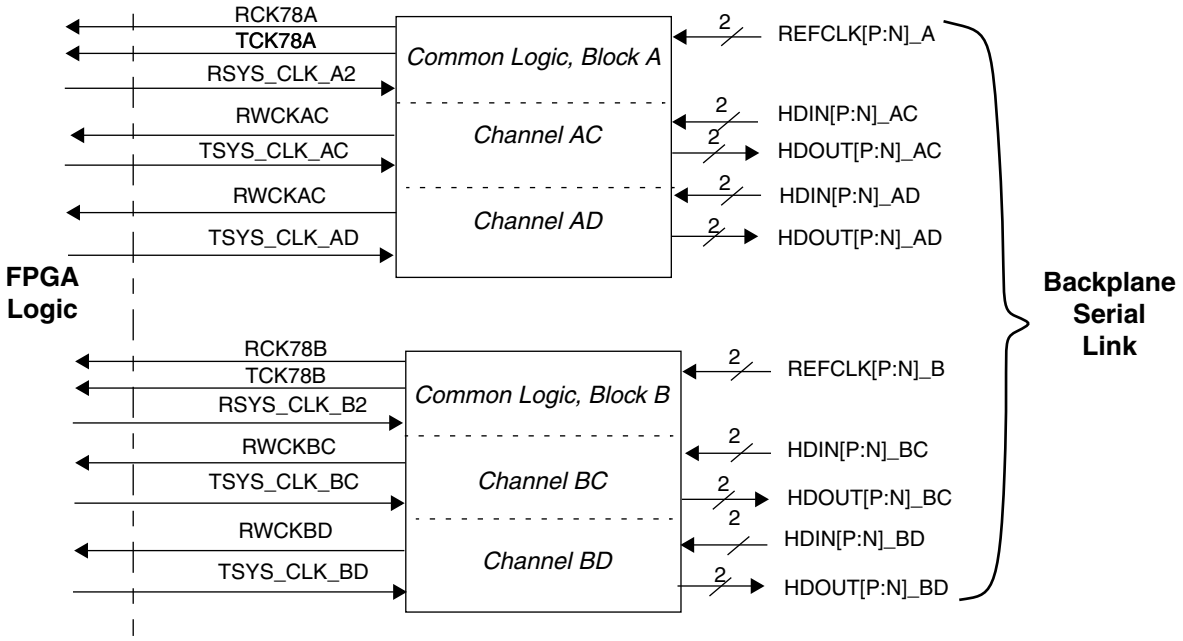
	8b10bR=0	8b10bR=1	
Bit Index	NOCHALGN[A:B]=1 CV_SELxx=0	NOCHALGN[A:B]=1 CV_SELxx=1	NOCHALGN[A:B]=0 CV_SELxx=1
39	bit 9 of 10-bit data 3	CV_xx3, code violation, byte 3	See Table 9 and Table 10
38	bit 8 of 10-bit data 3	K_CTRL for byte 3	K_CTRL for byte 3
37	bit 7 of 10-bit data 3	bit 7 of byte3	bit 7 of byte3
36	bit 6 of 10-bit data 3	bit 6 of byte 3	bit 6 of byte 3
35	bit 5 of 10-bit data 3	bit 5 of byte 3	bit 5 of byte 3
34	bit 4 of 10-bit data 3	bit 4 of byte 3	bit 4 of byte 3
33	bit 3 of 10-bit data 3	bit 3 of byte 3	bit 3 of byte 3
32	bit 2 of 10-bit data 3	bit 2 of byte 3	bit 2 of byte 3
31	bit 1of 10-bit data 3	bit 1 of byte 3	bit 1 of byte 3
30	bit 0 of 10-bit data 3	bit 0 of byte 3	bit 0 of byte 3
29	bit 9 of 10-bit data 2	CV_xx2, code violation, byte 2	See Table 9 and Table 10
28	bit 8 of 10-bit data 2	K_CTRL for byte 2	K_CTRL for byte 2
27	bit 7 of 10-bit data 2	bit 7 of byte 2	bit 7 of byte 2
26	bit 6 of 10-bit data 2	bit 6 of byte 2	bit 6 of byte 2
25	bit 5 of 10-bit data 2	bit 5 of byte 2	bit 5 of byte 2
24	bit 4 of 10-bit data 2	bit 4 of byte 2	bit 4 of byte 2
23	bit 3 of 10-bit data 2	bit 3 of byte 2	bit 3 of byte 2
22	bit 2 of 10-bit data 2	bit 2 of byte 2	bit 2 of byte 2
21	bit 1 of 10-bit data 2	bit 1 of byte 2	bit 1 of byte 2
20	bit 0 of 10-bit data 2	bit 0 of byte 2	bit 0 of byte 2
19	bit 9 of 10-bit data 1	CV_xx1, code violation, byte 1	See Table 9 and Table 10
18	bit 8 of 10-bit data 1	K_CTRL for byte 1	K_CTRL for byte 1
17	bit 7 of 10-bit data 1	bit 7 of byte 1	bit 7 of byte 1
16	bit 6 of 10-bit data 1	bit 6 of byte 1	bit 6 of byte 1
15	bit 5 of 10-bit data 1	bit 5 of byte 1	bit 5 of byte 1
14	bit 4 of 10-bit data 1	bit 4 of byte 1	bit 4 of byte 1
13	bit 3 of 10-bit data 1	bit 3 of byte 1	bit 3 of byte 1

data rate and bit-width so the FPGA core can run at 1/4th this frequency which gives a range of 15 to 92.5 MHz for the data in and out of the FPGA.

Internal Clock Signals at the FPGA/Core Interface for the ORT42G5

There are several clock signals defined at the FPGA/Embedded Core interface in addition to the external reference clock for each SERDES block. All of the ORT42G5 clock signals are shown in Figure 17 and are described following the figure.

Figure 17. ORT42G5 Clock Signals (High Speed Serial I/O Also Shown)



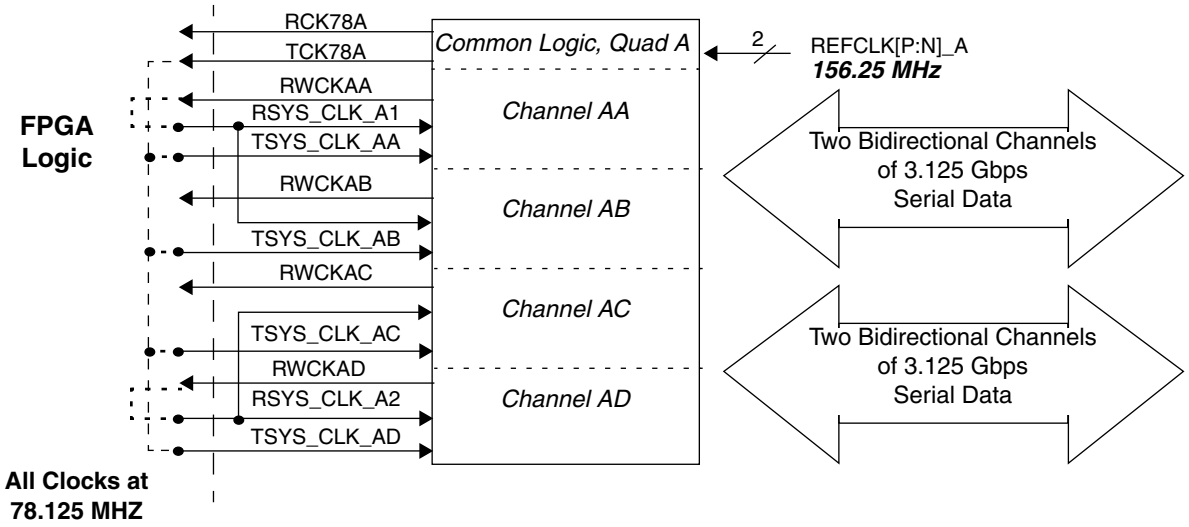
REFCLKP_[A:B], REFCLKN_[A:B]:
These are the differential reference clocks provided to the ORT42G5 device as described earlier. They are used as the reference clock for both TX and RX paths. For operation of the serial links at 3.125 Gbps, the reference clocks will be at a frequency of 156.25 MHz.

RWCK[AC, AD, BC, BD]:
These are the low-speed receive clocks from the embedded core to the FPGA across the core-FPGA interface. These are derived from the recovered low-speed complementary clocks from the SERDES blocks. RWCKAC belongs to Channel AC, RWCKBC belongs to channel BC and so on. With a reference clock input of 156.25 MHz, these clocks operate at 78.125 MHz.

RCK78[A:B]:
These are muxed outputs of RWCKA[C or D] and RWCKB[C or D] respectively. With a reference clock input of 156.25 MHz, these clocks operate at 78.125 MHz.

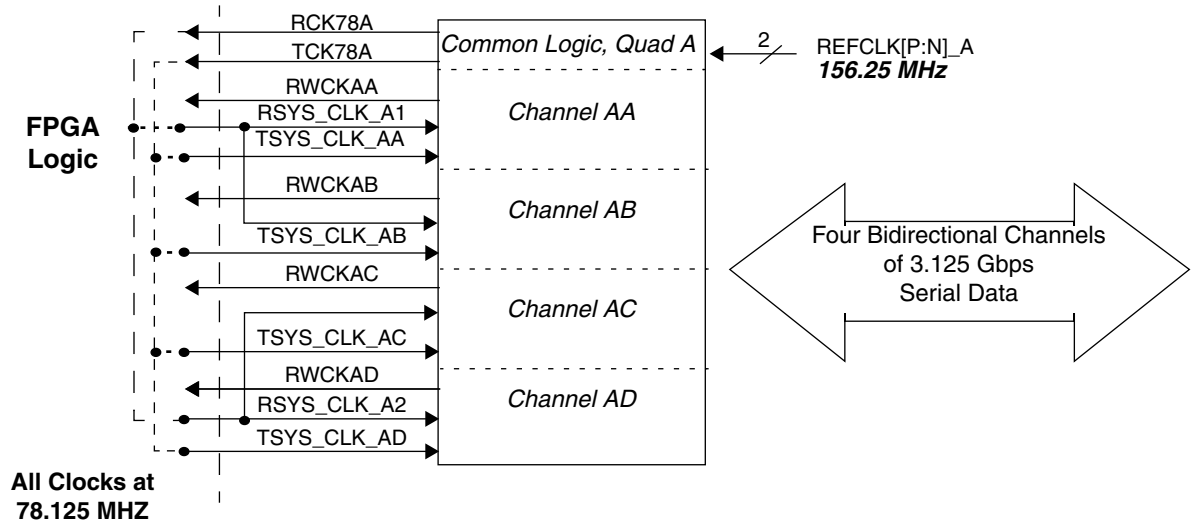
RSYS_CLK_[A:B]2
These clocks are inputs to the SERDES blocks A and B respectively from the FPGA. These are used by each channel as the read clock to read received data from the alignment FIFO within the embedded core. Clock RSYS_CLK_A2 is used by channels in the SERDES block A and RSYS_CLK_B2 by channels in the SERDES block B. To guarantee that there is no overflow in the alignment FIFO, it is an absolute requirement that the write and read clocks be frequency locked within 0 ppm. Examples of how to achieve this are shown in the later section on recommended board-level clocking.

Figure 29. Receive Clocking for a Dual Alignment in a Single Quad (Similar Connections Would Be Used for Quad B)



For receive quad alignment, RSYS_CLK_[A1,B1] and RSYS_CLK_[A2,B2] can be tied together as shown for quad A and B in Figure 30. In receive eight-channel alignment, either RCK78A or RCK78B can be used to source RSYS_CLK_[A1,A2] and RSYS_CLK_[B1,B2] as shown in Figure 31.

Figure 30. Clocking for Quad Alignment in a Single Quad (Similar Connections Would Be Used for Quad B)



- Parallel loopback at MUX/DEMUX boundary excluding SERDES (near end)

The three loopback modes are described in more detail in the following sections. As noted earlier, other specialized loopback modes can be obtained by configuration of the FPGA logic or by connections external to the FPSC.

High-Speed Serial Loopback at the CML Buffer Interface

The high-speed serial loopback mode has the serial transmit signals looped back internally to the serial receive circuitry. The internal loopback path is from the input connection to the transmit CML buffer to the output connection from the receive CML buffer. The data are sourced on the TWDxx[31:0], TCOMMAxx[3:0] and TBIT9xx[3:0] signal lines and received on the MRWDxx[39:0] signal lines. The serial loopback path does not include the high-speed input and output buffers. If TESTEN_xx is set, the HDOUTP_xx and HDOUTN_xx outputs are active in this mode while the CML input buffers are powered down. The device is otherwise in its normal mode of operation. This mode is normally used for tests where the data source and destination are on the same card and is the basic loopback path shown earlier in Figure 32(a).

The data rate selection bits, TXHR and RXHR, in the channel configuration registers must be configured to carry the same value. Table 19 and Table 20 summarize the settings of the control interface register configuration bits for high-speed serial loopback.

Table 19. High-Speed Serial Loopback Configuration Bit Definitions for the ORT42G5

Register Address	Bit Value	Bit Name	Comments
30022, 30032, 30122, 30132	Bit 0 = 0 or 1	TXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 7 = 0 or 1	8B10BT	Set to 0 or 1. If set to 0, the 8b/10b encoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to the same value.
30023, 30033, 30123, 30133	Bit 0 = 0 or 1	RXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 3 = 0 or 1	8B10BR	Set to 0 or 1. If set to 0, the 8b/10b decoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to the same value.
30801, 30901	Bit 2 = 1 (Channel C) Bit 3 = 1 (Channel D)	LOOPENB_xx	Set any of the bits 0-3 to 1 to do serial loopback on the corresponding channel.* The high speed serial outputs will not be active.

*This test mode can also be set using TESTEN_xx in place of LOOPENB_xx. In that case, Test Mode must be set to 00000.

Table 20. High-Speed Serial Loopback Configuration Bit Definitions for the ORT82G5

Register Address	Bit Value	Bit Name	Comments
30002, 30012, 30022, 30032, 30102, 30112, 30122, 30132	Bit 0 = 0 or 1	TXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 7 = 0 or 1	8B10BT	Set to 0 or 1. If set to 0, the 8b/10b encoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to the same value.
30003, 30013, 30023, 30033, 30103, 30113, 30123, 30133	Bit 0 = 0 or 1	RXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 3 = 0 or 1	8B10BR	Set to 0 or 1. If set to 0, the 8b/10b decoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to the same value.

Table 26. Embedded Memory Slice Core/FPGA Interface Signal Description

FPGA/Embedded Core Interface Signal Name]	Input (I) to or Output (O) from Core	Signal Description
Memory Slice Interface Signals		
D_[A:B][35:0]	I	Data in—memory slice [A:B]
CKW_[A:B]	I	Write clock—memory slice [A:B].
CSWA_[A:B]	I	Write chip select for SRAM A—memory slice [A:B].
CSWB_[A:B]	I	Write chip select for SRAM B—memory slice [A:B].
AW_[A:B][10:0]	I	Write address—memory slice [A:B].
BYTEWN_[A:B][3:0]	I	Write control pins for byte-at-a-time write-memory slice [A:B].
Q_[A:B][35:0]	O	Data out—memory slice [A:B].
CKR_[A:B]	I	Read clock—memory slice [A:B].
CSR_[A:B]	I	Read chip select—memory slice [A:B]. CSR_[A:B]= 0 selects SRAM A. CSR_[A:B]= 1 selects SRAM B.
AR_[A:B][10:0]	I	Read address—memory slice [A:B].

Memory Maps

Definition of Register Types

The SERDES blocks within the ORT42G5 and ORT82G5 cores have a set of status and control registers for SERDES operation. There is also other group of status and control registers which are implemented outside the SERDES, which are related to the SERDES and other functional blocks in the FPSC core. (Addresses for the control and status registers for the FPGA portion of the device are detailed in the ORCA Series 4 FPGAs data sheet, which also describes the functions of those registers).

ORT42G5 Memory Map

Each ORT42G5 SERDES block has two independent channels. Each channel is identified by both a quad identifier, A or B, and a channel identifier, C or D. (This naming convention follows that of the ORT82G5.) The registers in ORT42G5 are 8-bit memory locations, which can be classified into Status Register and Control Register.

Status Register

Read-only register to convey the status information of various operations within the FPSC core. An example is the state of the XAUI link-state-machine.

Control Register

Read-write register to set up the control inputs that define the operation of the FPSC core.

Reserved addresses for the FPSC register blocks are shown in Table 29.

Table 27. Structural Register Elements

Address (0x)	Description
300xx	SERDES A, internal registers.
301xx	SERDES B, internal registers.
308xx	Channel A [C or D] registers (external to SERDES blocks).
309xx	Channel B [C or D] registers (external to SERDES blocks).
30A0x	Global registers (external to SERDES blocks).

Table 28 details the memory map for the FPSC portion of the ORT42G5 device. In both Table 29 and Table 28, the addresses are given as 18-bit hexadecimal (18'h) values. The address may be sourced either through the MicroProcessor Interface or a User Master Interface. The MicroProcessor Interface (MPI) address bus is a 32-bit bus

which follows the Power PC convention where address bit 0 is the MSb and address bit 31 is the LSb. The MPI maps bits MPI_ADDR[14:31] to bits [17:0] of the system address bus. The User Master Interface (UMI) has an 18-bit address bus and uses the opposite notation, where address line 17 is the MSb and address line 0 is the LSb. The UMI maps bits um_addr[17:0] to bits [17:0] of the system address bus. Because of the address mapping done by the MPI and UMI, the same hexadecimal address value is valid for both interfaces.

The UMI, internal and microprocessor interface data buses have both 32-bit data and 4-bit parity fields and the data fields are mapped 1:1 to each other, i.e., bit 0 is bit 0 for all three buses. The bit ordering is specific to the targeted functional block. In the memory map, only bits [0:7] are specified and the convention followed for sub-field descriptions is to map the bits in the description directly to the bit order given in the bit column. For example, to select channel C as the source for the transmit and receive clocks, the register at location 30A00 should have bits 0, 2, 4 and 6 set to zero and bits 1, 3, 5 and 7 set to one.

In the example in the previous paragraph, the bits being set are control bits and are independent of the MSb/LSb convention used. The resulting bit pattern 01010101 maps to the hexadecimal value AA if the left-most bit is considered the LSb and to 55 if the right-most bit is considered the LSb. In some cases, however, the data represents the value of a specific parameter, such as a size or threshold level, and the value may be stored at more than one address location, since each location can hold only 8 bits of data. For a given register, either the MSb or the LSb bit position is specified explicitly in the memory map. If the parameter value extends over multiple register locations, the relative bit or byte ordering is also specified. For additional information on the MPI and the system bus, see Technical Note TN1017, *ORCA Series 4 MPI/System Bus.*

Table 28. ORT42G5 Memory Map

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Alarm Registers (Read Only, Clear on Read), xx = [AC, AD, BC or BD]				
30020 - AC 30030 - AD 30120 - BC 30130 - BD	[0]	Reserved	00	Reserved
	[1]	LKI_xx		Receive PLL Lock Indication, Channel xx. LKI_xx = 1 indicates the receive PLL is locked.
	[2]	Not used		Reserved
	[3]	Not used		Reserved
	[4:7]	Not used		Not used
SERDES Alarm Mask Registers (Read/Write), xx = [AC, AD, BC or BD]				
30021 - AC 30031 - AD 30121 - BC 30131 - BD	[0]	Reserved	FF	Reserved, must be set to 1. Set to 1 on device reset.
	[1]	MLKI_xx		Mask Receive PLL Lock Indication, Channel xx.
	[2]	Reserved		Reserved. Must be set to 1. Set to 1 on device reset.
	[3]	Reserved		Reserved. Must be set to 1. Set to 1 on device reset.
	[4]	Reserved		Reserved. Must be set to 1. Set to 1 on device reset.
	[5]	Reserved		Reserved. Must be set to 1. Set to 1 on device reset.
	[6]	Reserved		Reserved. Must be set to 1. Set to 1 on device reset.
	[7]	Reserved		Reserved. Must be set to 1. Set to 1 on device reset.

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Common Transmit and Receive Channel Configuration Registers (Read/Write), xx = [AC, AD, BC or BD]				
30022 - AC 30032 - AD 30122 - BC 30132 - BD	[0]	TXHR_xx	00	Transmit Half Rate Selection Bit, Channel xx. When TXHR_xx = 1, HDOUT_xx's baud rate = (REFCLK[A:B]*10) and TCK78[A:B] =(REFCLK[A:B]/4); when TXHR_xx=0, HDOUT_xx's baud rate = (REFCLK[A:B]*20) and TCK78[A:B]=(REFCLK[A:B]/2). TXHR_xx = 0 on device reset.
	[1]	PWRDNT_xx		Transmit Powerdown Control Bit, Channel xx. When PWRDNT_xx = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT_xx = 0 on device reset.
	[2]	PE0_xx		Transmit Preemphasis Selection Bit 0, Channel xx. PE0_xx and PE1_xx select one of three preemphasis settings for the transmit section. PEO_xx=PE1_xx = 0, Preemphasis is 0% PEO_xx=1, PE1_xx = 0 or PEO_xx=0, PE1_xx = 1, Preemphasis is 12.5% PEO_xx=PE1_xx = 1, Preemphasis is 25%. PEO_xx=PE1_xx = 0 on device reset.
	[3]	PE1_xx		
	[4]	HAMP_xx		Transmit Half Amplitude Selection Bit, Channel xx. When HAMP_xx = 1, the transmit output buffer voltage swing is limited to half its normal amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP_xx = 0 on device reset.
	[5]	Reserved		Reserved. Must be set to 0. Set to 0 on device reset.
	[6]	Reserved		Reserved
	[7]	8b10bT_xx		Transmit 8b/10b Encoder Enable Bit, Channel xx. When 8b10bT_xx = 1, the 8b/10b encoder in the transmit path is enabled. Otherwise, the data is passed unencoded. 8b10bT_xx = 0 on device reset.
30023 - AC 30033 - AD 30123 - BC 30133 - BD	[0]	RXHR_xx	20	Receive Half Rate Selection Bit, Channel xx. When RXHR_xx =1, HDIN_xx's baud rate = (REFCLK[A:B]*10) and RCK78[A:B]=(REFCLK[A:B]/4); when RXHR_xx=0, HDIN_xx's baud rate = (REFCLK[A:B]*20) and RCK78[A:B]=(REFCLK/2). RXHR_xx = 0 on device reset.
	[1]	PWRDNR_xx		Receiver Power Down Control Bit, Channel xx. When PWRDNR_xx = 1, sections of the receive hardware are powered down to conserve power. PWRDNR_xx = 0 on device reset.
	[2]	Reserved		Reserved. Set to 1 on device reset.
	[3]	8b10bR_xx		Receive 8b/10b Decoder Enable Bit, Channel xx. When 8b10bR = 1, the 8b/10b decoder in the receive path is enabled. Otherwise, the data is passed undecoded. 8b10bR_xx = 0 on device reset.
	[4]	LINKSM_xx		Link State Machine Enable Bit, Channel xx. When LINKSM_xx = 1, the receiver Fiber Channel link state machine is enabled. Otherwise, the Fibre Channel link state machine is disabled. Note: LINKSM_xx is ignored when XAUI_MODE_xx=1. LINKSM_xx = 0 on device reset.
	[5:7]	Not used		Not used.

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Common Transmit and Receive Channel Configuration Registers (Read/Write), xx = [AC, AD, BC or BD]				
30024 - AC 30034 - AD 30124 - BC 30134 - BD	[0]	Reserved	See Bit Desc.	Reserved, must be 0. Set to 0 on device reset.
	[1]	MASK_xx		Transmit and Receive Alarm Mask Bit, Channel xx. When MASK_xx = 1, the transmit and receive alarms of a channel are prevented from generating an interrupt (i.e., they are masked or disabled). The MASK_xx bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK_xx = 1 on device reset.
	[2]	SWRST_xx		Transmit and Receive Software Reset Bit, Channel xx. When SWRST_ss = 1, this bit provides the same function as the hardware reset, except that all configuration register settings are unaltered. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. SWRST = 0 on device reset.
	[3:6]	Not used		Not used
	[7]	TESTEN_xx		Transmit and Receive Test Enable Bit, Channel xx. When TESTEN_xx = 1, the transmit and receive sections are placed in test mode. The TestMode_[A:B][4:0] bits in the Global Control Registers specify the particular test, and must also be set. Note: When the global test enable bit GTESTEN_[A:B] = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN_[A:B] = 1, all channels in a block are set to test mode regardless of their TESTEN setting. TESTEN_xx = 0 on device reset.
SERDES Global Control Registers (Read Write) - Act on Both Channels in SERDES Block A or SERDES Block B.				
30005 - A 30105 - B	[0]	Reserved	See Bit Desc.	Reserved, must be 0. Set to 0 on device reset.
	[1]	GMASK_[A:B]		Global Mask. When GMASK_[A:B] = 1, the transmit and receive alarms of both channels in the SERDES block are prevented from generating an interrupt (i.e., they are masked or disabled). The GMASK_[A:B] bit overrides the individual MASK_xx bits. GMASK_[A:B] = 1 on device reset.
	[2]	GSWRST_[A:B]		Software reset bit. The GSWRST_[A:B] bit provides the same function as the hardware reset for the transmit and receive sections of both channels, except that the device configuration settings are not affected when GSWRST_[A:B] is asserted. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. The GSWRST_[A:B] bit overrides the individual SWRST_xx bits. GSWRST_[A:B] = 0 on device reset.
	[3]	GPWRDNT_[A:B]		Powerdown Transmit Function. When GPWRDNT_[A:B] = 1, sections of the transmit hardware for both channels are powered down to conserve power. The GPWRDNT_[A:B] bit overrides the individual PWRDNT_xx bits. GPWRDNT_[A:B] = 0 on device reset.
	[4]	GPWRDNR_[A:B]		Powerdown Receive Function. When GPWRDNR_[A:B] = 1, sections of the receive hardware for both channels are powered down to conserve power. The GPWRDNR_[A:B] bit overrides the individual PWRDNR_xx bits. GPWRDNR_[A:B] = 0 on device reset.
	[5]	Reserved		Reserved, 1 on device reset.
	[6]	Not used		Not used
	[7]	GTESTEN_[A:B]		Test Enable Control. When GTESTEN_[A:B] = 1, the transmit and receive sections of both channels are placed in test mode. The GTESTEN_[A:B] bit overrides the individual TESTEN_xx bits. GTESTEN_[A:B] = 0 on device reset.
30006 - A 30106 - B	[0:4]	TestMode[A:B]	00	Test Mode - See Test Mode section for settings
	[5]	Not used		Not used
	[6:7]	Reserved		Reserved

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30810 - Ax 30910 - Bx	[0]]	—	00	Reserved for future use
	[1]	—		Reserved for future use
	[2]	DOWDALIGN_xC		Word Realign Bit. When DOWDALIGN_xC transitions from 0 to 1, the receiver realigns on the next comma character for Channel xC. NOWDALIGN_xC=0 on device reset.
	[3]	DOWDALIGN_xC		Word Realign Bit. When DOWDALIGN_xC transitions from 0 to 1, the receiver realigns on the next comma character for Channel xC. NOWDALIGN_xC=0 on device reset.
	[4]	—		Reserved for future use. Set to zero.
	[5]	—		Reserved for future use. Set to zero.
	[6]	FMPU_STR_EN _xC		Enable multi-channel alignment for Channel xC. When FMPU_STR_EN _xC = 0, Channel xC is not part of a multi-channel alignment group When FMPU_STR_EN _xC = 1, Channel xC is part of a twin channel alignment (SERDES block A or B) or quad channel alignment (both SERDES blocks) group.
	[7]	FMPU_STR_EN _xD		Enable multi-channel alignment for Channel xD. When FMPU_STR_EN _xD = 0, Channel xD is not part of a multi-channel alignment group When FMPU_STR_EN _xD = 1, Channel xD is part of a twin channel alignment (SERDES block A or B) or quad channel alignment (both SERDES blocks) group.
30811 - Ax 30911 - Bx	[0:7]	FMPU_SYNMODE_ [A:B]	00	Sync mode for block [A:B] 00000000 = No channel alignment 00001010 = Twin channel alignment, SERDES block [A:B] 00001111 = Quad channel alignment (both SERDES blocks)
30820 - Ax 30920 - Bx	[0]	—	00	Reserved for future use.
	[1]	—		Reserved for future use.
	[2]	FMPU_RESYNC1_xC		Resync a Single Channel. When FMPU_RESYNC1_xC transitions from 0 to 1, the corresponding channel xC is resynchronized (the write and read pointers are reset). FMPU_STR_EN_xC=0 on device reset.
	[3]	FMPU_RESYNC1_xD		Resync a Single Channel. When FMPU_RESYNC1_xD transitions from 0 to 1, the corresponding channel xD is resynchronized (the write and read pointers are reset). FMPU_STR_EN_xD=0 on device reset.
	[4]	—		Reserved for future use.
	[5]	FMPU_RESYNC2[A:B]		Resync a Twin-Channel Group. When FMPU_RESYNC2[A:B] transitions from a 0 to a 1, the corresponding twin-channel group is resynchronized. FMPU_RESYNC2[A:B]=0 on device reset.
	[6]	—		Reserved for future use.
	[7]	XAUI_MODE[A:B]		Controls use of XAUI link state machine in place of Fibre-Channel state machine. When XAUI_MODE[A:B]=1, both channels in the SERDES block enable their XAUI link state machines. (LINKSM_xx bits are ignored). XAUI_MODE[A:B]=0 on device reset.
30821 - A 30921 - B	[0]	NOCHALGN [A:B]	00	Bypass channel alignment. NOCHALGN [A:B] =1 causes bypassing of multi-channel alignment FIFOs for the corresponding SERDES quad. NOCHALGN [A:B] =0 on device reset.
	[1:7]	—		Reserved for future use.

High Speed Data Transmitter

Table 32 specifies serial data output buffer parameters measured on devices with typical and worst case process parameters and over the full range of operation conditions.

Table 32. Serial Output Timing and Levels (CML I/O)

Parameter	Min.	Typ.	Max.	Units
Rise Time (20%—80%)	50	80	110	ps
Fall Time (80%—20%)	50	80	110	ps
Common Mode	VDDOB - 0.30	VDDOB - 0.25	VDDOB - 0.15	V
Differential Swing (Full Amplitude)[1]	600	700	1000	mVp-p
Differential Swing (Half Amplitude)[1]	300	350	500	mVp-p
Output Load (external)	—	86	—	Ω

1. Differential swings measured at the end of 3 inches of FR-4 and 12 inches of coax cable.

Transmitter output jitter is a critical parameter to systems with high speed data links. Table 33 and Table 34 specify the transmitter output jitter for typical and worst case devices over the full range of operating conditions.

Table 33. Channel Output Jitter (3.125 Gbps)

Parameter	Device	Min.	Typ.[1]	Max.[1]	Units
Deterministic	ORT42G5	—	0.12	0.21	Ulp-p
	ORT82G5	—	0.12	0.16	Ulp-p
Random	ORT42G5	—	0.05	0.10	Ulp-p
	ORT82G5	—	0.05	0.08	Ulp-p
Total[2, 3]	ORT42G5	—	0.17	0.31	Ulp-p
	ORT82G5	—	0.17	0.24	Ulp-p

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., 0ºC to 85ºC, 1.425V to 1.575V supply.
2. Wavecrest SIA-3000 instrument used to measure one-sigma (rms) random jitter component value. This value is multiplied by 14 to provide the peak-to-peak value that corresponds to a BER of 10^{-12}.
3. Total jitter measurement performed with Wavecrest SIA-3000 at a BER of 10^{-12}. See instrument documentation and other Wavecrest publications for a detailed discussion of jitter types included in this measurement.

Table 34. Channel Output Jitter (2.5 Gbps)

Parameter	Device	Min.	Typ.[1]	Max.[1]	Units
Deterministic	ORT42G5	—	0.11	0.13	Ulp-p
	ORT82G5	—	0.11	0.13	Ulp-p
Random	ORT42G5	—	0.05	0.14	Ulp-p
	ORT82G5	—	0.05	0.07	Ulp-p
Total[2, 3]	ORT42G5	—	0.16	0.27	Ulp-p
	ORT82G5	—	0.16	0.20	Ulp-p

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., 0ºC to 85ºC, 1.425V to 1.575V supply.
2. Wavecrest SIA-3000 instrument used to measure one-sigma (rms) random jitter component value. This value is multiplied by 14 to provide the peak-to-peak value that corresponds to a BER of 10^{-12}.
3. Total jitter measurement performed with Wavecrest SIA-3000 at a BER of 10^{-12}. See instrument documentation and other Wavecrest publications for a detailed discussion of jitter types included in this measurement.

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
V4	-	-	IO	LVDS_R	LVDS_R	-
V3	-	-	VDD33	VDD33	-	-
F17	-	-	VDD15	VDD15	-	-
W3	6 (BL)	5	IO	PB2A	DP2	-
AA2	6 (BL)	5	IO	PB2C	PLL_CK6T/PPLL	L23T
AB2	6 (BL)	5	IO	PB2D	PLL_CK6C/PPLL	L23C
AA3	6 (BL)	5	IO	PB4A	VREF_6_05	L24T
AB3	6 (BL)	5	IO	PB4B	DP3	L24C
T5	6 (BL)	-	VDDIO6	VDDIO6	-	-
H7	-	-	VSS	VSS	-	-
Y4	6 (BL)	6	IO	PB5C	VREF_6_06	L25T
W4	6 (BL)	6	IO	PB5D	D14	L25C
T8	6 (BL)	-	VDDIO6	VDDIO6	-	-
AA4	6 (BL)	7	IO	PB6C	D15	L26T
AB4	6 (BL)	7	IO	PB6D	D16	L26C
H8	-	-	VSS	VSS	-	-
W5	6 (BL)	7	IO	PB7C	D17	L27T
Y5	6 (BL)	7	IO	PB7D	D18	L27C
T9	6 (BL)	-	VDDIO6	VDDIO6	-	-
AA5	6 (BL)	7	IO	PB8C	VREF_6_07	L28T
AB5	6 (BL)	7	IO	PB8D	D19	L28C
H9	-	-	VSS	VSS	-	-
V6	6 (BL)	8	IO	PB9C	D20	-
G6	-	-	VDD15	VDD15	-	-
W6	6 (BL)	8	IO	PB10C	VREF_6_08	L29T
Y6	6 (BL)	8	IO	PB10D	D22	L29C
H10	-	-	VSS	VSS	-	-
AA6	6 (BL)	9	IO	PB11C	D23	L30T
AB6	6 (BL)	9	IO	PB11D	D24	L30C
U6	6 (BL)	-	VDDIO6	VDDIO6	-	-
W7	6 (BL)	9	IO	PB12C	VREF_6_09	L31T
Y7	6 (BL)	9	IO	PB12D	D25	L31C
H11	-	-	VSS	VSS	-	-
V7	6 (BL)	10	IO	PB14A	-	-
U7	6 (BL)	-	VDDIO6	VDDIO6	-	-
AA7	6 (BL)	10	IO	PB14C	VREF_6_10	L32T
AB7	6 (BL)	10	IO	PB14D	D28	L32C
V8	6 (BL)	11	IO	PB15A	-	-
H12	-	-	VSS	VSS	-	-
W8	6 (BL)	11	IO	PB15C	D29	L33T
Y8	6 (BL)	11	IO	PB15D	D30	L33C
U8	6 (BL)	11	IO	PB16A	-	-
AA8	6 (BL)	11	IO	PB16C	VREF_6_11	L34T
AB8	6 (BL)	11	IO	PB16D	D31	L34C

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
V9	5 (BC)	1	IO	PB17A	-	-
W9	5 (BC)	1	IO	PB17C	-	L35T
Y9	5 (BC)	1	IO	PB17D	-	L35C
U9	5 (BC)	1	IO	PB18A	-	-
AA9	5 (BC)	1	IO	PB18C	VREF_5_01	L36T
AB9	5 (BC)	1	IO	PB18D	-	L36C
G16	-	-	VDD15	VDD15	-	-
H13	-	-	VSS	VSS	-	-
AB10	5 (BC)	2	IO	PB19A	-	L37T
AA10	5 (BC)	2	IO	PB19B	-	L37C
W10	5 (BC)	2	IO	PB19C	PBCK0T	L38T
Y10	5 (BC)	2	IO	PB19D	PBCK0C	L38C
V10	5 (BC)	2	IO	PB20A	-	-
U13	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB11	5 (BC)	2	IO	PB20C	VREF_5_02	L39T
AA11	5 (BC)	2	IO	PB20D	-	L39C
U10	5 (BC)	2	IO	PB21A	-	-
H6	-	-	VDD15	VDD15	-	-
Y11	5 (BC)	3	IO	PB21C	-	L40T
W11	5 (BC)	3	IO	PB21D	VREF_5_03	L40C
U11	5 (BC)	3	IO	PB22A	-	-
J7	-	-	VSS	VSS	-	-
AB12	5 (BC)	3	IO	PB22C	-	L41T
AA12	5 (BC)	3	IO	PB22D	-	L41C
U12	5 (BC)	3	IO	PB23A	-	-
Y12	5 (BC)	3	IO	PB23C	PBCK1T	L42T
W12	5 (BC)	3	IO	PB23D	PBCK1C	L42C
V11	5 (BC)	3	IO	PB24A	-	-
J8	-	-	VSS	VSS	-	-
AB13	5 (BC)	4	IO	PB24C	-	L43T
AA13	5 (BC)	4	IO	PB24D	-	L43C
V12	5 (BC)	4	IO	PB25A	-	-
U14	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB14	5 (BC)	4	IO	PB25C	-	L44T
AA14	5 (BC)	4	IO	PB25D	VREF_5_04	L44C
J9	-	-	VSS	VSS	-	-
Y13	5 (BC)	5	IO	PB26C	-	L45T
W13	5 (BC)	5	IO	PB26D	VREF_5_05	L45C
U15	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB15	5 (BC)	5	IO	PB27C	-	L46T
AA15	5 (BC)	5	IO	PB27D	-	L46C
AB16	5 (BC)	6	IO	PB28C	-	L47T
AA16	5 (BC)	6	IO	PB28D	VREF_5_06	L47C
H14	-	-	VDD15	VDD15	-	-

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AA15	—	—	VSS	VSS	—	—
L4	0 (TL)	10	IO	PL11B	—	—
N5	7 (CL)	1	IO	PL12D	A15/PPC_A29	L1C_D0
M4	7 (CL)	1	IO	PL12C	A14/PPC_A28	L1T_D0
AA3	7 (CL)	—	VDDIO7	VDDIO7	—	—
L3	7 (CL)	1	IO	PL12B	—	L2C_D0
K2	7 (CL)	1	IO	PL12A	—	L2T_D0
H1	7 (CL)	1	IO	PL13D	VREF_7_01	L3C_A0
J1	7 (CL)	1	IO	PL13C	D4	L3T_A0
V18	—	—	VSS	VSS	—	—
N4	7 (CL)	2	IO	PL13B	—	L4C_D0
P5	7 (CL)	2	IO	PL13A	—	L4T_D0
M3	7 (CL)	2	IO	PL14D	RDY/BUSY_N/RCLK	L5C_D0
L2	7 (CL)	2	IO	PL14C	VREF_7_02	L5T_D0
AC2	7 (CL)	—	VDDIO7	VDDIO7	—	—
K1	7 (CL)	2	IO	PL14B	—	L6C_A0
L1	7 (CL)	2	IO	PL14A	—	L6T_A0
P4	7 (CL)	2	IO	PL15D	A13/PPC_A27	L7C_A0
P3	7 (CL)	2	IO	PL15C	A12/PPC_A26	L7T_A0
V19	—	—	VSS	VSS	—	—
M2	7 (CL)	2	IO	PL15B	—	L8C_A0
M1	7 (CL)	2	IO	PL15A	—	L8T_A0
N2	7 (CL)	3	IO	PL16D	—	L9C_A0
N1	7 (CL)	3	IO	PL16C	—	L9T_A0
N3	7 (CL)	—	VDDIO7	VDDIO7	—	—
R4	7 (CL)	3	IO	PL16B	—	—
P2	7 (CL)	3	IO	PL17D	A11/PPC_A25	L10C_D0
R3	7 (CL)	3	IO	PL17C	VREF_7_03	L10T_D0
W16	—	—	VSS	VSS	—	—
R5	7 (CL)	3	IO	PL17B	—	—
P1	7 (CL)	3	IO	PL18D	—	L11C_A0
R1	7 (CL)	3	IO	PL18C	—	L11T_A0
T5	7 (CL)	3	IO	PL18B	—	L12C_A0
T4	7 (CL)	3	IO	PL18A	—	L12T_A0
T3	7 (CL)	4	IO	PL19D	RD_N/MPI_STRB_N	L13C_A0
T2	7 (CL)	4	IO	PL19C	VREF_7_04	L13T_A0
W17	—	—	VSS	VSS	—	—
U1	7 (CL)	4	IO	PL19B	—	L14C_A0
T1	7 (CL)	4	IO	PL19A	—	L14T_A0
U4	7 (CL)	4	IO	PL20D	PLCK0C	L15C_A0
U5	7 (CL)	4	IO	PL20C	PLCK0T	L15T_A0
R2	7 (CL)	—	VDDIO7	VDDIO7	—	—
U2	7 (CL)	4	IO	PL20B	—	L16C_D0
V1	7 (CL)	4	IO	PL20A	—	L16T_D0

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
B29	1 (TC)	8	IO	PT33D	—	L1C_A0
C29	1 (TC)	8	IO	PT33C	VREF_1_08	L1T_A0
B15	1 (TC)	—	VDDIO1	VDDIO1	—	—
E27	1 (TC)	8	IO	PT32D	—	L2C_A0
E26	1 (TC)	8	IO	PT32C	—	L2T_A0
AP34	—	—	Vss	Vss	—	—
A30	1 (TC)	8	IO	PT32B	—	—
A29	1 (TC)	9	IO	PT31D	—	L3C_D3
E25	1 (TC)	9	IO	PT31C	VREF_1_09	L3T_D3
B17	1 (TC)	—	VDDIO1	VDDIO1	—	—
E24	1 (TC)	9	IO	PT31A	—	—
B28	1 (TC)	9	IO	PT30D	—	L4C_A0
C28	1 (TC)	9	IO	PT30C	—	L4T_A0
B2	—	—	Vss	Vss	—	—
D28	1 (TC)	9	IO	PT30A	—	—
C27	1 (TC)	9	IO	PT29D	—	L5C_A0
D27	1 (TC)	9	IO	PT29C	—	L5T_A0
E23	1 (TC)	9	IO	PT29B	—	L6C_A0
E22	1 (TC)	9	IO	PT29A	—	L6T_A0
D26	1 (TC)	1	IO	PT28D	—	L7C_A0
D25	1 (TC)	1	IO	PT28C	—	L7T_A0
B33	—	—	Vss	Vss	—	—
D24	1 (TC)	1	IO	PT28B	—	L8C_A0
D23	1 (TC)	1	IO	PT28A	—	L8T_A0
C26	1 (TC)	1	IO	PT27D	VREF_1_01	L9C_A0
C25	1 (TC)	1	IO	PT27C	—	L9T_A0
D11	1 (TC)	—	VDDIO1	VDDIO1	—	—
E21	1 (TC)	1	IO	PT27B	—	L10C_A0
E20	1 (TC)	1	IO	PT27A	—	L10T_A0
D22	1 (TC)	2	IO	PT26D	—	L11C_A0
D21	1 (TC)	2	IO	PT26C	VREF_1_02	L11T_A0
E34	—	—	Vss	Vss	—	—
A28	1 (TC)	2	IO	PT26B	—	—
B26	1 (TC)	2	IO	PT25D	—	L12C_A0
B25	1 (TC)	2	IO	PT25C	—	L12T_A0
D13	1 (TC)	—	VDDIO1	VDDIO1	—	—
B27	1 (TC)	2	IO	PT25B	—	—
A27	1 (TC)	3	IO	PT24D	—	L13C_A0
A26	1 (TC)	3	IO	PT24C	VREF_1_03	L13T_A0
N13	—	—	Vss	Vss	—	—
C24	1 (TC)	3	IO	PT24B	—	—
C22	1 (TC)	3	IO	PT23D	—	L14C_A0
C23	1 (TC)	3	IO	PT23C	—	L14T_A0
D15	1 (TC)	—	VDDIO1	VDDIO1	—	—

Table 46. Heat Sink Vendors

Vendor	Location	Phone
Aavid Thermalloy	Concord, NH	(603) 224-9988
Chip Coolers	Warwick, RI	(800) 227-0254
IERC	Burbank, CA	(818) 842-7277
R-Theta	Buffalo, NY	(800) 388-5428
Sanyo Denki	Torrance, CA	(310) 783-5400
Wakefield Thermal Solutions	Pelham, NH	(800) 325-1426

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 47 lists eight parasitics associated with the ORCA packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

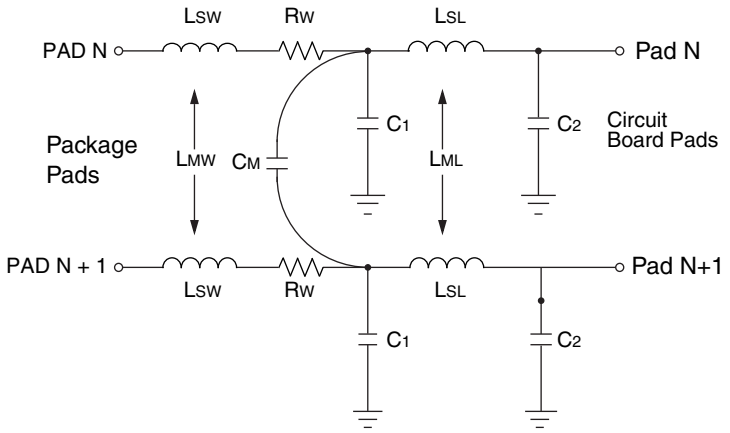
Four inductances in nH are listed: L_{SW} and L_{SL}, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead. Resistance values are in mΩ.

The parasitic values in Table 47 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C_1 and C_2 capacitors.

Table 47. ORCA Typical Package Parasitics

L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
3.8	1.3	250	1.0	1.0	0.3	2.8-5	0.5 -1

Figure 41. Package Parasitics



Package Outline Drawings

Package Outline Drawings for the 484-ball PBGAM (fpBGA) used for the ORT42G5 and 680-ball PBGAM (fpBGA) used for the ORT82G5 are available in the Package Diagrams section of the Lattice Semiconductor web site at www.latticesemi.com.