Lattice Semiconductor Corporation - ORT42G5-2BMN484C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	204
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort42g5-2bmn484c

Programmable Features

- High-performance programmable logic:
  - 0.16 µm 7-level metal technology.
  - Internal performance of >250 MHz.
  - Over 400K usable system gates.
  - Meets multiple I/O interface standards.
  - 1.5V operation (30% less power than 1.8V operation) translates to greater performance.
- Traditional I/O selections:
  - LVTTL (3.3V) and LVCMOS (2.5V and 1.8V) I/Os.
  - Per pin-selectable I/O clamping diodes provide 3.3V PCI compliance.
  - Individually programmable drive capability: 24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
  - Two slew rates supported (fast and slew-limited).
  - Fast-capture input latch and input Flip-Flop (FF)/latch for reduced input setup time and zero hold time.
  - Fast open-drain drive capability.
  - Capability to register 3-state enable signal.
  - Off-chip clock drive capability.
  - Two-input function generator in output path.
- New programmable high-speed I/O:
  - Single-ended: GTL, GTL+, PECL, SSTL3/2 (class I and II), HSTL (Class I, III, IV), ZBT, and DDR.
  - Double-ended: LVDS, bused-LVDS, and LVPECL. Programmable (on/off) internal parallel termination (100 Ω) is also supported for these I/Os.
- New capability to (de)multiplex I/O signals:
  - New DDR on both input and output at rates up to 350 MHz (700 MHz effective rate).
  - New 2x and 4x downlink and uplink capability per I/O (i.e., 50 MHz internal to 200 MHz I/O).
- Enhanced twin-block Programmable Function Unit (PFU):
  - Eight 16-bit Look-Up Tables (LUTs) per PFU.
  - Nine user registers per PFU, one following each LUT, and organized to allow two nibbles to act independently, plus one extra for arithmetic operations.
  - New register control in each PFU has two independent programmable clocks, clock enables, local SET/RESET, and data selects.
  - New LUT structure allows flexible combinations of LUT4, LUT5, new LUT6, 4 → 1 MUX, new 8 → 1 MUX, and ripple mode arithmetic functions in the same PFU.
  - 32 x 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the Supplemental Logic and Interconnect Cell (SLIC) decoders as bank drivers.
  - Soft-Wired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU through fast internal routing which reduces routing congestion and improves speed.
  - Flexible fast access to PFU inputs from routing.
  - Fast-carry logic and routing to all four adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Abundant high-speed buffered and nonbuffered routing resources provide 2x average speed improvements over previous architectures.
- Hierarchical routing optimized for both local and global routing with dedicated routing resources. This results in faster routing times with predictable and efficient performance.
- SLIC provides eight 3-statable buffers, up to a 10-bit decoder, and PAL®-like AND-OR-Invert (AOI) in each programmable logic cell.
- New 200 MHz embedded block-port RAM blocks, two read ports, two write ports, and two sets of byte lane enables. Each embedded RAM block can be configured as:

Dual Port RAMs

In addition to the backplane interface blocks, there are two independent memory blocks in the ASB. Each memory block has a capacity of 4k words by 36 bits. It has one read port, one write port, and four byte-write-enable (active-low) signals. The read data from the memory block is registered so that it works as a pipelined synchronous memory block.

FPSC Configuration

Configuration of the ORT42G5 and ORT82G5 occurs in two stages: FPGA bitstream configuration and embedded core setup.

Prior to becoming operational, the FPGA goes through a sequence of states, including power up, initialization, configuration, start-up, and operation. The FPGA logic is configured by standard FPGA bit stream configuration means as discussed in the Series 4 FPGA data sheet.

After the FPGA configuration is complete, the options for the embedded core are set based on the contents of registers that are accessed through the FPGA system bus.

The system bus itself can be driven by an external PowerPC compliant microprocessor via the MPI block or via a user master interface in FPGA logic. A simple IP block that drives the system by using the user register interface and very little FPGA logic is available in the MPI/System Bus Technical Note. This IP block sets up the embedded core via a state machine and allows the ORT42G5 and ORT82G5 to work in an independent system without an external microprocessor interface.

Backplane Transceiver Core Detailed Description

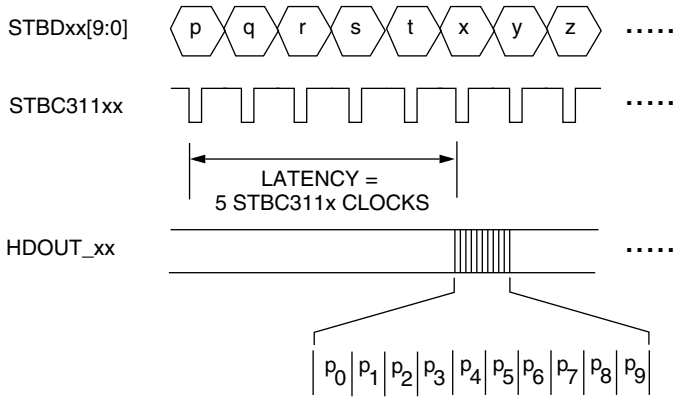
The following sections describe the various logic blocks in the Embedded Core portion of the FPSC. The FPGA section of the FPSC is identical to an ORCA OR4E04 FPGA except that the pads on one edge of the FPGA chip are replaced by the Embedded Core. For a detailed description of the programmable logic functions, please see the ORCA Series 4 FPGA Data Sheet and related application and technical notes.

The major functional blocks in the Embedded Core include:

- Two SERializer-DESerializer (SERDES) blocks and Clock and Data Recovery (CDR) circuitry
- 8b/10b encoder/decoders
- Transmit pre-emphasis circuitry
- 4-to-1 multiplexers (MUX) and 1-to-4 demultiplexers (DEMUX)
- Fibre channel synchronization state machine
- XAUI link alignment state machine
- Alignment FIFOs
- Embedded 4K x 36 RAM blocks (independent from transceiver logic).

A top level block diagram of the Embedded Core Logic is shown in Figure 2. The Embedded RAM blocks are not shown. The external pins for the Embedded Core are listed later in this data sheet in Table 41 and the signals at the Transceiver Embedded Core/FPGA interface for the ORT42G5 are listed in Table 8, Table 9 and Table 11; and for the ORT82G5, in Table 8, Table 10 and Table 12.

Figure 5. Transmit Path Timing - Single SERDES Channel



Each block also sends a clock to the FPGA logic. This clock, TCK78[A,B], is sourced from one of the four MUX blocks and has the same frequency as TSYS_CLK_xx, but arbitrary phase. Within each MUX block, the low frequency clock output is obtained by dividing by 4 the SERDES STBC311x clock which is used internally to synchronize the transmit data words. TCKSEL control bits select the channel to source TCK78[A:B].

The internal signals STBDxx[9:0] (where xx is represents AA...BD or AC, AD, BC, BD) from the MUX block carry unencoded character data and control bits. The 10th bit (STBDxx[9]) of each data lane into the SERDES is used to force a negative disparity present state.

8b/10b Encoder and 1:10 Multiplexer

The 8b/10b encoder encodes the incoming 8-bit data into a 10-bit format as described previously. The input signals to the block, STBDxx[7:0] are used for the 8-bit unencoded data. STBDxx[8] is used as the K_control input to indicate whether the 8 data bits need to be encoded as special characters (K_control = 1) or as data characters (K_control = 0). When STBDxx[9:0] = 1, a negative disparity present state is forced. When the encoder is bypassed STBDxx[9:0] serve as the data bits for the 10-bit unencoded data.

Within the definition of the 8b/10b transmission code, the bit positions of the 10-bit encoded transmission characters are labeled as a, b, c, d, e, i, f, g, h, and j in that order. Bit a corresponds to STBDxx[0], bit b to STBDxx[1], bit c to STBDxx[2], bit d to STBDxx[3], bit e to STBDxx[4], bit i to STBDxx[5], bit f to STBDxx[6], bit g to STBDxx[7], bit h to STBDxx[8], and bit j to STBDxx[9].

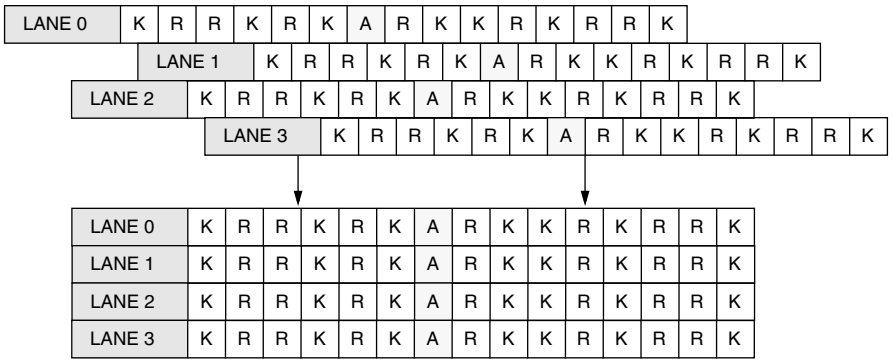
The 10-bit wide parallel data is converted to serial data by the 10:1 Multiplexer. The serial data are then sent to the CML output buffer and are transmitted serially with STBDxx[0] transmitted first and STBDxx[9] transmitted last.

CML Output Buffer

The transmitter's CML output buffer is terminated on-chip in 86 ohms to optimize the data eye as well as to reduce the number of discrete components required. The differential output swing reaches a maximum of 1.2 V_{PP} in the normal amplitude mode. A half amplitude mode can be selected via configuration register bit HAMP_xx. Half amplitude mode can be used to reduce power dissipation when the transmission medium has minimal attenuation or for testing of the integrity (loss) of the physical medium.

A programmable preemphasis circuit is provided to boost the high frequencies in the transmit data signal to maximize the data eye opening at the far-end receiver. Preemphasis is particularly useful when the data are transmitted over backplanes or low-quality coax cables which have a frequency-dependent amplitude loss. For example, for FR4 material at 2.5 GHz, the attenuation compared to the 1.0 GHz value is about 3 dB. The attenuation is a result of skin effect loss of the PCB conductor and the dielectric loss of the PCB substrate. This attenuation causes intersymbol interface which results in the closing of the data eye opening at the receiver.

Figure 16. Deskew Lanes by Aligning /A/ Columns



Mixing Half-rate, Full-rate Modes

When channel alignment is enabled, all receive channels within an alignment group should be configured at the same rate. For example, in the ORT82G5 channels AA, AB, can be configured for twin alignment and full-rate mode, while channels AC, AD that form an alignment group can be configured for half-rate mode. In block alignment mode, each receive block can be configured in either half or full-rate mode.

When channel alignment is disabled within a block, any receive channel within the block can be used in half-rate or full-rate mode. The clocking strategy for half-rate mode in both scenarios (channel alignment enabled or disabled) is described in the Reference Clocks and Internal Clock Distribution sections later in this data sheet.

Multi-channel Alignment Configuration

ORT42G5 Configuration

At startup, the legacy SERDES channel logic must be powered down and removed from any multi-channel alignment groups:

- Setting bit 1 to one in registers at locations 30002, 30012, 30102, 30112, 30003, 30013, 30103 and 30113 powers down the legacy logic. (Note that the reset value for these bits is 0.)
- Setting bits 4 and 5 to zero (reset condition) in the register at locations 30810 and 30910 removes the legacy logic from any alignment group.

Register settings for multi-channel alignment are shown in Table 6.

Table 6. Multichannel Alignment Modes

Register Bits FMPU_SYNMODE_[A:B][0:7]	Mode
00000000	No multichannel alignment.
00001010	Twin channel alignment.
00001111	Four channel alignment.

To align two channels in SERDES A:

- FMPU_SYNMODE_A = 00001010 (Register Location 30811)

To align two channels in SERDES B:

- FMPU_SYNMODE_B = 00001010 (Register Location 30911)

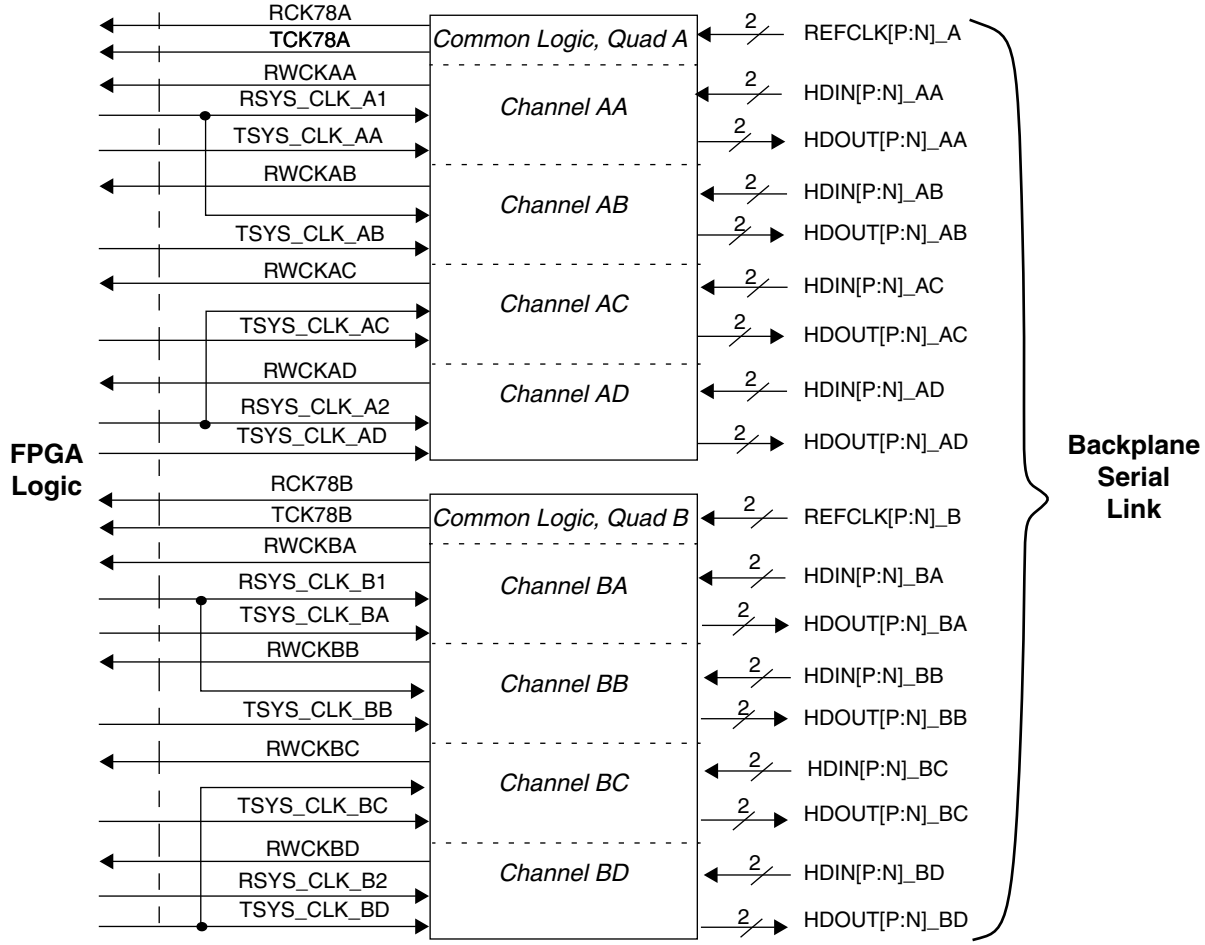
To align all four channels:

- FMPU_SYNMODE_A = 00001111 (Register Location 30811)

Internal Clock Signals at the FPGA/Core Interface for the ORT82G5

There are several clock signals defined at the FPGA/Embedded Core interface in addition to the external reference clock for each SERDES quad. All of the ORT82G5 clock signals are shown in Figure 24 and are described following the figure.

Figure 24. ORT82G5 Clock Signals (High Speed Serial I/O Also Shown)



REFCLKP_[A:B], REFCLKN_[A:B]:
These are the differential reference clocks provided to the ORT82G5 device as described earlier. They are used as the reference clock for both TX and RX paths. For operation of the serial links at 3.125 Gbps, the reference clocks will be at a frequency of 156.25 MHz.

RWCK[AA:BD]:
These are the low-speed receive clocks from the embedded core to the FPGA across the core-FPGA interface. These are derived from the recovered low-speed complementary clocks from the SERDES blocks. RWCK_AA belongs to Channel AA, RWCK_AB belongs to channel AB and so on. With a reference clock input of 156.25 MHz, these clocks operate at 78.125 MHz.

RCK78[A:B]:
These are muxed outputs of RWCKA[A:D] and RWCKB[B:D] respectively. With a reference clock input of 156.25 MHz, these clocks operate at 78.125 MHz.

RSYS_CLK_[A:B][1:2]
These clocks are inputs to the SERDES quad block A and B respectively from the FPGA. These are used by each channel as the read clock to read received data from the alignment FIFO within the embedded core. Clocks RSYS_CLK_A[1:2] are used by channels in the SERDES quad block A and RSYS_CLK_B[1:2] by channels in the SERDES quad block B. To guarantee that there is no overflow in the alignment FIFO, it is an absolute requirement that the write and read clocks be frequency locked within 0 ppm. Examples of how to achieve this are shown in the later section on recommended board-level clocking.

TCK78[A:B]:
This is a muxed output from the core to the FPGA across the core-FPGA interface of one of the 4 transmit SERDES clocks per quad operating at up to 92.5 MHz in the embedded core. There is one clock output per SERDES quad block.

TSYS_CLK[AA,…BD]:
These clocks are inputs to the SERDES quad block A and B respectively from the FPGA. These are used by each channel to control the timing of the Transmit Data Path. To guarantee correct transmit operation theses clocks must be frequency locked within 0 ppm to TCK78[A:B].

Transmit and Receive Clock Rates

Table 16 shows the typical relationship between the data rates, the reference clock, the transmit TCK78[A:B] clock and the receive RCK78[A:B] clock. The selection of full-rate or half-rate for a given reference clock speed is set by bits in the transmit and receive control registers and can be set per channel.

Table 16. Transmit Data and Clock Rates

Data Rate	Reference Clock	TCK78[A: B] and RCK78[A:B] Clocks	Rate of Channel Selected as Clock Source
0.6 Gbps	60 MHz	15 MHz	Half
1.0 Gbps	100 MHz	25 MHz	Half
1.25 Gbps	125 MHz	31.25 MHz	Half
2.0 Gbps	100 MHz	50 MHz	Full
2.5 Gbps	125 MHz	62.5 MHz	Full
3.125 Gbps	156 MHz	78 MHz	Full
3.7 Gbps	185 MHz	92.5 MHz	Full

Besides taking in a TSYS_CLK_xx from the FPGA logic for each channel, the transmit path logic sends back a clock of the same frequency, but arbitrary phase. This clock, TCK78[A:B], is derived from the MUX block of one of the 4 channels in its SERDES quad. The MUX blocks provide the potential source for TCK78[A:B] by a divide-by-4 of the SERDES STBC311xs clock used in synchronizing the transmit data words in the STBC311xx clock domain. The STBC311xx clocks are internal to the core and are not brought across the core/FPGA interface.

The receiver section receives high-speed serial data at its differential CML input port and sends in to the Clock and Data Recovery (CDR) block. The CDR block then generates a recovered clock (RWCKxx) and retimes the data. Thus, the recovered receive clocks are asynchronous between channels.

Transmit Clock Source Selection

The TCKSEL[0:1][A:B] bits select the source channel of TCK78[A:B]. The selection of the source for TCK78[A:B] is controlled by these bits as shown in Table 17.

Register Address	Bit Value	Bit Name	Comments
30801, 30901	Bit 0 =1 (Channel A) Bit 1 = 1 (Channel B) Bit 2 = 1 (Channel C) Bit 3 = 1 (Channel D)	LOOPENB_xx	Set any of the bits 0-3 to 1 to do serial loopback on the corresponding channel.* The high speed serial outputs will not be active.

*This test mode can also be set using TESTEN_xx in place of LOOPENB_xx. In that case, Test Mode must be set to 00000.

Parallel Loopback at the SERDES Boundary

In this parallel loopback differential data are received at the HDINP_xx and HDINN_xx pins and are retransmitted at the HDOUTP_xx and HDOUTN_xx pins. The loopback path is at the interface between the SERDES blocks and the MUX and DEMUX blocks and uses the parallel 10-bit buses at these interfaces (see Figure 32b). The loopback connection is made such that the input signals to the TX SERDES block is the same as the output signals from the RX SERDES block. In this parallel loopback mode, the MRWDxx[39:0] signal lines remain active and the TWDxx[31:0], TCOMMAxx[3:0] and TBIT9xx[3:0] signal lines are not used. This mode is normally used for tests where serial test data is received from and transmitted to either test equipment or via a serial backplane to a remote card and is the basic loopback path shown earlier in Figure 32(b).

The data rate selection bits TXHR and RXHR in the channel configuration registers must be configured to carry the same value. Also, the 8b/10b encoder and decoder are excluded from the loopback path by setting the 8b10bT and 8b10bR configuration bits to 0. Table 21 and Table 22 illustrate the control interface register configuration for the parallel loopback.

Table 21. Parallel Loopback at the SERDES Boundary Configuration Bit Definitions

Register Address (Hex)	Bit Value	Bit Name	Comments
30022, 30032, 30122, 30132	Bit 0 = 0 or 1	TXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 7 = 0	8b10bT	Set to 0 The 8b/10b encoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to 0.
30023, 30033, 30123, 30133	Bit 0 = 0 or 1	RXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 3 = 0	8b10bR	Set to 0.The 8b/10b decoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to 0.
30005, 30105	Bit 7 = 1	GTESTEN	SET to 1 if the loopback is done globally on both channels.
30026, 30036, 30126, 30136	Bits[4:0]	Testmode	Set to 00001

Table 22. Parallel Loopback at the SERDES Boundary Configuration Bit Definitions for the ORT82G5

Register Address (Hex)	Bit Value	Bit Name	Comments
30002, 30012, 30022, 30032, 30102, 30112, 30122, 30132	Bit 0 = 0 or 1	TXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 7 = 0	8b10bT	Set to 0 The 8b/10b encoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to 0.
30003, 30013, 30023, 30033, 30103, 30113, 30123, 30133	Bit 0 = 0 or 1	RXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 3 = 0	8b10bR	Set to 0.The 8b/10b decoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to 0.
30005, 30105	Bit 7 = 1	GTESTEN	SET to 1 if the loopback is done globally on all four channels.
30006, 30016, 30026, 30036, 30106, 30116, 30126, 30136	Bits[4:0]	Testmode	Set to 00001

Table 28. ORT42G5 Memory Map (Continued)

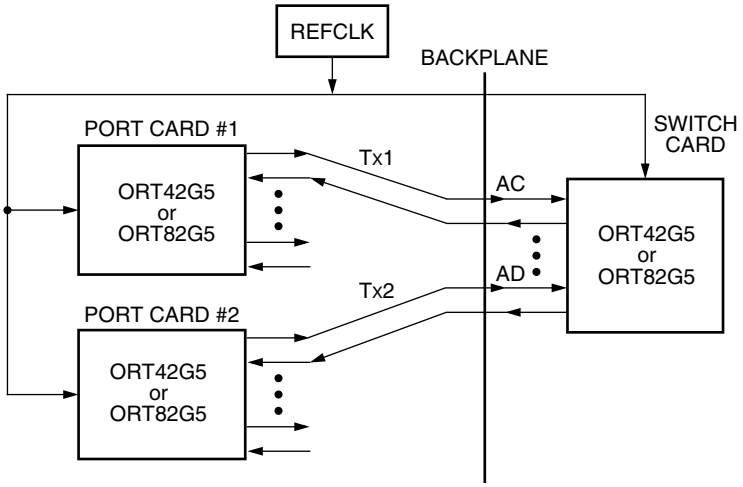
(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Common Transmit and Receive Channel Configuration Registers (Read/Write), xx = [AC, AD, BC or BD]				
30024 - AC 30034 - AD 30124 - BC 30134 - BD	[0]	Reserved	See Bit Desc.	Reserved, must be 0. Set to 0 on device reset.
	[1]	MASK_xx		Transmit and Receive Alarm Mask Bit, Channel xx. When MASK_xx = 1, the transmit and receive alarms of a channel are prevented from generating an interrupt (i.e., they are masked or disabled). The MASK_xx bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK_xx = 1 on device reset.
	[2]	SWRST_xx		Transmit and Receive Software Reset Bit, Channel xx. When SWRST_ss = 1, this bit provides the same function as the hardware reset, except that all configuration register settings are unaltered. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. SWRST = 0 on device reset.
	[3:6]	Not used		Not used
	[7]	TESTEN_xx		Transmit and Receive Test Enable Bit, Channel xx. When TESTEN_xx = 1, the transmit and receive sections are placed in test mode. The TestMode_[A:B][4:0] bits in the Global Control Registers specify the particular test, and must also be set. Note: When the global test enable bit GTESTEN_[A:B] = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN_[A:B] = 1, all channels in a block are set to test mode regardless of their TESTEN setting. TESTEN_xx = 0 on device reset.
SERDES Global Control Registers (Read Write) - Act on Both Channels in SERDES Block A or SERDES Block B.				
30005 - A 30105 - B	[0]	Reserved	See Bit Desc.	Reserved, must be 0. Set to 0 on device reset.
	[1]	GMASK_[A:B]		Global Mask. When GMASK_[A:B] = 1, the transmit and receive alarms of both channels in the SERDES block are prevented from generating an interrupt (i.e., they are masked or disabled). The GMASK_[A:B] bit overrides the individual MASK_xx bits. GMASK_[A:B] = 1 on device reset.
	[2]	GSWRST_[A:B]		Software reset bit. The GSWRST_[A:B] bit provides the same function as the hardware reset for the transmit and receive sections of both channels, except that the device configuration settings are not affected when GSWRST_[A:B] is asserted. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. The GSWRST_[A:B] bit overrides the individual SWRST_xx bits. GSWRST_[A:B] = 0 on device reset.
	[3]	GPWRDNT_[A:B]		Powerdown Transmit Function. When GPWRDNT_[A:B] = 1, sections of the transmit hardware for both channels are powered down to conserve power. The GPWRDNT_[A:B] bit overrides the individual PWRDNT_xx bits. GPWRDNT_[A:B] = 0 on device reset.
	[4]	GPWRDNR_[A:B]		Powerdown Receive Function. When GPWRDNR_[A:B] = 1, sections of the receive hardware for both channels are powered down to conserve power. The GPWRDNR_[A:B] bit overrides the individual PWRDNR_xx bits. GPWRDNR_[A:B] = 0 on device reset.
	[5]	Reserved		Reserved, 1 on device reset.
	[6]	Not used		Not used
	[7]	GTESTEN_[A:B]		Test Enable Control. When GTESTEN_[A:B] = 1, the transmit and receive sections of both channels are placed in test mode. The GTESTEN_[A:B] bit overrides the individual TESTEN_xx bits. GTESTEN_[A:B] = 0 on device reset.
30006 - A 30106 - B	[0:4]	TestMode[A:B]	00	Test Mode - See Test Mode section for settings
	[5]	Not used		Not used
	[6:7]	Reserved		Reserved

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30810 - Ax 30910 - Bx	[0]]	—	00	Reserved for future use
	[1]	—		Reserved for future use
	[2]	DOWDALIGN_xC		Word Realign Bit. When DOWDALIGN_xC transitions from 0 to 1, the receiver realigns on the next comma character for Channel xC. NOWDALIGN_xC=0 on device reset.
	[3]	DOWDALIGN_xC		Word Realign Bit. When DOWDALIGN_xC transitions from 0 to 1, the receiver realigns on the next comma character for Channel xC. NOWDALIGN_xC=0 on device reset.
	[4]	—		Reserved for future use. Set to zero.
	[5]	—		Reserved for future use. Set to zero.
	[6]	FMPU_STR_EN _xC		Enable multi-channel alignment for Channel xC. When FMPU_STR_EN _xC = 0, Channel xC is not part of a multi-channel alignment group When FMPU_STR_EN _xC = 1, Channel xC is part of a twin channel alignment (SERDES block A or B) or quad channel alignment (both SERDES blocks) group.
	[7]	FMPU_STR_EN _xD		Enable multi-channel alignment for Channel xD. When FMPU_STR_EN _xD = 0, Channel xD is not part of a multi-channel alignment group When FMPU_STR_EN _xD = 1, Channel xD is part of a twin channel alignment (SERDES block A or B) or quad channel alignment (both SERDES blocks) group.
30811 - Ax 30911 - Bx	[0:7]	FMPU_SYNMODE_ [A:B]	00	Sync mode for block [A:B] 00000000 = No channel alignment 00001010 = Twin channel alignment, SERDES block [A:B] 00001111 = Quad channel alignment (both SERDES blocks)
30820 - Ax 30920 - Bx	[0]	—	00	Reserved for future use.
	[1]	—		Reserved for future use.
	[2]	FMPU_RESYNC1_xC		Resync a Single Channel. When FMPU_RESYNC1_xC transitions from 0 to 1, the corresponding channel xC is resynchronized (the write and read pointers are reset). FMPU_STR_EN_xC=0 on device reset.
	[3]	FMPU_RESYNC1_xD		Resync a Single Channel. When FMPU_RESYNC1_xD transitions from 0 to 1, the corresponding channel xD is resynchronized (the write and read pointers are reset). FMPU_STR_EN_xD=0 on device reset.
	[4]	—		Reserved for future use.
	[5]	FMPU_RESYNC2[A:B]		Resync a Twin-Channel Group. When FMPU_RESYNC2[A:B] transitions from a 0 to a 1, the corresponding twin-channel group is resynchronized. FMPU_RESYNC2[A:B]=0 on device reset.
	[6]	—		Reserved for future use.
	[7]	XAUI_MODE[A:B]		Controls use of XAUI link state machine in place of Fibre-Channel state machine. When XAUI_MODE[A:B]=1, both channels in the SERDES block enable their XAUI link state machines. (LINKSM_xx bits are ignored). XAUI_MODE[A:B]=0 on device reset.
30821 - A 30921 - B	[0]	NOCHALGN [A:B]	00	Bypass channel alignment. NOCHALGN [A:B] =1 causes bypassing of multi-channel alignment FIFOs for the corresponding SERDES quad. NOCHALGN [A:B] =0 on device reset.
	[1:7]	—		Reserved for future use.

The disadvantage with this scheme is the fact that it is difficult to distribute a 156 MHz reference clock across a backplane. This may require expensive clock driver chips on the board to drive clocks to different destinations within the specified jitter limits for the reference clock.

Figure 38. Distributed Reference Clock to Rx And Tx Devices



Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

The ORCA Series 4 FPSCs include circuitry designed to protect the chips from damaging substrate injection currents and to prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_{STG}	– 65	150	°C
Power Supply Voltage with Respect to Ground	V_{DD33}	– 0.3	4.2	V
	V_{DDIO}	– 0.3	4.2	V
	V_{DD15}, V_{DD_ANA}, V_{DDGB}	—	2.0	V
Input Signal with Respect to Ground	V_{IN}	V_{SS} – 0.3	V_{DD}IO + 0.3	V
Signal Applied to High-impedance Output	—	V_{SS} – 0.3	V_{DD}IO + 0.3	V
Maximum Package Body (Soldering) Temperature	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage with Respect to Ground[1]	V_{DD33}	3.0	3.6	V
	V_{DD15}	1.425	1.575	V
Input Voltages	V_{IN}	V_{SS} – 0.3	V_{DDIO} + 0.3	V
Junction Temperature	T_J	– 40	125	°C
SERDES Supply Voltage	V_{DD_ANA}, V_{DDGB}	1.425	1.575	V
SERDES CML I/O Supply Voltage	V_{DDIB}, V_{DDOB}	1.425	1.89	V

1. For FPGA Recommended Operating Conditions and Electrical Characteristics, see the Recommended Operating Conditions and Electrical Characteristics tables in the ORCA Series 4 FPGA data sheet (OR4E04) and the ORCA Series 4 I/O Buffer Technical Note. FPSC Standby Currents (IDDSB15 and IDDSB33) are tested with the Embedded Core in the powered down state.

SERDES Electrical and Timing Characteristics

Table 31. Absolute Maximum Ratings

Parameter	Conditions	Max.[1]	Units
ORT82G5 Power Dissipation	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 1.25 Gbit/s	195	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 2.50 Gbit/s	210	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 3.125 Gbit/s	225	mW
	8b/10b Encoder/Decoder (per Channel)	50	mW
ORT42G5 Power Dissipation	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 1.25 Gbit/s	265	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 2.50 Gbit/s	275	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 3.125 Gbit/s	295	mW
	8b/10b Encoder/Decoder (per Channel)	50	mW

1. With all channels operating, 1.575V supply.

Pin Descriptions

This section describes the pins found on the Series 4 FPGAs. Any pin not described in this table is a user-programmable I/O. During configuration, the user-programmable I/Os are 3-stated with an internal pull-up resistor. If any pin is not used (or not bonded to a package pin), it is also 3-stated with an internal pull-up resistor after configuration. The pin descriptions in Table and throughout this data sheet show active-low signals with an overscore. The package pinout tables that follow, show this as a signal ending with _N. For example $\overline{\text{LDC}}$ and LDC_N are equivalent.

Table 40. Pin Descriptions

Symbol	I/O	Description
Dedicated Pins		
VDD33	—	3.3V positive power supply. This power supply is used for 3.3V configuration RAMs and internal PLLs. When using PLLs, this power supply should be well isolated from all other power supplies on the board for proper operation.
VDD15	—	1.5V positive power supply for internal logic.
VDDIO	—	Positive power supply used by I/O banks.
VSS	—	Ground.
PTEMP	I	Temperature sensing diode pin. Dedicated input.
$\overline{\text{RESET}}$	I	During configuration, $\overline{\text{RESET}}$ forces the restart of configuration and a pull-up is enabled. After configuration, $\overline{\text{RESET}}$ can be used as a general FPGA input or as a direct input, which causes all PLC latches/FFs to be asynchronously set/reset.
CCLK	O	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in.
	I	In the slave or readback after configuration, CCLK is input synchronous with the data on DIN or D[7:0]. CCLK is an output for daisy-chain operation when the lead device is in master, peripheral, or system bus modes.
DONE	I	As an input, a low level on DONE delays FPGA start-up after configuration.[1]
	O	As an active-high, open-drain output, a high level on this signal indicates that configuration is complete. DONE has an optional pull-up resistor.
PRGRM	I	$\overline{\text{PRGRM}}$ is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up.
RD_CFG	I	This pin must be held high during device initialization until the $\overline{\text{INIT}}$ pin goes high. This pin always has an active pull-up. During configuration, $\overline{\text{RD\_CFG}}$ is an active-low input that activates the TS_ALL function and 3-states all of the I/O. After configuration, $\overline{\text{RD\_CFG}}$ can be selected (via a bit stream option) to activate the TS_ALL function as described above, or, if readback is enabled via a bit stream option, a high-to-low transition on $\overline{\text{RD\_CFG}}$ will initiate readback of the configuration data, including PFU output states, starting with frame address 0.
RD_DATA/TDO	O	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary-scan, TDO is test data out.
$\overline{\text{CFG\_IRQ}}$/MPI_IRQ	O	During JTAG, slave, master, and asynchronous peripheral configuration assertion on this $\overline{\text{CFG\_IRQ}}$ (active-low) indicates an error or errors for block RAM or FPSC initialization. MPI active-low interrupt request output, when the MPI is used.
LVDS_R	—	Reference resistor connection for controlled impedance termination of Series 4 FPGA LVDS inputs.
Special-Purpose Pins		
M[3:0]	I	During powerup and initialization, M0—M3 are used to select the configuration mode with their values latched on the rising edge of $\overline{\text{INIT}}$. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O.[1]
PLL_CK[0:7][TC]	I	Semi-dedicated PLL clock pins. During configuration they are 3-stated with a pull up.
	I/O	These pins are user-programmable I/O pins if not used by PLLs after configuration.
P[TBLR]CLK[1:0][TC]	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.
	I/O	After configuration these pins are user programmable I/O, if not used for clock inputs.

Table 41. FPSC Function Pin Descriptions (Continued)

Symbol	I/O	Description
HDOUTP_AB (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad A, channel B.
HDOUTN_AC	O	High-speed CML transmit data output – SERDES quad A, channel C.
HDOUTP_AC	O	High-speed CML transmit data output – SERDES quad A, channel C.
HDOUTN_AD	O	High-speed CML transmit data output – SERDES quad A, channel D.
HDOUTP_AD	O	High-speed CML transmit data output – SERDES quad A, channel D.
HDOUTN_BA (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad B, channel A.
HDOUTP_BA (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad B, channel A.
HDOUTN_BB (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad B, channel B.
HDOUTP_BB (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad B, channel B.
HDOUTN_BC	O	High-speed CML transmit data output – SERDES quad B, channel C.
HDOUTP_BC	O	High-speed CML transmit data output – SERDES quad B, channel C.
HDOUTN_BD	O	High-speed CML transmit data output – SERDES quad B, channel D.
HDOUTP_BD	O	High-speed CML transmit data output – SERDES quad B, channel D.
Power and Ground		
VDDIB_AA (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_AB (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_AC	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_AD	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_BA (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_BB (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_BC	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDIB_BD	—	1.8V/1.5V power supply for high-speed serial input buffers.
VDDOB_AA (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_AB (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_AC	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_AD	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_BA (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_BB (ORT82G5 only)	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_BC	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDOB_BD	—	1.8V/1.5V power supply for high-speed serial output buffers.
VDDGB_A	—	1.5V guard band power supply.
VDDGB_B	—	1.5V guard band power supply.
VDD_ANA	—	1.5V power supply for SERDES analog receive and transmit circuitry.

1. Should be externally connected on board to 3.3V pull-up resistor.

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
D4	0 (TL)	6	IO	PT2C	PLL_CK1T/PPLL	L83T
A3	-	-	O	PCFG_MPI_IRQ	CFG_IRQ_N/MPI_IRQ_N	-
B3	-	-	IO	PCCLK	CCLK	-
F7	-	-	VDD15	VDD15	-	-
C3	-	-	IO	PDONE	DONE	-
E3	-	-	VDD33	VDD33	-	-
P15	-	-	VDD15	VDD15	-	-
R6	-	-	VDD15	VDD15	-	-
R15	-	-	VDD15	VDD15	-	-
T4	-	-	VDD15	VDD15	-	-
W19	-	-	VDD15	VDD15	-	-
Y3	-	-	VDD15	VDD15	-	-
Y19	-	-	VDD15	VDD15	-	-
Y20	-	-	VDD15	VDD15	-	-
T15	-	-	VDD15	VDD15	-	-
T16	-	-	VDD15	VDD15	-	-
U4	-	-	VDD15	VDD15	-	-
T12	-	-	VDD15	VDD15	-	-
T13	-	-	VDD15	VDD15	-	-
T14	-	-	VDD15	VDD15	-	-
T6	-	-	VDD15	VDD15	-	-
T7	-	-	VDD15	VDD15	-	-
T10	-	-	VDD15	VDD15	-	-
T11	-	-	VDD15	VDD15	-	-
G5	0 (TL)	-	VDDIO0	VDDIO0	-	-
H5	0 (TL)	-	VDDIO0	VDDIO0	-	-
J5	0 (TL)	-	VDDIO0	VDDIO0	-	-
V17	5 (BC)	-	VDDIO5	VDDIO5	-	-
W17	5 (BC)	-	VDDIO5	VDDIO5	-	-
W18	5 (BC)	-	VDDIO5	VDDIO5	-	-
M6	7 (CL)	-	VDDIO7	VDDIO7	-	-
N6	7 (CL)	-	VDDIO7	VDDIO7	-	-
U5	-	-	VDD15	VDD15	-	-
U17	-	-	VDD15	VDD15	-	-
V5	-	-	VDD15	VDD15	-	-
V18	-	-	VDD15	VDD15	-	-
R18	-	-	VSS	VSS	-	-
R19	-	-	VSS	VSS	-	-
T19	-	-	VSS	VSS	-	-
U19	-	-	VSS	VSS	-	-
U20	-	-	VSS	VSS	-	-
V19	-	-	VSS	VSS	-	-
V20	-	-	VSS	VSS	-	-
W20	-	-	VSS	VSS	-	-

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
Y20	—	—	VSS	VSS	—	—
AG2	7 (CL)	8	IO	PL31B	—	L34C_D0
AH1	7 (CL)	8	IO	PL31A	—	L34T_D0
AF3	6 (BL)	1	IO	PL32D	D8	L1C_A0
AG3	6 (BL)	1	IO	PL32C	VREF_6_01	L1T_A0
AL7	6 (BL)	—	VDDIO6	VDDIO6	—	—
AE4	6 (BL)	1	IO	PL32B	—	L2C_A0
AF4	6 (BL)	1	IO	PL32A	—	L2T_A0
AE5	6 (BL)	1	IO	PL33D	D9	L3C_A0
AF5	6 (BL)	1	IO	PL33C	D10	L3T_A0
R21	—	—	VSS	VSS	—	—
AJ1	6 (BL)	2	IO	PL34D	—	L4C_D0
AH2	6 (BL)	2	IO	PL34C	VREF_6_02	L4T_D0
AM5	6 (BL)	—	VDDIO6	VDDIO6	—	—
AK1	6 (BL)	2	IO	PL34B	—	L5C_D0
AJ2	6 (BL)	2	IO	PL34A	—	L5T_D0
R22	—	—	VSS	VSS	—	—
AG4	6 (BL)	3	IO	PL35B	D11	L6C_D0
AH3	6 (BL)	3	IO	PL35A	D12	L6T_D0
AL1	6 (BL)	3	IO	PL36D	—	L7C_D0
AK2	6 (BL)	3	IO	PL36C	—	L7T_D0
AM9	6 (BL)	—	VDDIO6	VDDIO6	—	—
AM1	6 (BL)	3	IO	PL36B	VREF_6_03	L8C_D0
AL2	6 (BL)	3	IO	PL36A	D13	L8T_D0
AJ3	6 (BL)	4	IO	PL37D	—	—
T16	—	—	VSS	VSS	—	—
AJ4	6 (BL)	4	IO	PL37B	—	L9C_A0
AH4	6 (BL)	4	IO	PL37A	VREF_6_04	L9T_A0
AK3	6 (BL)	4	IO	PL38C	—	—
AN2	6 (BL)	—	VDDIO6	VDDIO6	—	—
AG5	6 (BL)	4	IO	PL38B	—	L10C_A0
AH5	6 (BL)	4	IO	PL38A	—	L10T_A0
AN1	6 (BL)	4	IO	PL39D	PLL_CK7C/HPPLL	L11C_D0
AM2	6 (BL)	4	IO	PL39C	PLL_CK7T/HPPLL	L11T_D0
T17	—	—	VSS	VSS	—	—
AL3	6 (BL)	4	IO	PL39B	—	L12C_D0
AK4	6 (BL)	4	IO	PL39A	—	L12T_D0
T18	—	—	VSS	VSS	—	—
AM3	—	—	I	PTEMP	PTEMP	—
AN3	6 (BL)	—	VDDIO6	VDDIO6	—	—
AJ5	—	—	IO	LVDS_R	LVDS_R	—
AL4	—	—	VDD33	VDD33	—	—
T19	—	—	VSS	VSS	—	—
AK5	—	—	VDD33	VDD33	—	—

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AA32	—	—	VDD_ANA	VDD_ANA	—	—
AF30	—	—	—	REXT_B	—	—
AF31	—	—	—	REXTN_B	—	—
AE30	—	—	I	REFCLKN_B	—	—
AE31	—	—	I	REFCLKP_B	—	—
AB32	—	—	VSS	VSS	—	—
AD30	—	—	VDDIB	VDDIB_BA	—	—
AD32	—	—	VDD_ANA	VDD_ANA	—	—
AF33	—	—	I	HDINN_BA	—	—
AC32	—	—	VSS	VSS	—	—
AF34	—	—	I	HDINP_BA	—	—
AE32	—	—	VDD_ANA	VDD_ANA	—	—
AD31	—	—	VSS	VSS	—	—
K32	—	—	VDD_ANA	VDD_ANA	—	—
AE33	—	—	O	HDOUTN_BA	—	—
AF32	—	—	VSS	VSS	—	—
AE34	—	—	O	HDOUTP_BA	—	—
AC30	—	—	VDDOB	VDDOB_BA	—	—
AG30	—	—	VSS	VSS	—	—
AB30	—	—	VDDIB	VDDIB_BB	—	—
AD33	—	—	I	HDINN_BB	—	—
AG31	—	—	VSS	VSS	—	—
AD34	—	—	I	HDINP_BB	—	—
AC31	—	—	VSS	VSS	—	—
AC33	—	—	O	HDOUTN_BB	—	—
AG32	—	—	VSS	VSS	—	—
AC34	—	—	O	HDOUTP_BB	—	—
AB31	—	—	VDDOB	VDDOB_BB	—	—
AG33	—	—	VSS	VSS	—	—
AA30	—	—	VDDIB	VDDIB_BC	—	—
AB33	—	—	I	HDINN_BC	—	—
AG34	—	—	VSS	VSS	—	—
AB34	—	—	I	HDINP_BC	—	—
AA31	—	—	VSS	VSS	—	—
Y30	—	—	VDDOB	VDDOB_BC	—	—
AA33	—	—	O	HDOUTN_BC	—	—
H30	—	—	VSS	VSS	—	—
AA34	—	—	O	HDOUTP_BC	—	—
Y31	—	—	VDDOB	VDDOB_BC	—	—
H31	—	—	VSS	VSS	—	—
W30	—	—	VDDIB	VDDIB_BD	—	—
Y33	—	—	I	HDINN_BD	—	—
H32	—	—	VSS	VSS	—	—
Y34	—	—	I	HDINP_BD	—	—

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
W31	—	—	VSS	VSS	—	—
V30	—	—	VDDOB	VDDOB_BD	—	—
W33	—	—	O	HDOUTN_BD	—	—
H33	—	—	VSS	VSS	—	—
W34	—	—	O	HDOUTP_BD	—	—
V31	—	—	VDDOB	VDDOB_BD	—	—
H34	—	—	VSS	VSS	—	—
J32	—	—	VSS	VSS	—	—
U31	—	—	VDDOB	VDDOB_AD	—	—
T34	—	—	O	HDOUTP_AD	—	—
M32	—	—	VSS	VSS	—	—
T33	—	—	O	HDOUTN_AD	—	—
U30	—	—	VDDOB	VDDOB_AD	—	—
T31	—	—	VSS	VSS	—	—
R34	—	—	I	HDINP_AD	—	—
N32	—	—	VSS	VSS	—	—
R33	—	—	I	HDINN_AD	—	—
T30	—	—	VDDIB	VDDIB_AD	—	—
U32	—	—	VSS	VSS	—	—
R31	—	—	VDDOB	VDDOB_AC	—	—
P34	—	—	O	HDOUTP_AC	—	—
U33	—	—	VSS	VSS	—	—
P33	—	—	O	HDOUTN_AC	—	—
R30	—	—	VDDOB	VDDOB_AC	—	—
P31	—	—	VSS	VSS	—	—
N34	—	—	I	HDINP_AC	—	—
U34	—	—	VSS	VSS	—	—
N33	—	—	I	HDINN_AC	—	—
P30	—	—	VDDIB	VDDIB_AC	—	—
V32	—	—	VSS	VSS	—	—
M34	—	—	O	HDOUTP_AB	—	—
V33	—	—	VSS	VSS	—	—
M33	—	—	O	HDOUTN_AB	—	—
N31	—	—	VDDOB	VDDOB_AB	—	—
M31	—	—	VSS	VSS	—	—
L34	—	—	I	HDINP_AB	—	—
V34	—	—	VSS	VSS	—	—
L33	—	—	I	HDINN_AB	—	—
N30	—	—	VDDIB	VDDIB_AB	—	—
K34	—	—	O	HDOUTP_AA	—	—
K33	—	—	O	HDOUTN_AA	—	—
M30	—	—	VDDOB	VDDOB_AA	—	—
L32	—	—	VDD_ANA	VDD_ANA	—	—
L31	—	—	VSS	VSS	—	—

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
P32	—	—	VDD_ANA	VDD_ANA	—	—
J34	—	—	I	HDINP_AA	—	—
J33	—	—	I	HDINN_AA	—	—
R32	—	—	VDD_ANA	VDD_ANA	—	—
L30	—	—	VDDIB	VDDIB_AA	—	—
K31	—	—	—	REFCLKP_A	—	—
K30	—	—	—	REFCLKN_A	—	—
J31	—	—	O	REXTN_A	—	—
J30	—	—	O	REXT_A	—	—
Y32	—	—	VDD_ANA	VDD_ANA	—	—
G34	—	—	VDDGB_A	VDDGB_A	—	—
G33	—	—	VSS	VSS	—	—
G32	—	—	O	ATMOUT_A (no connect)	—	—
G31	—	—	I	PRESERVE01 (no connect)	—	—
F33	—	—	I	PRESERVE02 (no connect)	—	—
G30	—	—	I	PRESERVE03 (no connect)	—	—
F31	—	—	O	PSYS_RSSIG_ALL	—	—
F30	—	—	I	PSYS_DOBISTN	—	—
E31	—	—	VDD33	VDD33	—	—
AB17	—	—	VDD15	VDD15	—	—
AB18	—	—	VDD15	VDD15	—	—
D32	—	—	I	PBIST_TEST_ENN	—	—
E30	—	—	I	PLOOP_TEST_ENN	—	—
AB19	—	—	VDD15	VDD15	—	—
D31	—	—	I	PASB_PDN	—	—
C32	—	—	I	PMP_TESTCLK	—	—
C31	—	—	VDD33	VDD33	—	—
AJ32	—	—	VDD15	VDD15	—	—
B32	—	—	I	PASB_RESETN	—	—
A33	—	—	I	PASB_TRISTN	—	—
B31	—	—	I	PMP_TESTCLK_ENN	—	—
A32	—	—	I	PASB_TESTCLK	—	—
AK32	—	—	VDD15	VDD15	—	—
AB21	—	—	VSS	VSS	—	—
A31	—	—	VDD33	VDD33	—	—
B30	1 (TC)	7	IO	PT36D	—	—
AB22	—	—	VSS	VSS	—	—
C30	1 (TC)	7	IO	PT36B	—	—
D30	1 (TC)	7	IO	PT35D	—	—
B13	1 (TC)	—	VDDIO1	VDDIO1	—	—
E29	1 (TC)	7	IO	PT35B	—	—
E28	1 (TC)	7	IO	PT34D	VREF_1_07	—
AN33	—	—	VSS	Vss	—	—
D29	1 (TC)	8	IO	PT34B	—	—

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
U21	—	—	VDD15	VDD15	—	—
U22	—	—	VDD15	VDD15	—	—
V13	—	—	VDD15	VDD15	—	—
V14	—	—	VDD15	VDD15	—	—
V15	—	—	VDD15	VDD15	—	—
V20	—	—	VDD15	VDD15	—	—
V21	—	—	VDD15	VDD15	—	—
V22	—	—	VDD15	VDD15	—	—
W13	—	—	VDD15	VDD15	—	—
W14	—	—	VDD15	VDD15	—	—
W15	—	—	VDD15	VDD15	—	—
W20	—	—	VDD15	VDD15	—	—
W21	—	—	VDD15	VDD15	—	—
W22	—	—	VDD15	VDD15	—	—
Y16	—	—	VDD15	VDD15	—	—
Y17	—	—	VDD15	VDD15	—	—
Y18	—	—	VDD15	VDD15	—	—
Y19	—	—	VDD15	VDD15	—	—
T32	—	—	NC	NC	—	—
W32	—	—	NC	NC	—	—

Package Thermal Characteristics Summary

There are three thermal parameters that are in common use: Θ_{JA}, ψ_{JC}, and Θ_{JC}. It should be noted that all the parameters are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

Θ_{JA}

This is the thermal resistance from junction to ambient (theta-JA, R-theta, etc.):

$$\Theta_{JA} = \frac{T_J - T_A}{Q} \quad (1)$$

where T_J is the junction temperature, T_A, is the ambient air temperature, and Q is the chip power.

Experimentally, Θ_{JA} is determined when a special thermal test die is assembled into the package of interest, and the part is mounted on the thermal test board. The diodes on the test chip are separately calibrated in an oven. The package/board is placed either in a JEDEC natural convection box or in the wind tunnel, the latter for forced convection measurements. A controlled amount of power (Q) is dissipated in the test chip's heater resistor, the chip's temperature (T_J) is determined by the forward drop on the diodes, and the ambient temperature (T_A) is noted. Note that Θ_{JA} is expressed in units of °C/W.

ψ_{JC}

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance and it is defined by:

$$\psi_{JC} = \frac{T_J - T_C}{Q} \quad (2)$$

Industrial[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT42G5	ORT42G5-2BM484I	2	PBGAM	484	I
	ORT42G5-1BM484I	1	PBGAM	484	I
ORT82G5	ORT82G5-2F680I	2	PBGAM (No Heat Spreader)	680	I
	ORT82G5-1F680I	1	PBGAM (No Heat Spreader)	680	I
	ORT82G5-2BM680I[2]	2	PBGAM (With Heat Spreader)	680	I
	ORT82G5-1BM680I[2]	1	PBGAM (With Heat Spreader)	680	I

1. For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only.
2. BM680 package was converted to F680 via PCN#09A-08.

Lead-Free Packaging

Commercial[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT42G5	ORT42G5-3BMN484C	3	Lead-Free PBGAM	484	C
	ORT42G5-2BMN484C	2	Lead-Free PBGAM	484	C
	ORT42G5-1BMN484C	1	Lead-Free PBGAM	484	C
ORT82G5	ORT82G5-3FN680C	3	Lead-Free FPGA (No Heat Spreader)[2]	680	C
	ORT82G5-2FN680C	2	Lead-Free FPGA (No Heat Spreader)[2]	680	C
	ORT82G5-1FN680C	1	Lead-Free FPGA (No Heat Spreader)[2]	680	C

1. For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster.
2. Refer to the Thermal Management document at www.latticesemi.com for Θ_{JA} and Θ_{JC} information.

Industrial[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT42G5	ORT42G5-2BMN484I	2	Lead-Free PBGAM	484	I
	ORT42G5-1BMN484I	1	Lead-Free PBGAM	484	I
ORT82G5	ORT82G5-2FN680I	2	Lead-Free FPGA (No Heat Spreader)[2]	680	I
	ORT82G5-1FN680I	1	Lead-Free FPGA (No Heat Spreader)[2]	680	I

1. For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster.
2. Refer to the Thermal Management document at www.latticesemi.com for Θ_{JA} and Θ_{JC} information.