Lattice Semiconductor Corporation - ORT42G5-3BMN484C Datasheet

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	204
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort42g5-3bmn484c

Dual Port RAMs

In addition to the backplane interface blocks, there are two independent memory blocks in the ASB. Each memory block has a capacity of 4k words by 36 bits. It has one read port, one write port, and four byte-write-enable (active-low) signals. The read data from the memory block is registered so that it works as a pipelined synchronous memory block.

FPSC Configuration

Configuration of the ORT42G5 and ORT82G5 occurs in two stages: FPGA bitstream configuration and embedded core setup.

Prior to becoming operational, the FPGA goes through a sequence of states, including power up, initialization, configuration, start-up, and operation. The FPGA logic is configured by standard FPGA bit stream configuration means as discussed in the Series 4 FPGA data sheet.

After the FPGA configuration is complete, the options for the embedded core are set based on the contents of registers that are accessed through the FPGA system bus.

The system bus itself can be driven by an external PowerPC compliant microprocessor via the MPI block or via a user master interface in FPGA logic. A simple IP block that drives the system by using the user register interface and very little FPGA logic is available in the MPI/System Bus Technical Note. This IP block sets up the embedded core via a state machine and allows the ORT42G5 and ORT82G5 to work in an independent system without an external microprocessor interface.

Backplane Transceiver Core Detailed Description

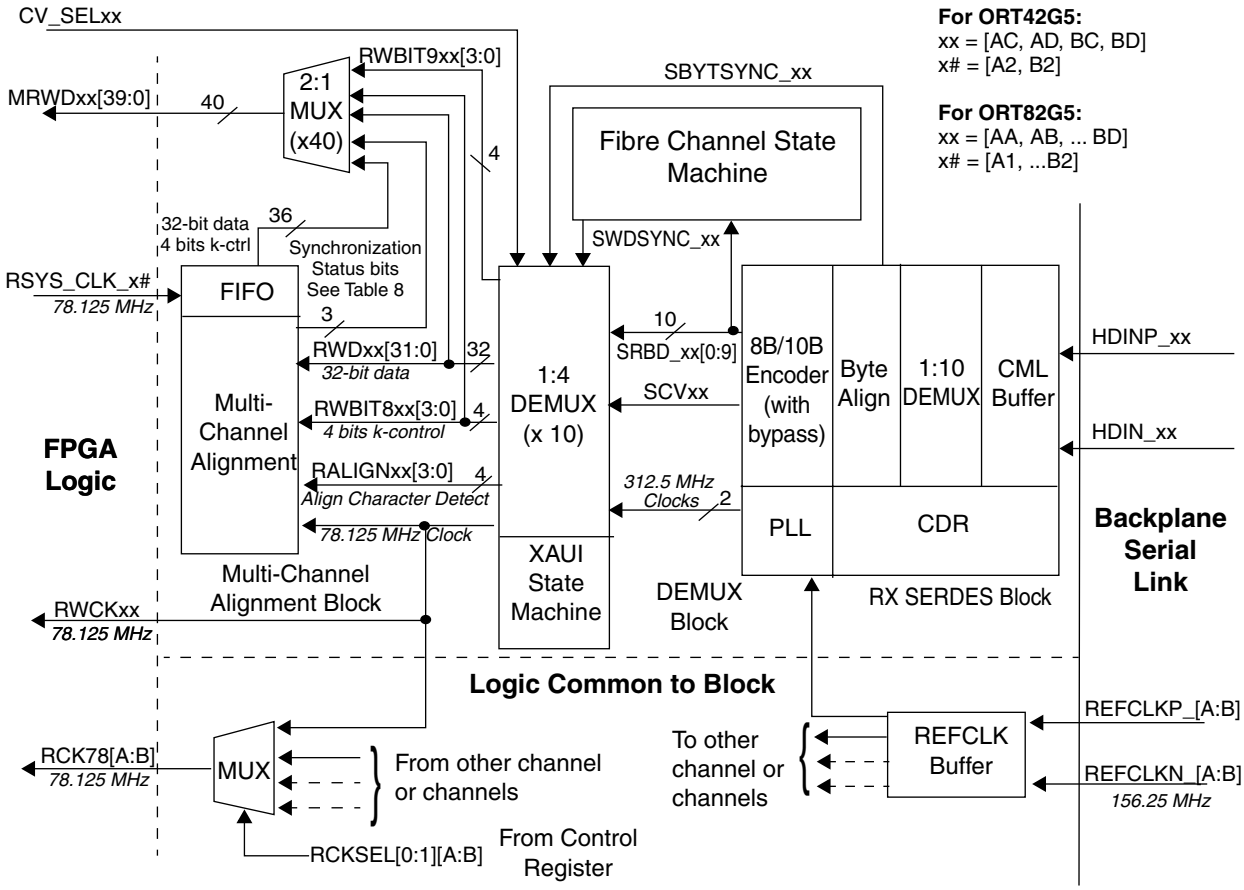
The following sections describe the various logic blocks in the Embedded Core portion of the FPSC. The FPGA section of the FPSC is identical to an ORCA OR4E04 FPGA except that the pads on one edge of the FPGA chip are replaced by the Embedded Core. For a detailed description of the programmable logic functions, please see the ORCA Series 4 FPGA Data Sheet and related application and technical notes.

The major functional blocks in the Embedded Core include:

- Two SERializer-DESerializer (SERDES) blocks and Clock and Data Recovery (CDR) circuitry
- 8b/10b encoder/decoders
- Transmit pre-emphasis circuitry
- 4-to-1 multiplexers (MUX) and 1-to-4 demultiplexers (DEMUX)
- Fibre channel synchronization state machine
- XAUI link alignment state machine
- Alignment FIFOs
- Embedded 4K x 36 RAM blocks (independent from transceiver logic).

A top level block diagram of the Embedded Core Logic is shown in Figure 2. The Embedded RAM blocks are not shown. The external pins for the Embedded Core are listed later in this data sheet in Table 41 and the signals at the Transceiver Embedded Core/FPGA interface for the ORT42G5 are listed in Table 8, Table 9 and Table 11; and for the ORT82G5, in Table 8, Table 10 and Table 12.

Figure 6. Basic Logic Blocks, Receive Path, Single Channel (Typical Reference Clock Frequency)



Each channel provides its own received clock, received data and K-character detect signals to the FPGA logic. Incoming data from multiple channels can be aligned using comma (/K/) characters or /A/ character (as specified either in Fibre Channel specifications or in IEEE 802.3ae for XAUI based interfaces). If the 8b/10b decoders are bypassed, then 40-bit data streams are passed to the FPGA logic. No channel alignment can be done in this 8b/10b bypass mode.

Detailed descriptions of data synchronization, of the SERDES, DEMUX and Multi-Channel Alignment blocks and of the Fibre Channel and XAUI state machines are given in following sections. Receive clock distribution is described in a later section of this data sheet.

Synchronization

The SERDES RX logic performs four levels of synchronization on the incoming serial data stream. Each level builds upon the previous, providing first bit, then byte (character), then channel (32-bit word), and finally multi-channel alignment. Each step is described functionally in the following paragraphs. The details of the logical implementations are described in subsequent sections.

Bit alignment is the task of the Clock/Data Recovery (CDR) block. This block utilizes a PLL that locks to the transitions in the incoming high-speed serial data stream, and outputs the extracted clock as well as the data. If the PLL is unable to lock to the serial data stream, it instead locks to REFCLK[A:B] to stabilize the voltage-controlled oscillator (VCO), and periodically switches back to the serial data stream to again attempt synchronization. This process continues until a valid input data stream is detected and lock is achieved. The CDR can maintain lock on data as long as the input data stream contains an adequate data “eye” (i.e., jitter is within specification) and the maximum data stream run length is not exceeded.

Bit alignment times fall into two categories: realignment when the input serial data stream experiences an abrupt phase change (as may occur when protection switching is performed between two paths having different delays), and alignment from a no-signal condition. Realignment is very quick, since the PLL's VCO is already locked on frequency and only needs to adapt to the new phase. This re-alignment has been observed to require no more than one microsecond when REFCLK[A:B] = 156.25 MHz.

Alignment from a no-signal condition has two components. First, there is the re-acquisition to the data's frequency and phase. The time required for re-acquisition to the data's frequency is minimized by logic that periodically switches the PLL to lock to the REFCLK[A:B] when it fails to lock on the serial data stream, thus limiting the VCO's frequency wander. Second, there is the time spent while the PLL is locking to REFCLK[A:B], which can be from zero to a maximum value, depending on when the serial data stream becomes valid in relation to the PLL's switching to/from REFCLK[A:B]. This alignment has been observed to require no more than 4 microseconds when REFCLK = 156.25 MHz.

Byte alignment occurs once valid bit alignment is achieved. The byte aligner looks for a particular 7-bit sequence (either 0011111 or its complement, 1100000) that, in data that has been 8b/10b encoded per Fibre Channel or IEEE 802.3ae specifications, only occurs in the comma (/K/) characters K28.1, K28.5 and K28.7. Byte alignment only occurs when the ENBYSYNC_xx signal for that channel is active high, and re-alignment occurs on each 7-bit sequence encountered. However, if ENBYSYNC_xx is asserted active high and no comma character is encountered, and then is brought inactive low, the channel will still perform one byte alignment operation on the next comma character. Byte alignment occurs immediately when an alignment sequence is detected, so the lock time is only one clock period.

Note: Each time the byte aligner performs an alignment, it also corrects the phase of the internal RBC_xx clock. This can result in the "stretching" of the clock by a half-phase in order to cause the output data to align with the rising edge of RBC_xx.

Word (32-bit) alignment can occur after the Fibre Channel (XAUI_MODE_xx = 0) or XAUI (XAUI_MODE_xx = 1) state machine has reached the in-synchronization state. In Fibre Channel mode, synchronization (WDSYNC_xx = 1) will occur after three ordered sets of data have been received in the absence of any code violations. After this, the next ordered set will cause the output data to be aligned such that the comma character is in the most significant byte. Thus, 32-bit word alignment has been achieved when four ordered sets have been detected. The time required is directly dependent on comma-character density.

Note: once word alignment is accomplished, no further alignment occurs unless and until WDSYNC_xx goes to zero and back to one again. Comma characters that are not located in the most significant byte position will not trigger further re-alignment while WDSYNC_xx is active. This behavior is as defined by the Fibre Channel specification. However, it means that, if the channel experiences an abrupt delay change (as could occur if an external MUX performs a protection switch between two links) and if the delay change is close enough to a full character or characters that not enough code violations are generated to cause loss of WDSYNC_xx, the channel could become misaligned and remain that way indefinitely. As mentioned above, this behavior is that defined by the Fibre Channel specification.

In XAUI mode, as the state diagram later in this data sheet indicates, three error-free code-groups containing commas must be detected before synchronization is declared.

Multi 2, 4 or 8 (ORT82G5 only) channel alignment (Lane alignment in XAUI mode) can be performed after 32-bit word alignment is complete. Multi-channel alignment is described in later sections of this data sheet.

Table 5. XAUI Link Synchronization State Diagram Notation – Variables

Variable	Description
sync_status	FAIL: Lane is not synchronized (correct 10-bit alignment has not been established). OK: Lane is synchronized. OK_NOC: Lane is synchronized but a comma character has not been detected in the past 200 code groups.
enable_CDET	TRUE: Align subsequent 10-bit words to the boundary indicated by the next received comma. FALSE: Maintain current 10-bit alignment.
gd_cg	Current number of consecutive cg_good indications.

Figure 10. XAUI Link Synchronization State Diagram

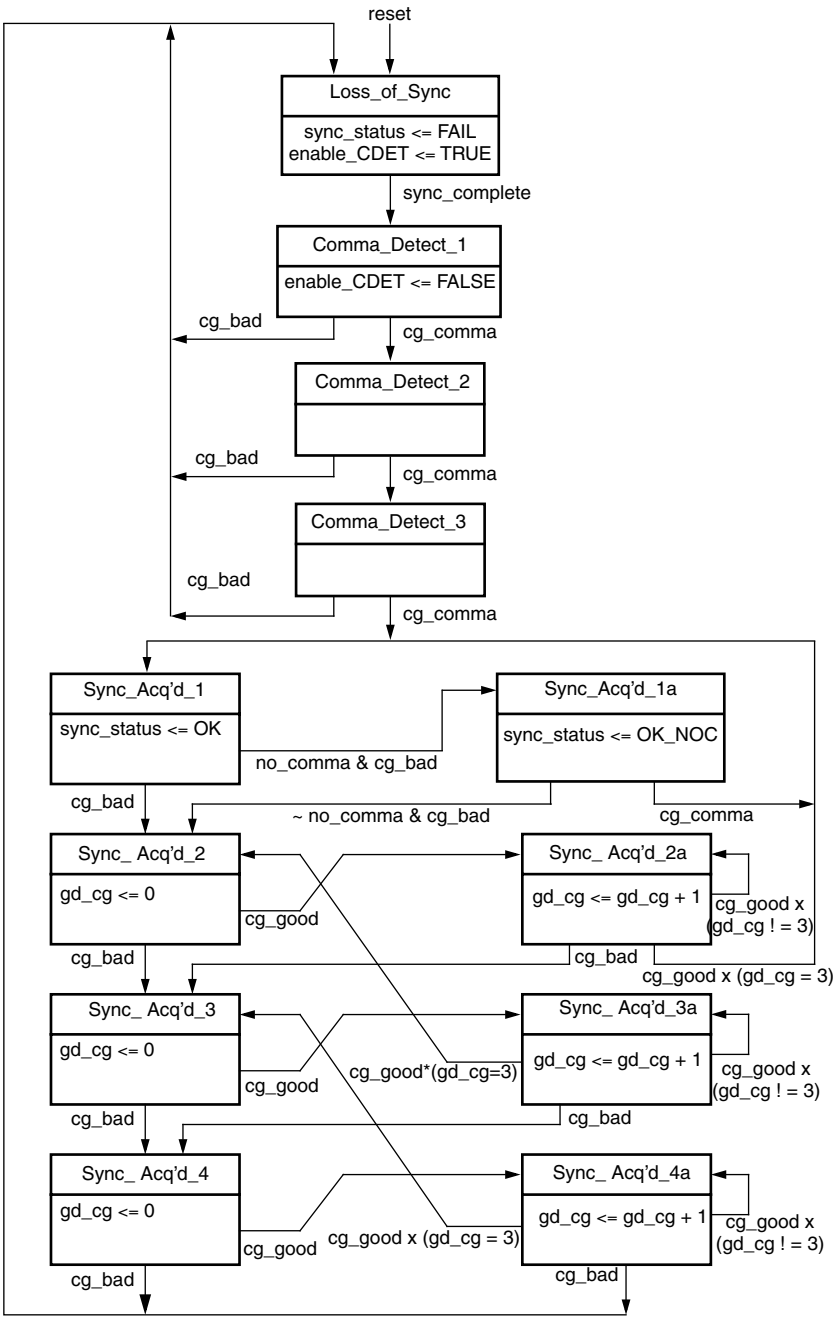
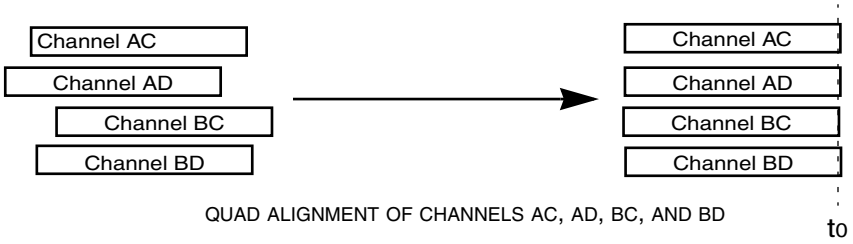


Figure 12. Four Channel Alignment of SERDES Blocks A and B



ORT82G5 Multi-channel Alignment

The ORT82G5 has a total of eight channels (four per SERDES block). The incoming data of these channels can be synchronized in several ways or they can be independent of one other. Two channels within a SERDES block can be aligned together. Channel A and B and/or channel C and D can form a pair as shown in Figure 13. Alternately, all four channels of a SERDES block can be aligned together to form a communication channel with a bandwidth of 10 Gbps as shown in Figure 14. Finally, the alignment can be extended across both SERDES block to align all eight channels in ORT82G5 as shown in Figure 15. Individual channels within an alignment group can be disabled (i.e., powered down) without disrupting other channels.

Figure 13. Dual Channel Alignment

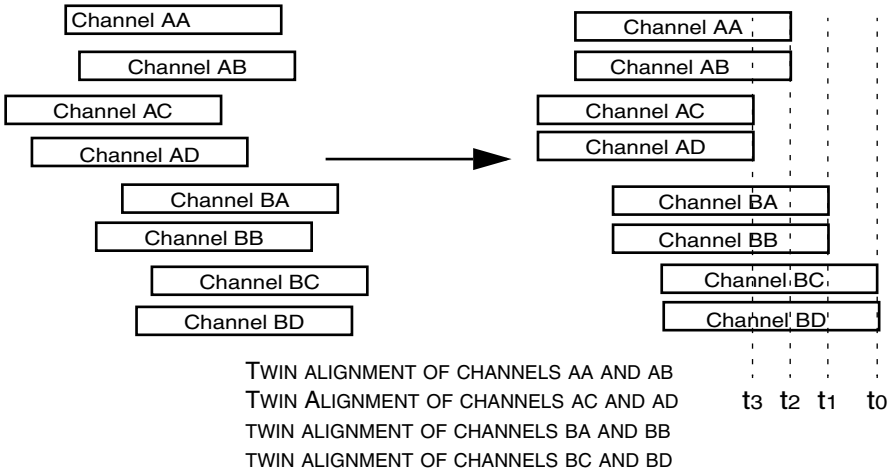
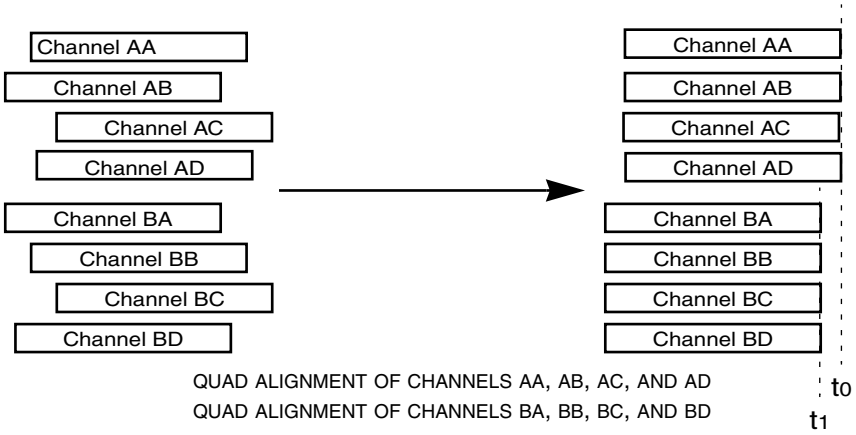


Figure 14. Alignment of SERDES Quads A and B



- FMPU_RESYNC2A2 for twin channel A[C:D]
- FMPU_RESYNC4B for quad channel B[A:D]
- FMPU_RESYNC2B1 for twin channel B[A:B]
- FMPU_RESYNC2B2 for twin channel B[C:D]

To resynchronize an independent channel (resetting the write and the read pointer of the FIFO) set the following bit to zero, and then set it to one:

- FMPU_RESYNC1_xx

ORT42G5 Alignment Sequence

1. Follow steps 1, 2 and 3 in the start up sequence described in a later section.

2. Initiate a SERDES software reset by setting the SWRST bit to 1 and then to 0. Note that, any changes to the SERDES configuration bits should be followed by a software reset.

3. Wait for 3 ms. REFCLK should be toggling by this time. During this time, configure the following registers.

Set the following bits in registers 30820, 30920:

- XAUI_MODE_xx-set to 1 for XAUI mode or keep the default value of 0 if the Fibre Channel state machine was selected.
- Enable channel alignment by setting FMPU_SYNMODE bits in registers 30811, 30911.
- FMPU_SYNMODE_xx. Set to appropriate values for 2 or 4 channel alignment based on Table 6.
- Set RCLKSEL[A:B] and TCKSEL[A:B] bits in register 30A00.
- RCKSEL[A:B]-choose clock source for 78 MHz RCK78x (Table 18).
- TCKSEL[A:B]-Choose clock source for 78 MHz TCK78x (Table 17).

Send data on serial links. Monitor the following status/alarm bits:

- Monitor the following alarm bits in registers 30020, 30030, 30120, 30130.
- LKI-PLL_xx lock indicator. A 1 indicates that PLL has achieved lock.
- Monitor the following status bits in registers 30804, 30904
- XAUISTAT_xx - In XAUI mode, they should be 10.

Monitor the following status bits in registers 30805, 30905

- DEMUXWAS_xx - They should be 1 indicating word alignment is achieved.
- CH24_SYNCxx - They should be 1 indicating channel alignment. This is cleared by resync.

4. Write a 1 to the appropriate resync registers 30820, 30920 or 30A02. Note that this assumes that the previous value of the resync bits are 0. The resync operation requires a rising edge. Two writes are required to the resync bits: write a 0 and then write a 1. It is highly recommended to precede a resync with a word alignment, especially in situations where a disturbance in the receive SERDES path can cause misalignment of data and OOS indications without bringing the FC/XAUI state machine to a loss of synch state. A word alignment is achieved by writing a 0 and then a 1 to the appropriate DOWDALIGNxx bits in registers 30810/30910.

Check out-of-sync and FIFO overflow status in registers 30814 (Bank A).

- SYNC2_A_OOS, SYNC2_A_OVFL - by 2 alignment.

Check out-of-sync status in registers 30914 (Bank B).

- SYNC2_B_OOS, SYNC2_B_OVFL - by 2 alignment.

Check out-of-sync status in registers 30A03.

- SYNC4_OOS, SYNC4_OVFL - by 4 alignment.
- If out-of-sync bit is 1, then rewrite a 1 to the appropriate resync registers and monitor the OOS bit again.
- If Out of Synchronization (OOS) bit is 0 but OVFL bit is 1, then check if the RX_FIFO_MIN value has been pro-

Table 10. Definition of Status Bits of MRWDxx that Vary for Different Channels for the ORT82G5 (Continued)

Channel Index	Bit Index	Name	Description
BA	29	CV_BA_OR	Code violation in one or more of the received 10-bit groups for channel BA
BA	19	SYNC2_B1_OOS	Dual channel synchronization of channels BA and BB not successful if 1
BB	29	CV_BB_OR	Code violation in one or more of the received 10-bit groups for channel BB
BB	19	SYNC4_B_OOS	Quad channel synchronization of SERDES quad B not successful if 1
BC	29	CV_BC_OR	Code violation in one or more of the received 10-bit groups for channel BC
BC	19	SYNC2_B2_OOS	Dual channel synchronization of channels BC and BD not successful if 1
BD	29	CV_BD_OR	Code violation in one or more of the received 10-bit groups for channel BD
BD	19	SYNC8_OOS	Eight channel synchronization not successful if 1

For the ORT82G5, the SYNC2_[A1,A2,B1,B2]_OOS, SYNC4_[A:B]_OOS,and SYNC8_OOS signals can be used with CH248_SYNC_xx to determine if the desired multi-channel alignment was successful. If, when CH248_SYNC_xx goes high the corresponding OOS signal remains low, the data being transferred across the core/FPGA interface is correctly aligned between channels. Note that only the signals corresponding to the selected alignment mode will be meaningful.

For both devices, the code violation signals will only be valid if the corresponding CV_SELxx = 1. (If 8b10bR=0, CV_SEL should also be zero. The CV_xx_OR signals are obtained by ORing four code violation signals from the 1:4 DEMUX block. These are primarily indicators of received signal quality since a single code violation will not force a loss of sync (LOS) state in the word alignment state machines. Since these signals come from the DEMUX block, if multi-channel alignment is enabled, the code violation signals correspond to data that must still be multi-channel aligned. Hence these signals provide advance notification of detected violations in data that will appear at the core/FPGA interface several clock cycles later. The exact number of clock cycles that the data is delayed depends on the skew between the incoming data for the different channels.

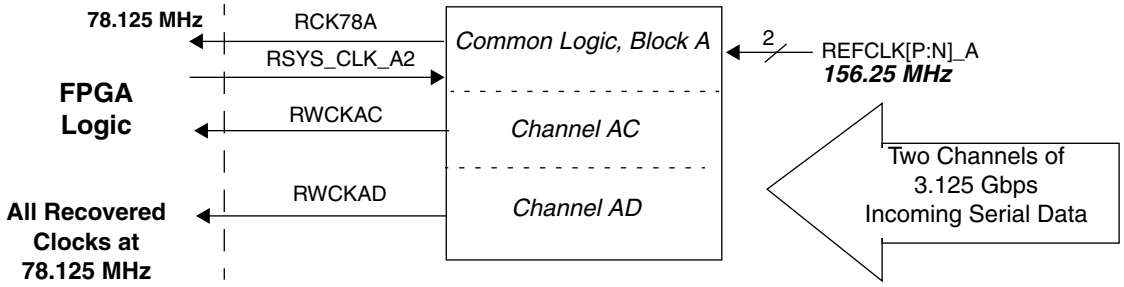
Transceiver FPGA/Embedded Core Signals

Table 12 summarizes the interface signals between the FPGA logic and the core. In the table, an input refers to a signal flowing into the embedded core and an output refers to a signal flowing out of the embedded core.

Table 11. Transceiver Embedded Core/FPGA Interface Signal Description for the ORT42G5

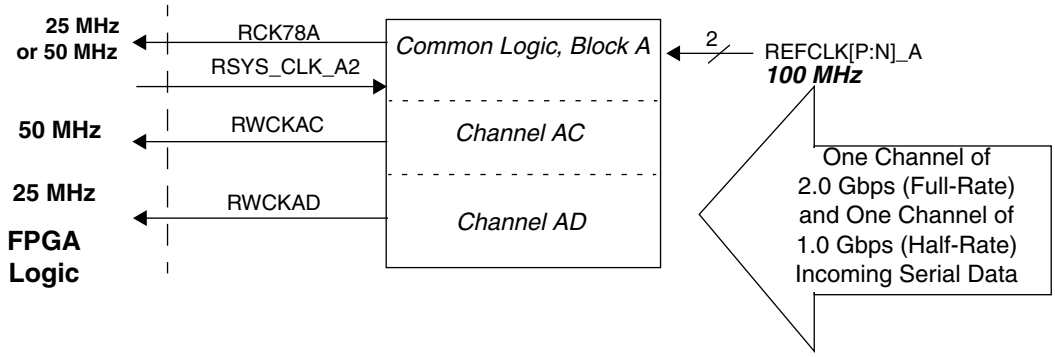
FPGA/Embedded Core Interface Signal Name (xx = [AC, AD, BC or BD])	Input (I) to or Output (O) from Core	Signal Description
Transmit Path Signals		
TWDxx[31:0]	I	Transmit data – channel xx.
TCOMMAxx[3:0]	I	Transmit comma character – channel xx.
TBIT9xx[3:0]	I	Transmit force negative disparity – channel xx
TSYS_CLK_xx	I	Transmit low-speed clock to the FPGA – channel xx
TCK78[A:B]	O	Transmit low-speed clock to the FPGA – SERDES Quad [A:B].
Receive Path Signals		
MRWDxx[39:0]	O	Receive data – Channel xx (see Table 8 and Table 9).
RWCKxx	O	Low-speed receive clock—Channel xx.
RCK78[A:B]	O	Receive low-speed clock to FPGA—SERDES Quad [A:B].
RSYS_CLK_A2	I	Low-speed receive FIFO clock for channels AC, AD
RSYS_CLK_B2	I	Low-speed receive FIFO clock for channels BC, BD
CV_SELxx	I	Enable detection of code violations in the incoming data
SYS_RST_N	I	Synchronous reset of the channel alignment blocks.

Figure 20. Receive Clocking for a Single Block (Similar Connections Would Be Used for Block B)



The receive channel alignment bypass mode allows mixing of half and full line rates among the channels, as shown in Figure 21. The figure shows channel AC configured in full rate mode at 2.0 Gbps. Channel AD configured in half-rate mode at 1.0 Gbps. The receive alignment FIFO per channel cannot be used in this mode.

Figure 21. Receive Clocking for Mixed Line Rates



Each SERDES block can also be configured for any line rate (0.6 to 3.7 Gbps), since each block has its own reference clock input pins.

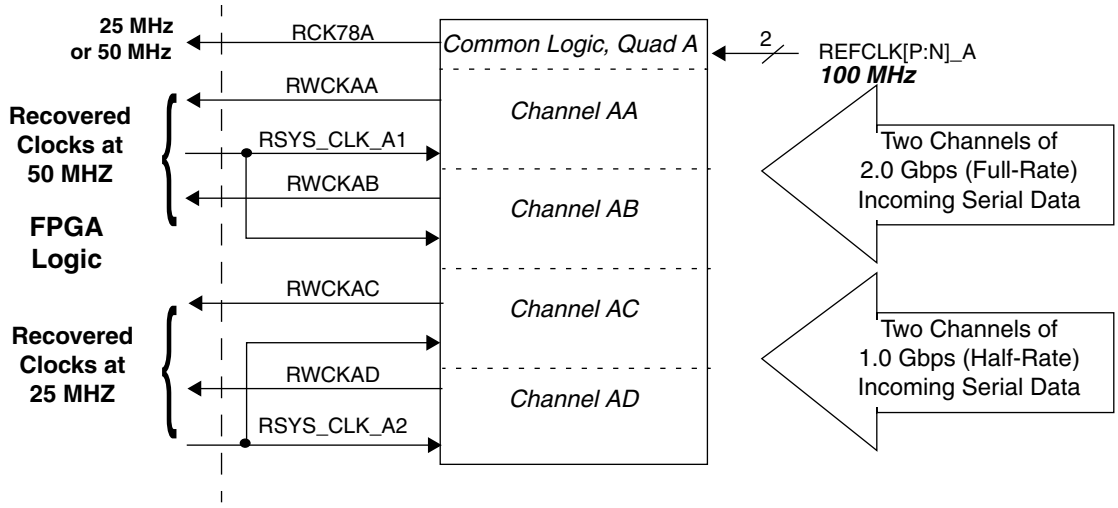
Multi-Channel Alignment Clocking Strategies for the ORT42G5

The data on the four channels in the ORT42G5 can be independent of each other or can be synchronized in two different ways. For example, two channels within a SERDES block can be aligned together, channel C and channel D. Alternatively, all four channels in a SERDES block can be aligned together to form a communication channel with a bandwidth of 10 Gbps. Individual channels within an alignment group can be disabled (i.e., powered down) without disrupting other channels. Clocking strategies for these various modes are described in the following paragraphs.

For dual alignment both channels must be sourced by the same clock. Either RWCKAC or RWCKAD can be connected to RSYS_CLK_A2. A clocking example for dual alignment is shown in Figure 22.

The receive channel alignment bypass mode allows mixing of half and full line rates among the channels, as shown in Figure 28. The figure shows channel pair AA and AB configured in full rate mode at 2.0 Gbps. Channel pair AC and AD are configured in half-rate mode at 1.0 Gbps.

Figure 28. Receive Clocking for Mixed Line Rates



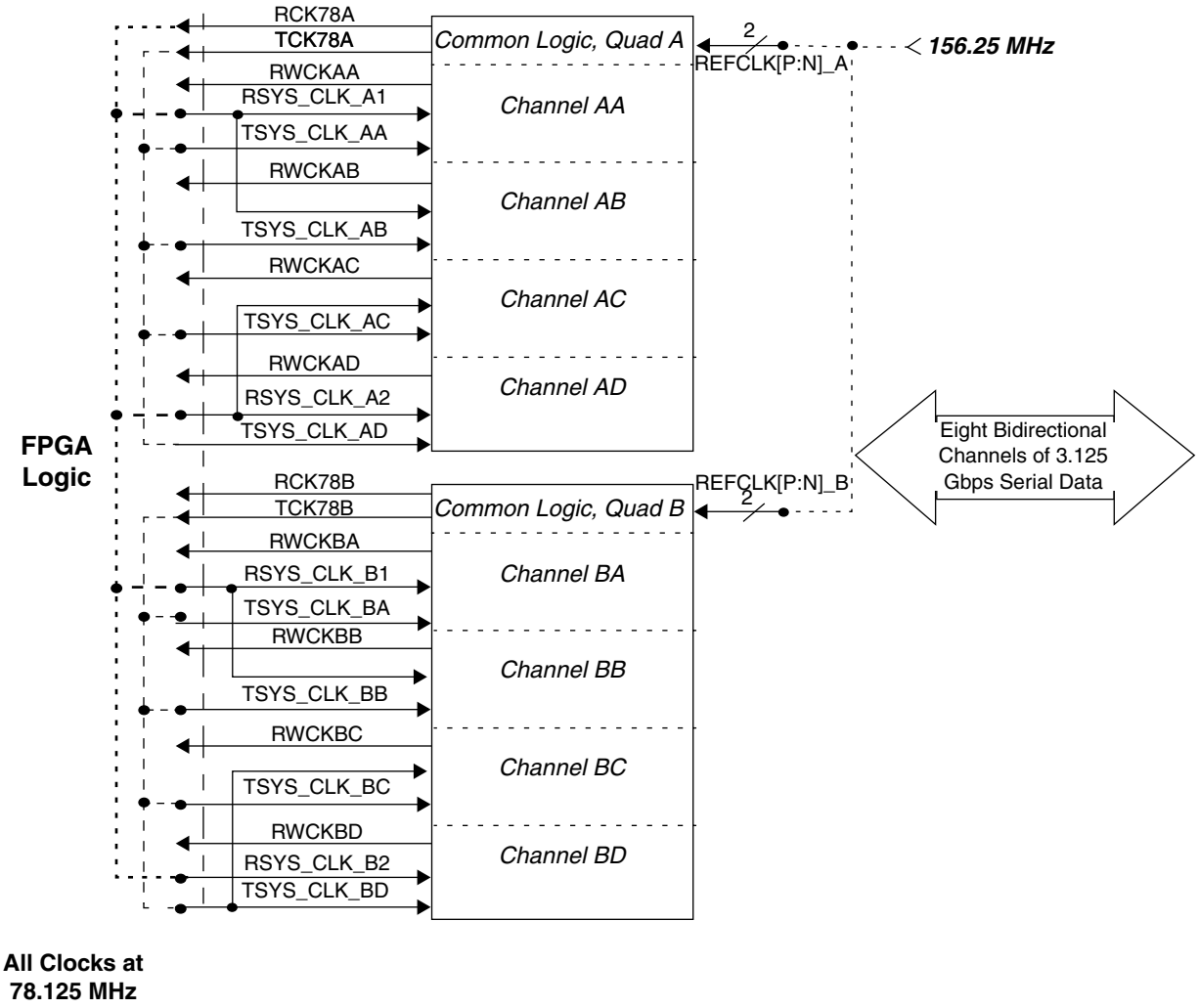
As noted in the caption of Figure 28, each quad can be configured in any line rate (0.6 to 3.7 Gbps), since each quad has its own reference clock input pins. The receive alignment FIFO per channel cannot be used in this mode.

Multi-Channel Alignment Clocking Strategies for the ORT82G5

The data on the eight channels (four per SERDES quad) in the ORT82G5 can be independent of each other or can be synchronized in several ways. For example, two channels within a SERDES can be aligned together; channel A and B and/or channel C and D. Alternatively, all four channels in a SERDES quad can be aligned together to form a communication channel with a bandwidth of 10 Gbps. Finally, the alignment can be extended across both SERDES quads to align all eight channels. Individual channels within an alignment group can be disabled (i.e., powered down) without disrupting other channels. Clocking strategies for these various modes are described in the following paragraphs.

For dual alignment both twins within a quad can be sourced by clocks that are different from the other channels, however each pair of SERDES must have the same clock. The channel pair AA and AB is driven on the low speed side by RSYS_CLK_A1 and the channel pair AC and AD are driven on the low speed side by RSYS_CLK_A2. Either RWCKAA or RWCKAB can be connected to RSYS_CLK_A1 and either RWCKAC or RWCKAD can be connected to RSYS_CLK_A2. A clocking example for dual alignment is shown in Figure 29.

Figure 31. Clocking for Eight Channel Alignment



Reset Operation

The SERDES block can be reset in one of three different ways as follows: on power up, using the hardware reset, or via the microprocessor interface. The power up reset process begins when the power supply voltage ramps up to approximately 80% of the nominal value of 1.5V. Following this event, the device will be ready for normal operation after 3 ms.

A hardware reset is initiated by making the PASB_RESETN low for at least two microprocessor clock cycles. The device will be ready for operation 3 ms after the low to high transition of the PASB_RESETN. This reset function affects all SERDES channels and resets all microprocessor and internal registers and counters.

Using the software reset option, each channel can be individually reset by setting SWRST (bit 2) to a logic 1 in the channel configuration register. The device will be ready 3 ms after the SWRST bit is deasserted. Similarly, all four channels per quad SERDES can be reset by setting the global reset bit GSWRST. The device will be ready for normal operation 3 ms after the GSWRST bit is deasserted. Note that the software reset option resets only SERDES internal registers and counters. The microprocessor registers are not affected. It should also be noted that the embedded block cannot be accessed until after FPGA configuration is complete.

- Parallel loopback at MUX/DEMUX boundary excluding SERDES (near end)

The three loopback modes are described in more detail in the following sections. As noted earlier, other specialized loopback modes can be obtained by configuration of the FPGA logic or by connections external to the FPSC.

High-Speed Serial Loopback at the CML Buffer Interface

The high-speed serial loopback mode has the serial transmit signals looped back internally to the serial receive circuitry. The internal loopback path is from the input connection to the transmit CML buffer to the output connection from the receive CML buffer. The data are sourced on the TWDxx[31:0], TCOMMAxx[3:0] and TBIT9xx[3:0] signal lines and received on the MRWDxx[39:0] signal lines. The serial loopback path does not include the high-speed input and output buffers. If TESTEN_xx is set, the HDOUTP_xx and HDOUTN_xx outputs are active in this mode while the CML input buffers are powered down. The device is otherwise in its normal mode of operation. This mode is normally used for tests where the data source and destination are on the same card and is the basic loopback path shown earlier in Figure 32(a).

The data rate selection bits, TXHR and RXHR, in the channel configuration registers must be configured to carry the same value. Table 19 and Table 20 summarize the settings of the control interface register configuration bits for high-speed serial loopback.

Table 19. High-Speed Serial Loopback Configuration Bit Definitions for the ORT42G5

Register Address	Bit Value	Bit Name	Comments
30022, 30032, 30122, 30132	Bit 0 = 0 or 1	TXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 7 = 0 or 1	8B10BT	Set to 0 or 1. If set to 0, the 8b/10b encoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to the same value.
30023, 30033, 30123, 30133	Bit 0 = 0 or 1	RXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 3 = 0 or 1	8B10BR	Set to 0 or 1. If set to 0, the 8b/10b decoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to the same value.
30801, 30901	Bit 2 = 1 (Channel C) Bit 3 = 1 (Channel D)	LOOPENB_xx	Set any of the bits 0-3 to 1 to do serial loopback on the corresponding channel.* The high speed serial outputs will not be active.

*This test mode can also be set using TESTEN_xx in place of LOOPENB_xx. In that case, Test Mode must be set to 00000.

Table 20. High-Speed Serial Loopback Configuration Bit Definitions for the ORT82G5

Register Address	Bit Value	Bit Name	Comments
30002, 30012, 30022, 30032, 30102, 30112, 30122, 30132	Bit 0 = 0 or 1	TXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 7 = 0 or 1	8B10BT	Set to 0 or 1. If set to 0, the 8b/10b encoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to the same value.
30003, 30013, 30023, 30033, 30103, 30113, 30123, 30133	Bit 0 = 0 or 1	RXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 3 = 0 or 1	8B10BR	Set to 0 or 1. If set to 0, the 8b/10b decoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to the same value.

Table 24. Decoding of SCHAR_CHAN

SCHAR_CHAN0	SCHAR_CHAN1	Channel
0	0	BA
1	0	BB
0	1	BC
1	1	BD

The receive characterization test mode is entered when SCHAR_ENA=1 and SCHAR_TXSEL=0, In this mode, one of the channels of SERDES outputs is observed at chip ports as shown in Table 25. The channel that is observed is also based on the decoding of SCHAR_CHAN as shown in Table 25.

Table 25. SERDES Receive Characterization Mode

SERDES Output	Chip Port
BYTSYNCBx	PSCHAR_BYTSYNC
WDSYNCBx	PSCHAR_WDSYNC
CVOBx	PSCHAR_CV
LDOUTBx[9:0]	PSCHAR_LDIO[9:0]
RBC0Bx	PSCHAR_CKIO0
RBC1Bx	PSCHAR_CKIO1

Embedded Core Block RAM

There are two independent memory blocks (labeled A and B) built-into the Embedded ASIC Core (EAC). Each memory block has a capacity of 4K words by 36 bits. These two memory blocks (also called “slices”) are in addition to the block RAMs found in the FPGA portion of the ORT82G5.

Although the memory blocks/slices are in the EAC part of the chip, they do not interact with the rest of the EAC circuits, but are standalone memories designed specifically to increase RAM capacity in the ORT82G5 chip. They can be used by logic implemented in the FPGA portion of the FPSC. Figure 34 represents one of the two available memory slices built into the EAC. The index “x” refers to the memory slice (x=A for slice A, x=B for slice B). Each memory slice is organized into two sections, which are also labeled as A and B. In Figure 34, SDRAM A is one section of slice x, and SDRAM B is another section of slice x. Data can be written to both sections of a slice independently. However, a read access can access only one of sections A or B at any given time (CSR_x=0 selects section A, CSR_x=1 selects section B).

The 36 bits written to or read from the memory slice are composed of 32 bits of data (bits 31:24, 23:16, 15:8, 7:0), and 4 bits of parity (bits 35,34,33,32). The core performs no parity checking functions. The data read from the memory is registered so that it works as a pipelined synchronous memory block.

For illustration purposes, assuming that the memory slice in Figure 34 is slice A (x=A), then certain signals apply to both sections of slice A. These include D_A[35:0], CKW_A, AW_A[10:0], BYTEWN_A[3:0], Q_A[35:0], CKR_A, CSR_A, and AR_A[10:0]. The BYTEWN_A[3:0] are byte and parity write enable bits for each byte and parity bit of data being written.

BYTEWN_A[3] is associated with D_A[35,31:24].
BYTEWN_A[2] is associated with D_A[34,23:16].
BYTEWN_A[1] is associated with D_A[33,15:8].
BYTEWN_A[0] is associated with D_A[32,7:0].

The signals that are unique to each section of slice A are:

CSWA_A --enables writing to section A of slice A
CSWB_A -- enables writing to section B of slice A

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Common Transmit and Receive Channel Configuration Registers (Read/Write), xx = [AC, AD, BC or BD]				
30022 - AC 30032 - AD 30122 - BC 30132 - BD	[0]	TXHR_xx	00	Transmit Half Rate Selection Bit, Channel xx. When TXHR_xx = 1, HDOUT_xx's baud rate = (REFCLK[A:B]*10) and TCK78[A:B] =(REFCLK[A:B]/4); when TXHR_xx=0, HDOUT_xx's baud rate = (REFCLK[A:B]*20) and TCK78[A:B]=(REFCLK[A:B]/2). TXHR_xx = 0 on device reset.
	[1]	PWRDNT_xx		Transmit Powerdown Control Bit, Channel xx. When PWRDNT_xx = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT_xx = 0 on device reset.
	[2]	PE0_xx		Transmit Preemphasis Selection Bit 0, Channel xx. PE0_xx and PE1_xx select one of three preemphasis settings for the transmit section. PEO_xx=PE1_xx = 0, Preemphasis is 0% PEO_xx=1, PE1_xx = 0 or PEO_xx=0, PE1_xx = 1, Preemphasis is 12.5% PEO_xx=PE1_xx = 1, Preemphasis is 25%. PEO_xx=PE1_xx = 0 on device reset.
	[3]	PE1_xx		
	[4]	HAMP_xx		Transmit Half Amplitude Selection Bit, Channel xx. When HAMP_xx = 1, the transmit output buffer voltage swing is limited to half its normal amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP_xx = 0 on device reset.
	[5]	Reserved		Reserved. Must be set to 0. Set to 0 on device reset.
	[6]	Reserved		Reserved
	[7]	8b10bT_xx		Transmit 8b/10b Encoder Enable Bit, Channel xx. When 8b10bT_xx = 1, the 8b/10b encoder in the transmit path is enabled. Otherwise, the data is passed unencoded. 8b10bT_xx = 0 on device reset.
30023 - AC 30033 - AD 30123 - BC 30133 - BD	[0]	RXHR_xx	20	Receive Half Rate Selection Bit, Channel xx. When RXHR_xx =1, HDIN_xx's baud rate = (REFCLK[A:B]*10) and RCK78[A:B]=(REFCLK[A:B]/4); when RXHR_xx=0, HDIN_xx's baud rate = (REFCLK[A:B]*20) and RCK78[A:B]=(REFCLK/2). RXHR_xx = 0 on device reset.
	[1]	PWRDNR_xx		Receiver Power Down Control Bit, Channel xx. When PWRDNR_xx = 1, sections of the receive hardware are powered down to conserve power. PWRDNR_xx = 0 on device reset.
	[2]	Reserved		Reserved. Set to 1 on device reset.
	[3]	8b10bR_xx		Receive 8b/10b Decoder Enable Bit, Channel xx. When 8b10bR = 1, the 8b/10b decoder in the receive path is enabled. Otherwise, the data is passed undecoded. 8b10bR_xx = 0 on device reset.
	[4]	LINKSM_xx		Link State Machine Enable Bit, Channel xx. When LINKSM_xx = 1, the receiver Fiber Channel link state machine is enabled. Otherwise, the Fibre Channel link state machine is disabled. Note: LINKSM_xx is ignored when XAUI_MODE_xx=1. LINKSM_xx = 0 on device reset.
	[5:7]	Not used		Not used.

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30810 - Ax 30910 - Bx	[0]]	—	00	Reserved for future use
	[1]	—		Reserved for future use
	[2]	DOWDALIGN_xC		Word Realign Bit. When DOWDALIGN_xC transitions from 0 to 1, the receiver realigns on the next comma character for Channel xC. NOWDALIGN_xC=0 on device reset.
	[3]	DOWDALIGN_xC		Word Realign Bit. When DOWDALIGN_xC transitions from 0 to 1, the receiver realigns on the next comma character for Channel xC. NOWDALIGN_xC=0 on device reset.
	[4]	—		Reserved for future use. Set to zero.
	[5]	—		Reserved for future use. Set to zero.
	[6]	FMPU_STR_EN _xC		Enable multi-channel alignment for Channel xC. When FMPU_STR_EN _xC = 0, Channel xC is not part of a multi-channel alignment group When FMPU_STR_EN _xC = 1, Channel xC is part of a twin channel alignment (SERDES block A or B) or quad channel alignment (both SERDES blocks) group.
	[7]	FMPU_STR_EN _xD		Enable multi-channel alignment for Channel xD. When FMPU_STR_EN _xD = 0, Channel xD is not part of a multi-channel alignment group When FMPU_STR_EN _xD = 1, Channel xD is part of a twin channel alignment (SERDES block A or B) or quad channel alignment (both SERDES blocks) group.
30811 - Ax 30911 - Bx	[0:7]	FMPU_SYNMODE_ [A:B]	00	Sync mode for block [A:B] 00000000 = No channel alignment 00001010 = Twin channel alignment, SERDES block [A:B] 00001111 = Quad channel alignment (both SERDES blocks)
30820 - Ax 30920 - Bx	[0]	—	00	Reserved for future use.
	[1]	—		Reserved for future use.
	[2]	FMPU_RESYNC1_xC		Resync a Single Channel. When FMPU_RESYNC1_xC transitions from 0 to 1, the corresponding channel xC is resynchronized (the write and read pointers are reset). FMPU_STR_EN_xC=0 on device reset.
	[3]	FMPU_RESYNC1_xD		Resync a Single Channel. When FMPU_RESYNC1_xD transitions from 0 to 1, the corresponding channel xD is resynchronized (the write and read pointers are reset). FMPU_STR_EN_xD=0 on device reset.
	[4]	—		Reserved for future use.
	[5]	FMPU_RESYNC2[A:B]		Resync a Twin-Channel Group. When FMPU_RESYNC2[A:B] transitions from a 0 to a 1, the corresponding twin-channel group is resynchronized. FMPU_RESYNC2[A:B]=0 on device reset.
	[6]	—		Reserved for future use.
	[7]	XAUI_MODE[A:B]		Controls use of XAUI link state machine in place of Fibre-Channel state machine. When XAUI_MODE[A:B]=1, both channels in the SERDES block enable their XAUI link state machines. (LINKSM_xx bits are ignored). XAUI_MODE[A:B]=0 on device reset.
30821 - A 30921 - B	[0]	NOCHALGN [A:B]	00	Bypass channel alignment. NOCHALGN [A:B] =1 causes bypassing of multi-channel alignment FIFOs for the corresponding SERDES quad. NOCHALGN [A:B] =0 on device reset.
	[1:7]	—		Reserved for future use.

ORT82G5 Memory Map

Each ORT82G5 SERDES block has eight independent channels. Each channel is identified by both a quad identifier, A or B, and a channel identifier, A, B, C or D. The registers in ORT82G5 are 8-bit memory locations, which can be classified into Status Register and Control Register.

Status Register
Read-only register to convey the status information of various operations within the FPSC core. An example is the state of the XAUI link-state-machine.

Control Register
Read-write register to set up the control inputs that define the operation of the FPSC core.

Reserved addresses for the FPSC register blocks are shown in Table 29.

Table 29. Structural Register Elements

Address (0x)	Description
300xx	SERDES A, internal registers.
301xx	SERDES B, internal registers.
308xx	Channel A [A:D] registers (external to SERDES blocks).
309xx	Channel B [A:D] registers (external to SERDES blocks).
30A0x	Global registers (external to SERDES blocks).

Table 30 details the memory map for the FPSC portion of the ORT82G5 device. In both Table 29 and Table 30, the addresses are given as 18-bit hexadecimal (18'h) values. The address may be sourced either through the Microprocessor interface or a User Master Interface. The MicroProcessor Interface (MPI) address bus is a 32-bit bus which follows the Power PC convention where address bit 0 is the MSb and address bit 31 is the LSb. The MPI maps bits MPI_ADDR[14:31] to bits [17:0] of the system address bus. The User Master Interface (UMI) has an 18-bit address bus and uses the opposite notation, where address line 17 is the MSb and address line 0 is the LSb. The UMI maps bits um_addr[17:0] to bits [17:0] of the system address bus. Because of the address mapping done by the MPI and UMI, the same hexadecimal address value is valid for both interfaces.

The UMI, internal and microprocessor interface data buses have both 32-bit data and 4-bit parity fields and the data fields are mapped 1:1 to each other, i.e., bit 0 is bit 0 for all three buses. The bit ordering is specific to the targeted functional block. In the memory map, only bits [0:7] are specified and the convention followed for sub-field descriptions is to map the bits in the description directly to the bit order given in the bit column. For example, to select channel C as the source for the transmit and receive clocks, the register at location 30A00 should have bits 0, 2, 4 and 6 set to zero and bits 1, 3, 5 and 7 set to one.

In the example in the previous paragraph, the bits being set are control bits and are independent of the MSb/LSb convention used. The resulting bit pattern 01010101 maps to the hexadecimal value AA if the left-most bit is considered the LSb and to 55 if the right-most bit is considered the LSb. In some cases, however, the data represents the value of a specific parameter, such as a size or threshold level, and the value may be stored at more than one address location, since each location can hold only 8 bits of data. For a given register, either the MSb or the LSb bit position is specified explicitly in the memory map. If the parameter value extends over multiple register locations, the relative bit or byte ordering is also specified. For additional information on the MPI and the system bus, see Technical Note TN1017, *ORCA Series 4 MPI/System Bus.*

Table 30. ORT82G5 Memory Map

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Alarm Registers (Read Only), xx=[AA,...,BD]				
30000 - AA 30010 - AB 30020 - AC 30030 - AD 30100 - BA 30110 - BB 30120 - BC 30130 - BD	[0]	Reserved	00	Reserved
	[1]	LKI_xx		Receive PLL Lock Indication, Channel xx. LKI_xx = 1 indicates the receive PLL is locked.
	[2]	Reserved		Reserved
	[3]	Reserved		Reserved
	[4:7]	Not used		Not used
SERDES Alarm Mask Registers (Read/Write), xx=[AA,...,BD]				
30001 - AA 30011 - AB 30021 - AC 30031 - AD 30101 - BA 30111 - BB 30121 - BC 30131 - BD	[0]	Reserved	FF	Reserved, must be set to 1. Set to 1 on device reset.
	[1]	MLKI_xx		Mask Receive PLL Lock Indication, Channel xx.
	[2]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
	[3]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
	[4]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
	[5]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
	[6]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
	[7]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
SERDES Common Transmit and Receive Channel Configuration Registers (Read/Write), xx=[AA,...,BD]				
30002 - AA 30012 - AB 30022 - AC 30032 - AD 30102 - BA 30112 - BB 30122 - BC 30132 - BD	[0]	TXHR_xx	00	Transmit Half Rate Selection Bit, Channel xx. When TXHR_xx = 1, HDOUT_xx's baud rate = (REFCLK[A:B]*10) and TCK78[A:B] =(REFCLK[A:B]/4); when TXHR_xx=0, HDOUT_xx's baud rate = (REFCLK[A:B]*20) and TCK78[A:B]=(REFCLK[A:B]/2). TXHR_xx = 0 on device reset.
	[1]	PWRDNT_xx		Transmit Powerdown Control Bit, Channel xx. When PWRDNT_xx = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT_xx = 0 on device reset.
	[2]	PE0_xx		Transmit Preemphasis Selection Bit 0, Channel xx. PE0_xx and PE1_xx select one of three preemphasis settings for the transmit section. PEO_xx=PE1_xx = 0, Preemphasis is 0% PEO_xx=1, PE1_xx = 0 or PEO_xx=0, PE1_xx = 1, Preemphasis is 12.5% PEO_xx=PE1_xx = 1, Preemphasis is 25%. PEO_xx=PE1_xx = 0 on device reset.
	[3]	PE1_xx		
	[4]	HAMP_xx		Transmit Half Amplitude Selection Bit, Channel xx. When HAMP_xx = 1, the transmit output buffer voltage swing is limited to half its normal amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP_xx = 0 on device reset.
	[5]	Reserved		Reserved. Must be set to 0. Set to 0 on device reset.
	[6]	Reserved		Reserved
	[7]	8b10bT_xx		Transmit 8b/10b Encoder Enable Bit, Channel xx. When 8b10bT_xx = 1, the 8b/10b encoder in the transmit path is enabled. Otherwise, the data is passed unencoded. 8b10bT_xx = 0 on device reset.

The disadvantage with this scheme is the fact that it is difficult to distribute a 156 MHz reference clock across a backplane. This may require expensive clock driver chips on the board to drive clocks to different destinations within the specified jitter limits for the reference clock.

Figure 38. Distributed Reference Clock to Rx And Tx Devices

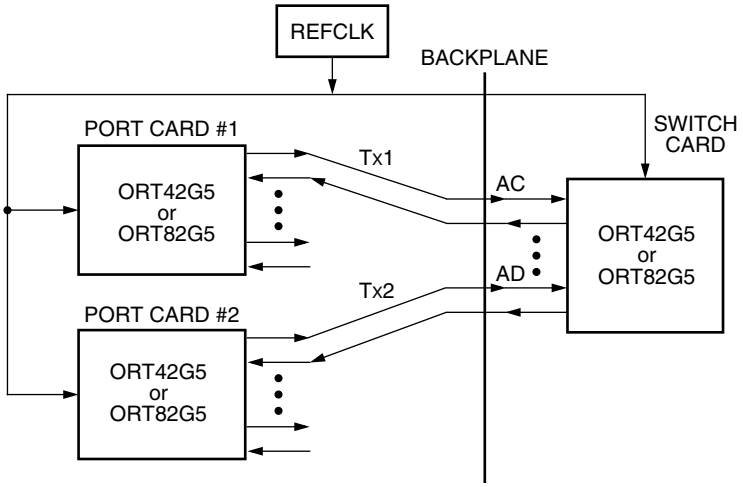


Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
L11	-	-	VSS	VSS	-	-
N15	-	-	VDD15	VDD15	-	-
D10	1 (TC)	5	IO	PT18D	PTCK1C	L68C
C10	1 (TC)	5	IO	PT18C	PTCK1T	L68T
A12	1 (TC)	5	IO	PT17D	PTCK0C	L69C
B12	1 (TC)	5	IO	PT17C	PTCK0T	L69T
P6	-	-	VDD15	VDD15	-	-
A11	1 (TC)	5	IO	PT16D	VREF_1_05	L70C
B11	1 (TC)	5	IO	PT16C	-	L70T
L12	-	-	VSS	VSS	-	-
D9	1 (TC)	6	IO	PT15D	-	L71C
C9	1 (TC)	6	IO	PT15C	-	L71T
G15	1 (TC)	-	VDDIO1	VDDIO1	-	-
B10	1 (TC)	6	IO	PT14D	-	L72C
A10	1 (TC)	6	IO	PT14C	VREF_1_06	L72T
B9	0 (TL)	1	IO	PT13D	MPI_RTRY_N	L73C
A9	0 (TL)	1	IO	PT13C	MPI_ACK_N	L73T
D8	0 (TL)	1	IO	PT12D	M0	L74C
C8	0 (TL)	1	IO	PT12C	M1	L74T
A22	-	-	VSS	VSS	-	-
B8	0 (TL)	2	IO	PT12B	MPI_CLK	L75C
A8	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L75T
C7	0 (TL)	2	IO	PT11D	M2	L76C
D7	0 (TL)	2	IO	PT11C	M3	L76T
E9	0 (TL)	-	VDDIO0	VDDIO0	-	-
E6	0 (TL)	2	IO	PT11A	MPI_TEA_N	-
F6	-	-	VDD15	VDD15	-	-
B7	0 (TL)	3	IO	PT9D	VREF_0_03	L77C
A7	0 (TL)	3	IO	PT9C	-	L77T
A6	0 (TL)	3	IO	PT8D	D0	L78C
B6	0 (TL)	3	IO	PT8C	TMS	L78T
C6	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L79C
D6	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L79T
B1	-	-	VSS	VSS	-	-
A5	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L80C
B5	0 (TL)	4	IO	PT6C	D3	L80T
C5	0 (TL)	5	IO	PT5D	D1	L81C
D5	0 (TL)	5	IO	PT5C	D2	L81T
B2	-	-	VSS	VSS	-	-
A4	0 (TL)	5	IO	PT4D	TDI	L82C
B4	0 (TL)	5	IO	PT4C	TCK	L82T
E10	0 (TL)	-	VDDIO0	VDDIO0	-	-
B22	-	-	VSS	VSS	-	-
C4	0 (TL)	6	IO	PT2D	PLL_CK1C/PPLL	L83C

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AL19	5 (BC)	3	IO	PB22A	—	L11T_D0
AK18	5 (BC)	3	IO	PB22B	—	L11C_D0
P15	—	—	VSS	VSS	—	—
AP24	5 (BC)	3	IO	PB22C	—	L12T_D0
AN23	5 (BC)	3	IO	PB22D	—	L12C_D0
AP25	5 (BC)	3	IO	PB23A	—	L13T_A0
AP26	5 (BC)	3	IO	PB23B	—	L13C_A0
AL13	5 (BC)	—	VDDIO5	VDDIO5	—	—
AL20	5 (BC)	3	IO	PB23C	PBCK1T	L14T_D0
AK19	5 (BC)	3	IO	PB23D	PBCK1C	L14C_D0
AK20	5 (BC)	3	IO	PB24A	—	L15T_D0
AL21	5 (BC)	3	IO	PB24B	—	L15C_D0
P20	—	—	VSS	VSS	—	—
AN24	5 (BC)	4	IO	PB24C	—	L16T_D0
AM23	5 (BC)	4	IO	PB24D	—	L16C_D0
AN26	5 (BC)	4	IO	PB25A	—	L17T_A0
AN25	5 (BC)	4	IO	PB25B	—	L17C_A0
AL15	5 (BC)	—	VDDIO5	VDDIO5	—	—
AK21	5 (BC)	4	IO	PB25C	—	L18T_D0
AL22	5 (BC)	4	IO	PB25D	VREF_5_04	L18C_D0
AM24	5 (BC)	4	IO	PB26A	—	L19T_D0
AL23	5 (BC)	4	IO	PB26B	—	L19C_D0
P21	—	—	VSS	VSS	—	—
AP27	5 (BC)	5	IO	PB26C	—	L20T_A0
AN27	5 (BC)	5	IO	PB26D	VREF_5_05	L20C_A0
AL24	5 (BC)	5	IO	PB27A	—	L21T_D0
AM25	5 (BC)	5	IO	PB27B	—	L21C_D0
AN13	5 (BC)	—	VDDIO5	VDDIO5	—	—
AP28	5 (BC)	5	IO	PB27C	—	L22T_A0
AP29	5 (BC)	5	IO	PB27D	—	L22C_A0
AN29	5 (BC)	6	IO	PB28B	—	—
P22	—	—	VSS	VSS	—	—
AM27	5 (BC)	6	IO	PB28C	—	L23T_D0
AN28	5 (BC)	6	IO	PB28D	VREF_5_06	L23C_D0
AM26	5 (BC)	6	IO	PB29B	—	—
AK22	5 (BC)	6	IO	PB29C	—	L24T_A0
AK23	5 (BC)	6	IO	PB29D	—	L24C_A0
AL25	5 (BC)	7	IO	PB30B	—	—
R13	—	—	VSS	VSS	—	—
AP30	5 (BC)	7	IO	PB30C	—	L25T_A0
AP31	5 (BC)	7	IO	PB30D	—	L25C_A0
AK24	5 (BC)	7	IO	PB31B	—	—
AN15	5 (BC)	—	VDDIO5	VDDIO5	—	—
AM29	5 (BC)	7	IO	PB31C	VREF_5_07	L26T_A0

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
P32	—	—	VDD_ANA	VDD_ANA	—	—
J34	—	—	I	HDINP_AA	—	—
J33	—	—	I	HDINN_AA	—	—
R32	—	—	VDD_ANA	VDD_ANA	—	—
L30	—	—	VDDIB	VDDIB_AA	—	—
K31	—	—	—	REFCLKP_A	—	—
K30	—	—	—	REFCLKN_A	—	—
J31	—	—	O	REXTN_A	—	—
J30	—	—	O	REXT_A	—	—
Y32	—	—	VDD_ANA	VDD_ANA	—	—
G34	—	—	VDDGB_A	VDDGB_A	—	—
G33	—	—	VSS	VSS	—	—
G32	—	—	O	ATMOUT_A (no connect)	—	—
G31	—	—	I	PRESERVE01 (no connect)	—	—
F33	—	—	I	PRESERVE02 (no connect)	—	—
G30	—	—	I	PRESERVE03 (no connect)	—	—
F31	—	—	O	PSYS_RSSIG_ALL	—	—
F30	—	—	I	PSYS_DOBISTN	—	—
E31	—	—	VDD33	VDD33	—	—
AB17	—	—	VDD15	VDD15	—	—
AB18	—	—	VDD15	VDD15	—	—
D32	—	—	I	PBIST_TEST_ENN	—	—
E30	—	—	I	PLOOP_TEST_ENN	—	—
AB19	—	—	VDD15	VDD15	—	—
D31	—	—	I	PASB_PDN	—	—
C32	—	—	I	PMP_TESTCLK	—	—
C31	—	—	VDD33	VDD33	—	—
AJ32	—	—	VDD15	VDD15	—	—
B32	—	—	I	PASB_RESETN	—	—
A33	—	—	I	PASB_TRISTN	—	—
B31	—	—	I	PMP_TESTCLK_ENN	—	—
A32	—	—	I	PASB_TESTCLK	—	—
AK32	—	—	VDD15	VDD15	—	—
AB21	—	—	VSS	VSS	—	—
A31	—	—	VDD33	VDD33	—	—
B30	1 (TC)	7	IO	PT36D	—	—
AB22	—	—	VSS	VSS	—	—
C30	1 (TC)	7	IO	PT36B	—	—
D30	1 (TC)	7	IO	PT35D	—	—
B13	1 (TC)	—	VDDIO1	VDDIO1	—	—
E29	1 (TC)	7	IO	PT35B	—	—
E28	1 (TC)	7	IO	PT34D	VREF_1_07	—
AN33	—	—	VSS	Vss	—	—
D29	1 (TC)	8	IO	PT34B	—	—