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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	372
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort82g5-1f680i

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  - 1—512 x 18 (block-port, two read/two write) with optional built in arbitration.
  - 1—256 x 36 (dual-port, one read/one write).
  - 1—1K x 9 (dual-port, one read/one write).
  - 2—512 x 9 (dual-port, one read/one write for each).
  - 2 RAMS with arbitrary number of words whose sum is 512 or less by 18 (dual-port, one read/one write).
  - Supports joining of RAM blocks.
  - Two 16 x 8-bit content addressable memory (CAM) support.
  - FIFO 512 x 18, 256 x 36, 1K x 9, or dual 512 x 9.
  - Constant multiply (8 x 16 or 16 x 8).
  - Dual variable multiply (8 x 8).
- Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, microprocessor interface (MPI), embedded RAM blocks, and embedded standard cell blocks with 100 MHz bus performance. Included are built-in system registers that act as the control and status center for the device.
- Built-in testability:
  - Full boundary scan (IEEE 1149.1 and Draft 1149.2 JTAG).
  - Programming and readback through boundary scan port compliant to IEEE Draft 1532:D1.7.
  - TS_ALL testability function to 3-state all I/O pins.
  - New temperature-sensing diode.
- Improved built-in clock management with Programmable Phase-Locked Loops (PPLLs) provide optimum clock modification and conditioning for phase, frequency, and duty cycle from 20 MHz up to 420 MHz. Multiplication of the input frequency up to 64x and division of the input frequency down to 1/64x possible.
- New cycle stealing capability allows a typical 15% to 40% internal speed improvement after final place and route. This feature also enables compliance with many setup/hold and clock to out I/O specifications and may provide reduced ground bounce for output buses by allowing flexible delays of switching output buffers.
- Per channel Pseudo-Random Bit Sequence (PRBS) generator and checker in FPGA logic.

Programmable Logic System Features

- PCI local bus compliant for FPGA I/Os.
- Improved PowerPC ® 860 and PowerPC II high-speed synchronous microprocessor interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA logic, RAMs, and embedded standard cell blocks. Glueless interface to synchronous PowerPC processors with user-configurable address space provided.
- New embedded system bus facilitates communication among the microprocessor interface, configuration logic, Embedded Block RAM, FPGA logic, and embedded standard cell blocks.
- Variable size bused readback of configuration data capability with the built-in microprocessor interface and system bus.
- Internal, 3-state, and bidirectional buses with simple control provided by the SLIC.
- New clock routing structures for global and local clocking significantly increases speed and reduces skew (<200 ps for OR4E04).
- New local clock routing structures allow creation of localized clock trees.
- Two new edge clock routing structures allow up to six high-speed clocks on each edge of the device for improved setup/hold and clock to out performance.
- New Double-Data Rate (DDR) and Zero-Bus Turn-around (ZBT) memory interfaces support the latest high-speed memory interfaces.
- New 2x/4x uplink and downlink I/O capabilities interface high-speed external I/Os to reduced speed internal logic.

FPGA Logic Overview

The ORCA Series 4 architecture is a new generation of SRAM-based programmable devices from Lattice. It includes enhancements and innovations geared toward today's high-speed systems on a single chip. Designed with networking applications in mind, the Series 4 family incorporates system-level features that can further reduce logic requirements and increase system speed. ORCA Series 4 devices contain many new patented enhancements and are offered in a variety of packages and speed grades.

The hierarchical architecture of the logic, clocks, routing, RAM, and system-level blocks create a seamless merge of FPGA and ASIC designs. Modular hardware and software technologies enable System-on-Chip integration with true plug-and-play design implementation.

The architecture consists of four basic elements: Programmable Logic Cells (PLCs), Programmable I/O cells (PIOs), Embedded Block RAMs (EBRs), plus supporting system-level features. These elements are interconnected with a rich routing fabric of both global and local wires. An array of PLCs is surrounded by common interface blocks which provide an abundant interface to the adjacent PLCs or system blocks. Routing congestion around these critical blocks is eliminated by the use of the same routing fabric implemented within the programmable logic core.

Each PLC contains a PFU, SLIC, local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU, but decoders, PAL-like functions, and 3-state buffering can be performed in the SLIC. The PIOs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, uplink and downlink functions, and other functions on two output signals.

Large blocks of 512 x 18 block-port RAM complement the existing distributed PFU memory. The RAM blocks can be used to implement RAM, ROM, FIFO, multiplier, and CAM. Some of the other system-level functions include the MPI, PLLs, and the Embedded System Bus (ESB).

PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) LUTs, eight latches/FFs, and one additional Flip-Flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-block fashion; two sets of four LUTs and FFs that can be controlled independently. Each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth FF for pipelining.

Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The FFs (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The FFs also have programmable clock polarity, clock enables, and local set/reset.

The SLIC is connected from PLC routing resources and from the outputs of the PFU. It contains eight 3-state, bidirectional buffers, and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT to perform PAL-like functions. The 3-state drivers in the SLIC and their direct connections from the PFU outputs make fast, true, 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

Programmable I/O

The Series 4 PIO addresses the demand for the flexibility to select I/Os that meet system interface requirements. I/Os can be programmed in the same manner as in previous ORCA devices, with the additional new features which allow the user the flexibility to select new I/O types that support High-Speed Interfaces.

Each PIO contains four programmable I/O pads and is interfaced through a common interface block to the FPGA array. The PIO is split into two pairs of I/O pads with each pair having independent clock enables, local set/reset, and global set/reset. On the input side, each PIO contains a programmable latch/Flip-Flop which enables very fast latching of data from any pad. The combination provides for very low setup requirements and zero hold times for

System Bus

An on-chip, multimaster, 8-bit system bus with 1-bit parity facilitates communication among the MPI, configuration logic, FPGA control, status registers, Embedded Block RAMs, as well as user logic. Utilizing the AMBA specification Rev 2.0 AHB protocol, the Embedded System Bus offers arbiter, decoder, master, and slave elements. Master and slave elements are also available for the user-logic and a slave interface is used for control and status of the embedded backplane transceiver portion of the device.

The system bus control registers can provide control to the FPGA such as signaling for reprogramming, reset functions, and PLL programming. Status registers monitor INIT, DONE, and system bus errors. An interrupt controller is integrated to provide up to eight possible interrupt resources. Bus clock generation can be sourced from the microprocessor interface clock, configuration clock (for slave configuration modes), internal oscillator, user clock from routing, or from the port clock (for JTAG configuration modes).

Phase-Locked Loops

Up to eight PLLs are provided on each Series 4 device, with four user PLLs generally provided for FPSCs. Programmable PLLs can be used to manipulate the frequency, phase, and duty cycle of a clock signal. Each PPLL is capable of manipulating and conditioning clocks from 20 MHz to 200 MHz. Frequencies can be adjusted from 1/8x to 8x, the input clock frequency. Each programmable PLL provides two outputs that have different multiplication factors but can have the same phase relationships. Duty cycles and phase delays can be adjusted in 12.5% of the clock period increments. An automatic input buffer delay compensation mode is available for phase delay. Each PPLL provides two outputs that can have programmable (12.5% steps) phase differences.

Embedded Block RAM

New 512 x 18 block-port RAM blocks are embedded in the FPGA core to significantly increase the amount of memory and complement the distributed PFU memories. The EBRs include two write ports, two read ports, and two byte lane enables which provide four-port operation. Optional arbitration between the two write ports is available, as well as direct connection to the high-speed system bus.

Additional logic has been incorporated to allow significant flexibility for FIFO, constant multiply, and two-variable multiply functions. The user can configure FIFO blocks with flexible depths of 512K, 256K, and 1K including asynchronous and synchronous modes and programmable status and error flags. Multiplier capabilities allow a multiple of an 8-bit number with a 16-bit fixed coefficient or vice versa (24-bit output), or a multiple of two 8-bit numbers (16-bit output). On-the-fly coefficient modifications are available through the second read/write port.

Two 16 x 8-bit CAMs per embedded block can be implemented in single match, multiple match, and clear modes. The EBRs can also be preloaded at device configuration time.

Configuration

The FPGAs functionality is determined by internal configuration RAM. The FPGAs internal initialization/configuration circuitry loads the configuration data at power up or under system control. The configuration data can reside externally in an EEPROM or any other storage media. Serial EEPROMs provide a simple, low pin-count method for configuring FPGAs.

The RAM is loaded by using one of several configuration modes. Supporting the traditional master/slave serial, master/slave parallel, and asynchronous peripheral modes, the Series 4 also utilizes its microprocessor interface and Embedded System Bus to perform both programming and readback. Daisy chaining of multiple devices and partial reconfiguration are also permitted.

Other configuration options include the initialization of the embedded-block RAM memories and FPSC memory as well as system bus options and bit stream error checking. Programming and readback through the JTAG (IEEE 1149.2) port is also available meeting In-System Programming (ISP™) standards (IEEE 1532 Draft).

Additional Information

Contact your local Lattice representative for additional information regarding the ORCA Series 4 FPGA devices, or visit the Lattice web site at www.latticesemi.com.

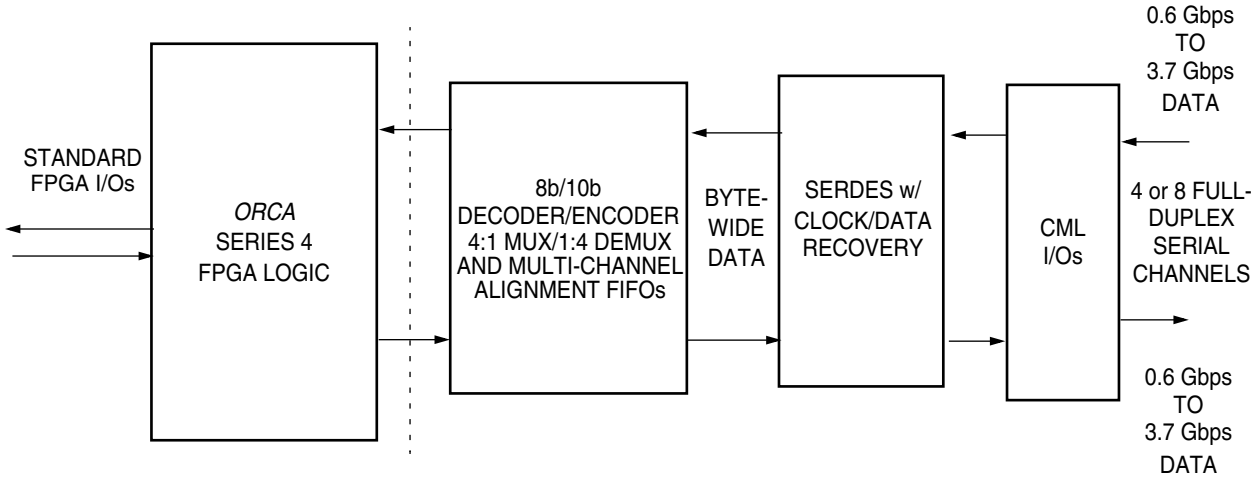
ORT42G5/ORT82G5 Overview

The ORT42G5 and ORT82G5 FPSCs provide high-speed backplane transceivers combined with FPGA logic. They are based on the 1.5V OR4E04 ORCA FPGA and have 36 x 36 arrays of Programmable Logic Cells (PLCs). The embedded core, which contains the backplane transceivers is attached to the right side of the device and is integrated directly into the FPGA array. A top level diagram of the basic chip configuration is shown in Figure 1.

Embedded Core Overview

The embedded core portions of the ORT42G5 and ORT82G5 contain respectively four or eight Clock and Data Recovery (CDR) macrocells and Serialize/Deserialize (SERDES) blocks and support 8b/10b (*IEEE* 802.3.2002) encoded serial links. It is intended for high-speed serial backplane data transmission. Figure 1 shows the ORT42G5 and ORT82G5 top level block diagram and the basic data flow. Boundary scan for the ORT42G5/ORT82G5 only includes programmable I/Os and does not include any of the embedded block I/Os.

Figure 1. ORT42G5/ORT82G5 Top Level Block Diagram



The serial channels can each operate at up to 3.7 Gbps (2.96 Gbps data rate) with a full-duplex synchronous interface with built-in clock recovery (CDR). The 8b/10b encoding provides guaranteed ones density for the CDR, byte alignment, and error detection. The core is also capable of frame synchronization and physical link monitoring and contains independent 4k x 36 RAM blocks. Overviews of the various blocks in the embedded core are presented in the following paragraphs.

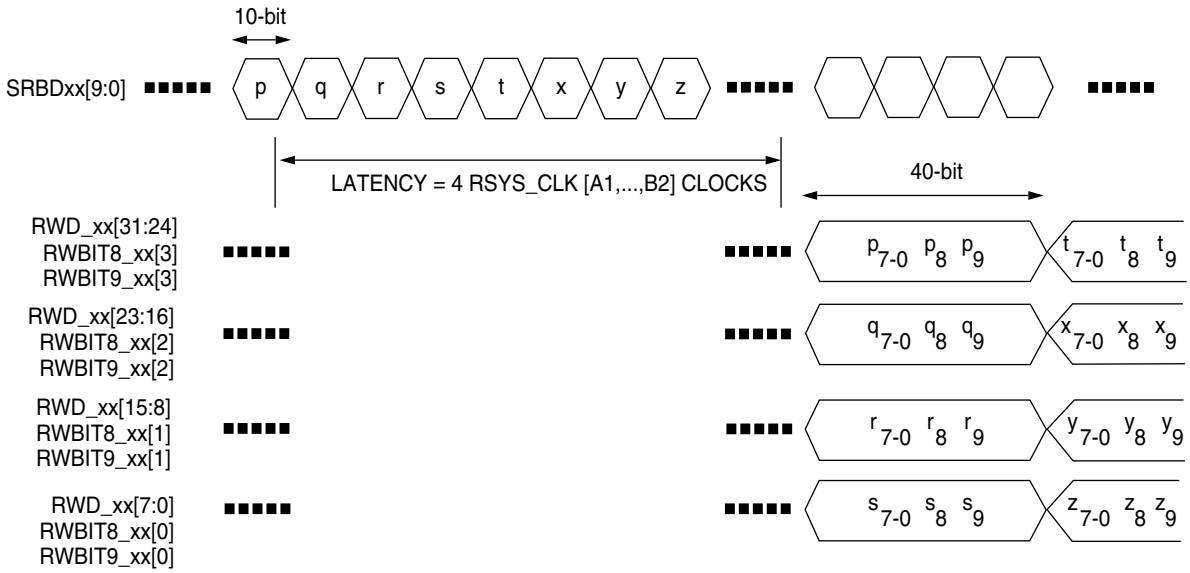
Serializer and Deserializer (SERDES)

The SERDES portion of the core contains two transceiver blocks for serial data transmission at a selectable data rate of 0.6 to 3.7 Gbps. Each SERDES channel features high-speed 8b/10b parallel I/O interfaces to other core blocks and high-speed CML interfaces to the serial links.

The SERDES circuitry consists of receiver, transmitter, and auxiliary functional blocks. The receiver accepts high-speed (up to 3.7 Gbps) serial data. Based on data transitions, the receiver locks an analog receive PLL for each channel to retime the data, then demultiplexes the data down to parallel bytes and an accompanying clock.

The transmitter operates in the reverse direction. Parallel bytes are multiplexed up to 3.7 Gbps serial data for off-chip communication. The transmitter generates the necessary 3.7 GHz clocks for operation from a lower speed reference clock.

Figure 8. Receive DEMUX Block for a Single SERDES Channel



One clock per block of two or four channels, called RCK78[A,B], is sent to the FPGA. The control bits RCKSEL[A,B] are used to select the channel that is the source for these clocks.

Link State Machines

Two link state machines are included in the device, one for XAUI applications and a second for Fibre Channel applications.

The Fibre Channel link state machine is responsible for establishing a valid link between the transmitter and the receiver and for maintaining link synchronization. The machine is initially in the Loss Of Synchronization (LOS) state upon power-on reset. This is indicated by WDSYNC_xx = 0. While in this state, the machine looks for a particular number of consecutive idle ordered sets without any invalid data transmission in between before declaring synchronization achieved. Achievement of synchronization is indicated by asserting WDSYNC_xx = 1. Specifically, the machine looks for three continuous idle ordered sets without any misaligned comma character or any running disparity based code violation in between. In the event of any such code violation, the machine would reset itself to the ground state and start its search for the idle ordered sets again. A typical valid sequence for achieving link synchronization would be K28.5 D21.4 D21.5 D21.5 repeated three times.

In the synchronization achieved state, the machine constantly monitors the received data and looks for any kind of code violation that might result due to running disparity errors. If it were to receive four such consecutive invalid words, the link machine loses its synchronization and once again enters the loss of synchronization state (LOS). A pair of valid words received by the machine overcomes the effect of a previously encountered code violation. LOS is indicated by the status of WDSYNC_xx output which now transitions from 1 to 0. At this point the machine attempts to establish the link yet again. Figure 9 shows the state diagram for the Fibre Channel link state machine.

LOS is also indicated by DEMUXWAS_xx status register bit. This bit is set to 0 during loss of synchronization.

Multi-channel Alignment

The alignment FIFO allows the transfer of all data to the system clock. The Multi-Channel Alignment block (Figure 6) allows the system to be configured to allow the frame alignment of multiple slightly varying data streams. This optional alignment ensures that matching SERDES streams will arrive at the FPGA end in perfect data synchronization.

Each channel is provided with a 24 word x 36-bit FIFO. The FIFO can perform two tasks: (1) to change the clock domain from receive clock to a clock from the FPGA side, and (2) to align the receive data over 2, 4, or 8 channels. This FIFO allows a timing budget of ±230.4 ns that can be allocated to skew between the data lanes and for transfer to the system clock. The input to the FIFO consists of 36 bits of demultiplexed data, RALIGN_xx[3:0], RWD_xx[31:0], and RWBIT8_xx[3:0].

The four RALIGN_xx bits are control signals, and can be the alignment character detect signals indicating the presence of a comma character in Fibre Channel mode and the /A/ character in XAUI mode. The other 32 RWD_xx bits are the 8-bit data bytes from the 8b/10b decoder. The alignment character, if present, is the MSB of the data. The RWBIT8_xx indicates the presence of a Km.n control character in the receive data byte. Only RWBIT8_xx and RWD_xx inputs are stored in the FIFO. During alignment process, RALIGN[3]_xx is used to synchronize multiple channels.

If a channel is not in any alignment group, it will set the FIFO-write-address to the beginning of the FIFO, and will set the FIFO-read-address to the middle of the FIFO, at the first assertion of RALIGN[3]_xx after reset or after the resync command.

The RX_FIFO_MIN_xx register bits can be used to control the threshold for minimum unused buffer space in the alignment FIFOs between read and write pointers before overflow (OVFL) status is flagged. The synchronization algorithm consists of a down counter which starts to count down by 1 from its initial value of 18 (decimal) when an alignment character from any channel within an alignment group has been received. Once all the alignment characters within the alignment group have been received, the count is decremented by 2 until 0 is reached. Data is then read from the FIFOs and output to the FPGA. This algorithm is not repeated after multi-channel alignment has been achieved; resynchronization must be forced by toggling the appropriate FMPU_RESYNC bit.

ORT42G5 Multi-channel Alignment

The ORT42G5 has a total of four channels. The incoming data of these channels can be synchronized in two ways or they can be independent of one other. Two channels, C and D, within either SERDES block can be aligned together to form a pair, as shown in Figure 11. Alternately, all four channels can be aligned together to form a communication channel with a bandwidth of 10 Gbps, as shown in Figure 12. Individual channels within an alignment group can be disabled (i.e., powered down) without disrupting other channels.

Figure 11. Dual Channel Alignment

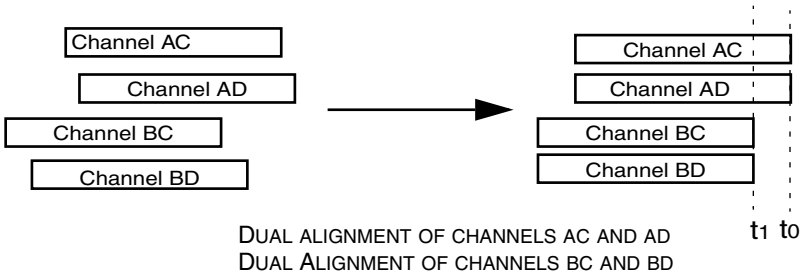
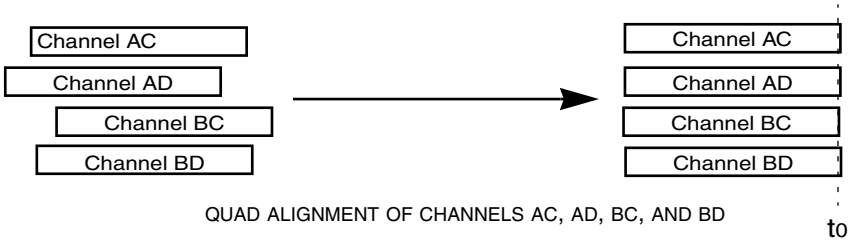


Figure 12. Four Channel Alignment of SERDES Blocks A and B



ORT82G5 Multi-channel Alignment

The ORT82G5 has a total of eight channels (four per SERDES block). The incoming data of these channels can be synchronized in several ways or they can be independent of one other. Two channels within a SERDES block can be aligned together. Channel A and B and/or channel C and D can form a pair as shown in Figure 13. Alternately, all four channels of a SERDES block can be aligned together to form a communication channel with a bandwidth of 10 Gbps as shown in Figure 14. Finally, the alignment can be extended across both SERDES block to align all eight channels in ORT82G5 as shown in Figure 15. Individual channels within an alignment group can be disabled (i.e., powered down) without disrupting other channels.

Figure 13. Dual Channel Alignment

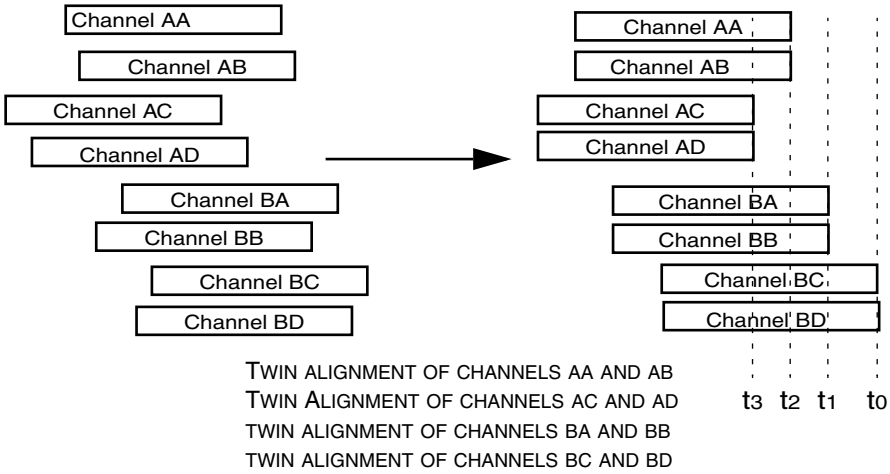
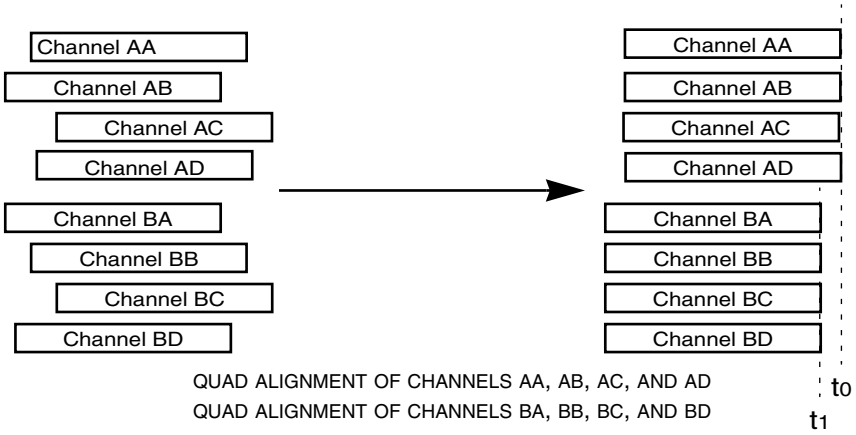


Figure 14. Alignment of SERDES Quads A and B



Start Up Sequence for the ORT82G5

The following sequence is required by the ORT82G5 device. For information required for simulation that may be different than this sequence, see the ORT82G5 Design Kit.

1. Initiate a hardware reset by making PASB_RESETN low. Keep this low during FPGA configuration of the device. The device will be ready for operation 3 ms after the low to high transition of PASB_RESETN.

2. Configure the following SERDES internal and external registers. Note that after device initialization, all alarm and status bits should be read once to clear them. A subsequent read will provide the valid state. Set the following bits in register 30800:
   – Bits LCKREFN_[AA:AD] to 1, which implies lock to data.
   – Bits ENBYSYNC_[AA:AD] to 1 which enables dynamic alignment to comma.

   Set the following bits in register 30801:
   – Bits LOOPENB_[AA:AD] to 1 if high-speed serial loopback is desired.

   Set the following bits in register 30900:
   – Bits LCKREFN_[BA:BD] to 1 which implies lock to data.
   – Bits ENBYSYNC_[BA:BD] to 1 which enables dynamic alignment to comma.

   Set the following bits in register 30901:
   – Bits LOOPENB_[BA:BD] to 1 if high-speed serial loopback is desired.

   Set the following bits in registers 30002, 30012, 30022, 30032, 30102, 30112, 30122, 30132:
   – TXHR set to 1 if TX half-rate is desired.
   – 8B10BT set to 1

   Set the following bits in registers 30003, 30013, 30023, 30033, 30103, 30113, 30123, 30133:
   – RXHR Set to 1 if RX half-rate is desired.
   – 8B10BR set to 1.
   – LINKSM set to 1 if the Fibre Channel state machine is desired.

   Assert GSWRST bit by writing two 1's. Deassert GSWRST bit by writing two 0's. Wait 3ms. If higher speed serial loopback has been selected, the receive PLLs will use this time to lock to the new serial data.

   Monitor the following alarm bits in registers 30000, 30010, 30020, 30030, 30100, 30110, 30120, 30130:
   – LKI, PLL lock indicator. 1 indicates that PLL has achieved lock.

3. If 8b/10b mode is enabled, enable link synchronization by periodically sending the following sequence three times:
   – K28.5 D21.4 D21.5 D21.5 or any other idle ordered set (starting with a /comma/) in FC mode.
   – /comma/ characters for the XAUI state machine and /A/ characters for word and channel alignment in XAUI mode.

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30933	[0:3]	—	00	Reserved for future use.
	[4:5]	—		Reserved for future use.
	[6]	—		Reserved for future use.
	[7]	—		Reserved for future use.
Status Registers (Read Only, Clear on Read), xx = [AC, AD, BC or BD]				
30804 - Ax 30904 - Bx	[0:1]	—	00	Reserved for future use.
	[2:3]	—		Reserved for future use.
	[4:5]	XAUISTAT_xC		XAUI Status Register. Status of XAUI link state machine for Channel xC 00 – No synchronization, 10 – Synchronization done, 11 – Not used, 01 – no_comma (see XAUI state machine) and at least one CV detected. XAUISTAT_xC[0:1] = 00 on device reset.
	[6:7]	XAUISTAT_xD		XAUI Status Register. Status of XAUI link state machine for Channel xD 00 – No synchronization, 10 – Synchronization done, 11 – Not used, 01 – no_comma (see XAUI state machine) and at least one CV detected. XAUISTAT_xD[0:1] = 00 on device reset.
30805 - Ax 30905 - Bx	[0]]	—	00	Reserved for future use.
	[1]	—		Reserved for future use.
	[2]	DEMUXWAS_xC		Status of Word Alignment. When DEMUX_WAS_xC=1, word alignment is achieved for Channel xC. DEMUX_WAS_xC=0 on device reset.
	[3]	DEMUXWAS_xD		Status of Word Alignment. When DEMUX_WAS_xD=1, word alignment is achieved for Channel xD. DEMUX_WAS_xD=0 on device reset.
	[4]	—		Reserved for future use.
	[5]	—		Reserved for future use.
	[6]	CH24_SYNC_xC		Status of Channel Alignment. When CH24_SYNC_xC=1, multi-channel alignment is achieved for Channel xC. CH24_SYNC_xC=0 on device reset.
	[7]	CH24_SYNC_xD		Status of Channel Alignment. When CH24_SYNC_xD=1, multi-channel alignment is achieved for Channel xD. CH24_SYNC_xD=0 on device reset.
30814 - A 30914 - B	[0]	—	00	Reserved for future use.
	[1]	SYNC2_[A:B]_OVFL		Multi-Channel Overflow Status. When SYNC2_[A:B]_OVFL=1, twin channel synchronization FIFO overflow has occurred. SYNC2_[A:B]_OVFL=0 on device reset.
	[2:3]	—		Reserved for future use.
	[4]	SYNC2_[A:B]_OOS		Multi-Channel Out-Of-Sync Status. When SYNC2_[A:B]_OOS=1, twin channel synchronization has failed. SYNC2_[A:B]_OOS=0 on device reset.
	[5:7]	—		Reserved for future use.

Table 30. ORT82G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30810 - Ax 30910 - Bx	[0]xA [1]xB [2]xC [3]xD	DOWDALIGN_xx	00	Word Realign Bit. When DOWDALIGN_xx transitions from 0 to 1, the receiver realigns on the next comma character for Channel xx. NOWDALIGN_xx=0 on device reset.
	[4]xA [5]xB [6]xC [7]xD	FMPU_STR_EN_xx		Enable multi-channel alignment for Channel xx. When FMPU_STR_EN_xx=1, the corresponding channel participates in multi-channel alignment. FMPU_STR_EN_xx=0 on device reset.
30811 - Ax 30911 - Bx	[0:1] xA [2:3] xB [4:5] xC [6:7] xD	FMPU_SYNMODE_xx[0:1]	00	Sync mode for xx 00 = No channel alignment 10 = Twin channel alignment 01 = Quad channel alignment 11 = Eight channel alignment
30820 - Ax 30920 - Bx	[0]xA [1]xB [2]xC [3]xD	FMPU_RESYNC1_xx	00	Resync a Single Channel. When FMPU_RESYNC1_xx transitions from 0 to 1, the corresponding channel is resynchronized (the write and read pointers are reset). FMPU_STR_EN_xx=0 on device reset.
	[4] xA & xB [5] xC & xD	FMPU_RESYNC2_x[1:2]		Resync a Pair of Channels. When FMPU_RESYNC2_[A:B][1:2] transitions from a 0 to a 1, the corresponding channel pair is resynchronized. FFMPU_RESYNC2_[A:B][1:2]=0 on device reset.
	[6]	FMPU_RESYNC4[A:B]		Resync a Four-Channel Group. When FMPU_RESYNC4[A:B] transitions from a 0 to a 1, the corresponding four-channel group is resynchronized. FMPU_RESYNC4[A:B]=0 on device reset.
	[7]	XAUI_MODE[A:B]		Controls use of XAUI link state machine in place of Fibre-Channel state machine. When XAUI_MODE[A:B]=1, all four channels in the SERDES quad enable their XAUI link state machines. (LINKSM_xx bits are ignored). XAUI_MODE[A:B]=0 on device reset.
30821 - A 30921 - B	[0]	NOCHALGN [A:B]	00	Bypass channel alignment. NOCHALGN [A:B] =1 causes bypassing of multi-channel alignment FIFOs for the corresponding SERDES quad. NOCHALGN [A:B] =0 on device reset.
	[1:7]	Reserved for future use.		
30933	[0:3]	Reserved for future use.		
	[4:5]	SCHAR_CHAN[0:1]	00	Select channel to test 00 = Channel BA 10 = Channel BB 01 =Channel BC 11 = Channel BD
	[6]	SCHAR_TXSEL		1=Select TX option 0=Select RX option
	[7]	SCHAR_ENA		1=Enable Characterization of SERDES B
Status Registers (Read Only), xx=[AA,...,BD]				
30804 - Ax 30904 - Bx	[0:1] xA [2:3] xB [4:5] xC [6:7] xD	XAUISTAT_xx[0:1]	00	XAUI Status Register. Status of XAUI link state machine for Channel xx 00 – No synchronization. 10 – Synchronization done. 11 – Not used. 01 – no_comma (see XAUI state machine) and at least one CV detected XAUISTAT_xx[0:1] = 00 on device reset.

Table 30. ORT82G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30A02	[0:1]	RX_FIFO_MIN	00	MSb's for the threshold for low address in RX_FIFOs. RX_FIFO_MIN, Bit 1 is MSb. Useful values for RX_FIFO_MIN [0:4] are 0 to 17(decimal).
	[2]	FMPU_RESYNC8		Resynchronizes all 8 channels when it transitions from 0 to 1. Status is a 0 on device reset.
	[3:7]	—		Reserved for future use.
Common Status Registers xx=[AA,...,BD]				
30A03	[0]	SYNC8_OVFL	00	Read-Only Multi-Channel Overflow Status. When SYNC8_OVFL=1, 8-channel synchronization FIFO overflow has occurred. SYNC8_OVFL=0 on device reset.
	[1]	SYNC8_OOS		Read-Only Multi-Channel Out-Of-Sync Status. When SYNC8_OOS=1, 8-channel synchronization has failed. SYNC8_OOS=0 on device reset.
	[2:7]	Reserved for future use.		

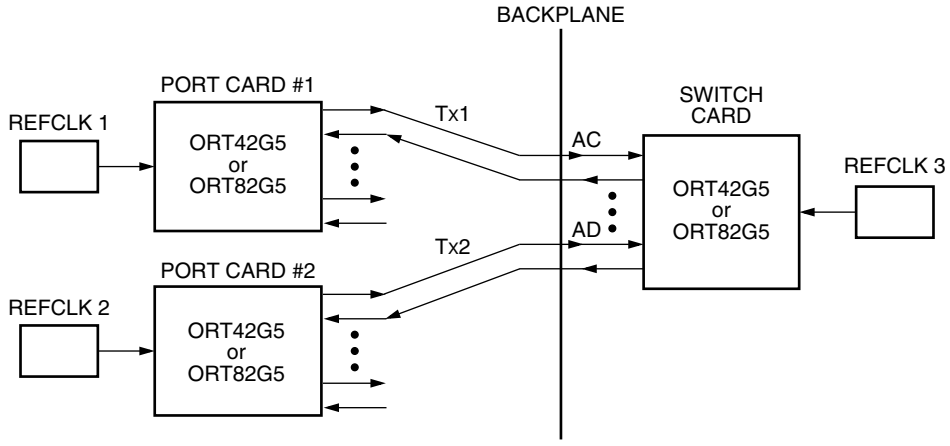
Recommended Board-level Clocking for the ORT42G5 and ORT82G5

Option 1: Asynchronous Reference Clocks Between Rx and Tx Devices

Each board that uses the ORT42G5 or ORT82G5 as a transmit or receive device will have its own local reference clock as shown in Figure 37. Figure 37 shows the ORT82G5 device on the switch card receiving data on two of its channels from a separate source. Data tx1 is transmitted from a tx device with refclk1 as the reference clock and Data tx2 is transmitted from a tx device with refclk2 as the reference clock. Receive channel AA locks to the incoming data tx1 and receive channel AB locks to the incoming data tx2.

The advantage of this clocking scheme is the fact that it is not necessary to distribute a reference clock (typically 156 MHz for 10GE and 155.52 MHz for OC-192 applications) across a backplane.

Figure 37. Asynchronous Clocking Between Rx and Tx Devices



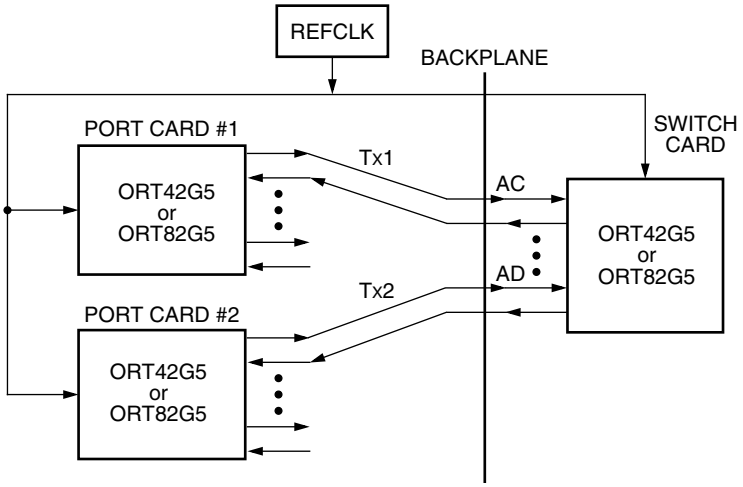
Option 2: Synchronous Reference Clocks to Rx and Tx Devices

In this type of clocking, a single reference clock is distributed to all receive and transmit devices in a system (Figure 38). This distributed clocking scheme will permit maximum flexibility in the usage of transmit and receive channels in the current silicon such as:

- All transmit and receive channels can be used within any quad in receive channel alignment or alignment bypass mode.
- In channel alignment mode, each receive channel operates on its own independent clock domain.

The disadvantage with this scheme is the fact that it is difficult to distribute a 156 MHz reference clock across a backplane. This may require expensive clock driver chips on the board to drive clocks to different destinations within the specified jitter limits for the reference clock.

Figure 38. Distributed Reference Clock to Rx And Tx Devices



Input Eye-Mask Characterization

Figure 39. provides an eye-mask characterization of the SERDES receiver input. The eye-mask is specified below for two different eye-mask heights. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance. Almost all detrimental characteristics of transmit signal and the interconnection link design result in eye-closure. This, combined with the eye-opening limitations of the line receiver, can provide a good indication of a link's ability to transfer data error-free.

The Clock and Data Recovery (CDR) portion of the ORT42G5 and ORT82G5 SERDES receiver has the ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth (about 3 MHz). The eye-mask specifications of Table 37 are for jitter frequencies above the PLL bandwidth of the CDR, which is a worst case condition. When jitter occurs at frequencies below the PLL bandwidth, the receiver jitter tolerance is significantly better. For this case error-free data detection can occur even with a completely closed eye-mask.

Figure 39. Receive Data Eye-Diagram Template (Differential)

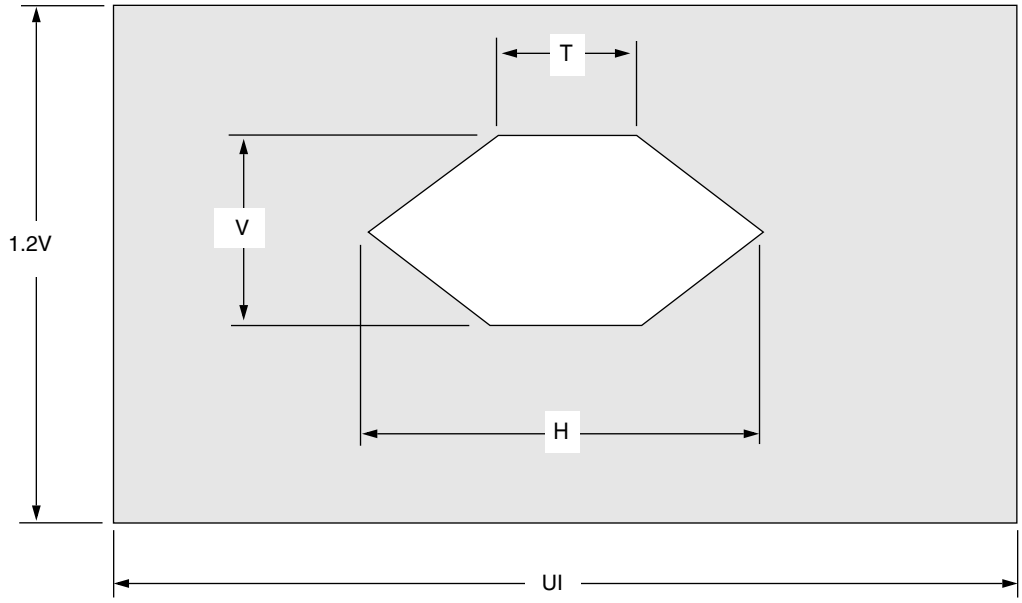


Table 37. Receiver Eye-Mask Specifications[1]

Parameter	Conditions	Value	Unit
Input Data			
Eye Opening Width (H)@ 3.125Gbps	V=175 mV diff[1]	0.55	UIP-P
Eye Opening Width (T)@ 3.125Gbps	V=175 mV diff[1]	0.15	UIP-P
Eye Opening Width (H)@ 3.125Gbps	V=600 mV diff[1]	0.35	UIP-P
Eye Opening Width (T)@ 3.125Gbps	V=600 mV diff[1]	0.10	UIP-P
Eye Opening Width (H)@ 2.5Gbps	V=175 mV diff[1]	0.42	UIP-P
Eye Opening Width (T)@ 2.5Gbps	V=175 mV diff[1]	0.15	UIP-P
Eye Opening Width (H)@ 2.5Gbps	V=600 mV diff[1]	0.33	UIP-P
Eye Opening Width (T)@ 2.5Gbps	V=600 mV diff[1]	0.10	UIP-P

1. With PRBS 2^7-1 data pattern, 10 MHz sinusoidal jitter, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., T_A = 0ºC to 85ºC, 1.425V to 1.575V supply.

- Example connections are shown in Figure 40. The naming convention for the power supply sources shown in the figure are as follows:
  - Supply_1.5V – Tx-Rx digital, auxiliary power pins.
  - Supply_VDDIB – Input Rx buffer power pins.
  - Supply_VDDOB – Output Tx buffer power pins.
  - Supply_VDDANA – Tx analog power pins, Rx analog power pins, guard band power pins.

Figure 40. Power Supply Filtering

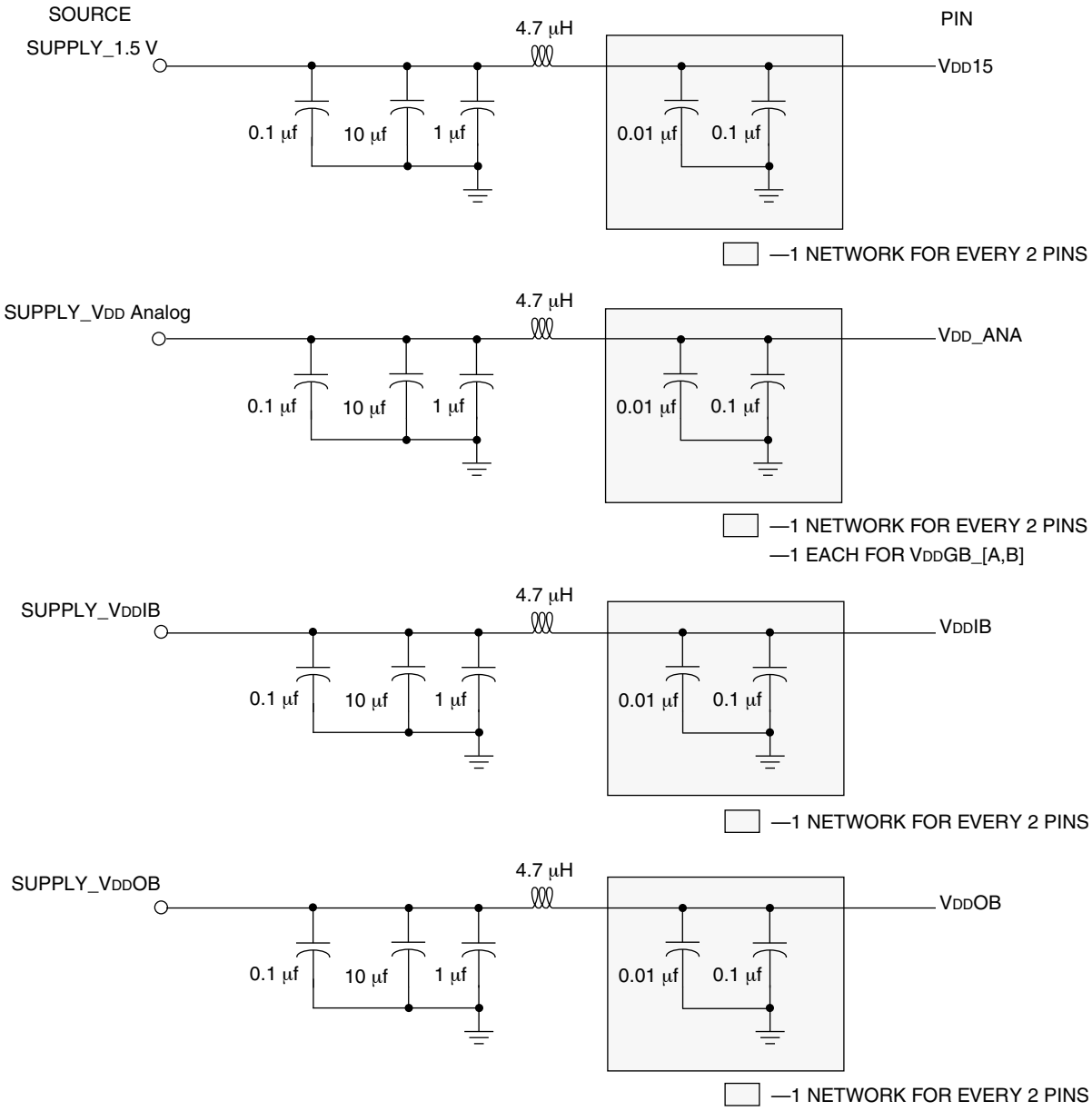


Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
G9	-	-	VSS	VSS	-	-
L3	7 (CL)	5	IO	PL21D	A10/PPC_A24	L10C
L4	7 (CL)	5	IO	PL21C	A9/PPC_A23	L10T
L5	7 (CL)	5	IO	PL22D	A8/PPC_A22	-
F10	-	-	VDD15	VDD15	-	-
G10	-	-	VSS	VSS	-	-
M3	7 (CL)	6	IO	PL24D	PLCK1C	L11C
M4	7 (CL)	6	IO	PL24C	PLCK1T	L11T
N4	7 (CL)	6	IO	PL25C	A7/PPC_A21	-
M2	7 (CL)	6	IO	PL26D	A6/PPC_A20	L12C
M1	7 (CL)	6	IO	PL26C	A5/PPC_A19	L12T
N3	7 (CL)	7	IO	PL27D	WR_N/MPI_RW	-
F11	-	-	VDD15	VDD15	-	-
N5	7 (CL)	8	IO	PL28D	A4/PPC_A18	-
M5	7 (CL)	-	VDDIO7	VDDIO7	-	-
N2	7 (CL)	8	IO	PL29D	A3/PPC_A17	L13C
N1	7 (CL)	8	IO	PL29C	A2/PPC_A16	L13T
G11	-	-	VSS	VSS	-	-
P2	7 (CL)	8	IO	PL30D	A1/PPC_A15	L14C
P1	7 (CL)	8	IO	PL30C	A0/PPC_A14	L14T
F12	-	-	VDD15	VDD15	-	-
P3	7 (CL)	8	IO	PL31D	DP0	L15C
P4	7 (CL)	8	IO	PL31C	DP1	L15T
R4	6 (BL)	1	IO	PL32D	D8	L16C
R3	6 (BL)	1	IO	PL32C	VREF_6_01	L16T
R2	6 (BL)	1	IO	PL33D	D9	L17C
R1	6 (BL)	1	IO	PL33C	D10	L17T
G12	-	-	VSS	VSS	-	-
T3	6 (BL)	2	IO	PL34D	-	-
P5	6 (BL)	-	VDDIO6	VDDIO6	-	-
T2	6 (BL)	2	IO	PL34B	-	L18C
T1	6 (BL)	2	IO	PL34A	-	L18T
U1	6 (BL)	3	IO	PL35B	D11	L19C
U2	6 (BL)	3	IO	PL35A	D12	L19T
R5	6 (BL)	-	VDDIO6	VDDIO6	-	-
V1	6 (BL)	3	IO	PL36B	VREF_6_03	L20C
V2	6 (BL)	3	IO	PL36A	D13	L20T
G13	-	-	VSS	VSS	-	-
W2	6 (BL)	4	IO	PL37B	-	L21C
W1	6 (BL)	4	IO	PL37A	VREF_6_04	L21T
Y1	6 (BL)	4	IO	PL39D	PLL_CK7C/HPPLL	L22C
Y2	6 (BL)	4	IO	PL39C	PLL_CK7T/HPPLL	L22T
U3	-	-	I	PTEMP	PTEMP	-
F13	-	-	VDD15	VDD15	-	-

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
T22	-	-	I	HDINP_BC	-	HSP_2
J19	-	-	VDD_ANA	VDD_ANA	-	-
F20	-	-	VSS	VSS	-	-
K16	-	-	VDD_ANA	VDD_ANA	-	-
R20	-	-	VDDOB	VDDOB_BC	-	-
R21	-	-	O	HDOUTN_BC	-	HSN_3
G19	-	-	VSS	VSS	-	-
R22	-	-	O	HDOUTP_BC	-	HSP_3
P21	-	-	VDDOB	VDDOB_BC	-	-
H16	-	-	VSS	VSS	-	-
P22	-	-	VDDIB	VDDIB_BD	-	-
K17	-	-	VDD_ANA	VDD_ANA	-	-
N22	-	-	I	HDINN_BD	-	HSN_4
H17	-	-	VSS	VSS	-	-
N21	-	-	I	HDINP_BD	-	HSP_4
K18	-	-	VDD_ANA	VDD_ANA	-	-
H18	-	-	VSS	VSS	-	-
K19	-	-	VDD_ANA	VDD_ANA	-	-
P20	-	-	VDDOB	VDDOB_BD	-	-
M22	-	-	O	HDOUTN_BD	-	HSN_5
H19	-	-	VSS	VSS	-	-
M21	-	-	O	HDOUTP_BD	-	HSP_5
N20	-	-	VDDOB	VDDOB_BD	-	-
L16	-	-	VSS	VSS	-	-
L17	-	-	VSS	VSS	-	-
M20	-	-	VDDOB	VDDOB_AD	-	-
L22	-	-	O	HDOUTP_AD	-	HSP_6
L18	-	-	VSS	VSS	-	-
L21	-	-	O	HDOUTN_AD	-	HSN_6
L20	-	-	VDDOB	VDDOB_AD	-	-
N16	-	-	VDD_ANA	VDD_ANA	-	-
L19	-	-	VSS	VSS	-	-
N17	-	-	VDD_ANA	VDD_ANA	-	-
K22	-	-	I	HDINP_AD	-	HSP_7
M16	-	-	VSS	VSS	-	-
K21	-	-	I	HDINN_AD	-	HSN_7
N18	-	-	VDD_ANA	VDD_ANA	-	-
K20	-	-	VDDIB	VDDIB_AD	-	-
M17	-	-	VSS	VSS	-	-
J20	-	-	VDDOB	VDDOB_AC	-	-
J21	-	-	O	HDOUTP_AC	-	HSP_8
M18	-	-	VSS	VSS	-	-
J22	-	-	O	HDOUTN_AC	-	HSN_8
H20	-	-	VDDOB	VDDOB_AC	-	-

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
L11	-	-	VSS	VSS	-	-
N15	-	-	VDD15	VDD15	-	-
D10	1 (TC)	5	IO	PT18D	PTCK1C	L68C
C10	1 (TC)	5	IO	PT18C	PTCK1T	L68T
A12	1 (TC)	5	IO	PT17D	PTCK0C	L69C
B12	1 (TC)	5	IO	PT17C	PTCK0T	L69T
P6	-	-	VDD15	VDD15	-	-
A11	1 (TC)	5	IO	PT16D	VREF_1_05	L70C
B11	1 (TC)	5	IO	PT16C	-	L70T
L12	-	-	VSS	VSS	-	-
D9	1 (TC)	6	IO	PT15D	-	L71C
C9	1 (TC)	6	IO	PT15C	-	L71T
G15	1 (TC)	-	VDDIO1	VDDIO1	-	-
B10	1 (TC)	6	IO	PT14D	-	L72C
A10	1 (TC)	6	IO	PT14C	VREF_1_06	L72T
B9	0 (TL)	1	IO	PT13D	MPI_RTRY_N	L73C
A9	0 (TL)	1	IO	PT13C	MPI_ACK_N	L73T
D8	0 (TL)	1	IO	PT12D	M0	L74C
C8	0 (TL)	1	IO	PT12C	M1	L74T
A22	-	-	VSS	VSS	-	-
B8	0 (TL)	2	IO	PT12B	MPI_CLK	L75C
A8	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L75T
C7	0 (TL)	2	IO	PT11D	M2	L76C
D7	0 (TL)	2	IO	PT11C	M3	L76T
E9	0 (TL)	-	VDDIO0	VDDIO0	-	-
E6	0 (TL)	2	IO	PT11A	MPI_TEA_N	-
F6	-	-	VDD15	VDD15	-	-
B7	0 (TL)	3	IO	PT9D	VREF_0_03	L77C
A7	0 (TL)	3	IO	PT9C	-	L77T
A6	0 (TL)	3	IO	PT8D	D0	L78C
B6	0 (TL)	3	IO	PT8C	TMS	L78T
C6	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L79C
D6	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L79T
B1	-	-	VSS	VSS	-	-
A5	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L80C
B5	0 (TL)	4	IO	PT6C	D3	L80T
C5	0 (TL)	5	IO	PT5D	D1	L81C
D5	0 (TL)	5	IO	PT5C	D2	L81T
B2	-	-	VSS	VSS	-	-
A4	0 (TL)	5	IO	PT4D	TDI	L82C
B4	0 (TL)	5	IO	PT4C	TCK	L82T
E10	0 (TL)	-	VDDIO0	VDDIO0	-	-
B22	-	-	VSS	VSS	-	-
C4	0 (TL)	6	IO	PT2D	PLL_CK1C/PPLL	L83C

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AM12	6 (BL)	9	IO	PB12B	—	L28C_A0
AP12	6 (BL)	9	IO	PB12C	VREF_6_09	L29T_A0
AP13	6 (BL)	9	IO	PB12D	D25	L29C_A0
AM13	6 (BL)	9	IO	PB13A	—	L30T_D0
AN14	6 (BL)	9	IO	PB13B	—	L30C_D0
V17	—	—	VSS	VSS	—	—
AP14	6 (BL)	10	IO	PB13C	D26	L31T_A0
AP15	6 (BL)	10	IO	PB13D	D27	L31C_A0
AK13	6 (BL)	10	IO	PB14A	—	L32T_A0
AK14	6 (BL)	10	IO	PB14B	—	L32C_A0
AM14	6 (BL)	10	IO	PB14C	VREF_6_10	L33T_A0
AL14	6 (BL)	10	IO	PB14D	D28	L33C_A0
AP17	6 (BL)	11	IO	PB15A	—	L34T_A0
AP16	6 (BL)	11	IO	PB15B	—	L34C_A0
AM15	6 (BL)	11	IO	PB15C	D29	L35T_D0
AN16	6 (BL)	11	IO	PB15D	D30	L35C_D0
AM17	6 (BL)	11	IO	PB16A	—	L36T_A0
AM16	6 (BL)	11	IO	PB16B	—	L36C_A0
AP18	6 (BL)	11	IO	PB16C	VREF_6_11	L37T_A0
AP19	6 (BL)	11	IO	PB16D	D31	L37C_A0
AL16	5 (BC)	1	IO	PB17A	—	L1T_D0
AK15	5 (BC)	1	IO	PB17B	—	L1C_D0
N22	—	—	VSS	VSS	—	—
AN18	5 (BC)	1	IO	PB17C	—	L2T_A0
AN19	5 (BC)	1	IO	PB17D	—	L2C_A0
AP20	5 (BC)	1	IO	PB18A	—	L3T_A0
AP21	5 (BC)	1	IO	PB18B	—	L3C_A0
AL17	5 (BC)	1	IO	PB18C	VREF_5_01	L4T_D0
AK16	5 (BC)	1	IO	PB18D	—	L4C_D0
P13	—	—	VSS	VSS	—	—
AM19	5 (BC)	2	IO	PB19A	—	L5T_A0
AM18	5 (BC)	2	IO	PB19B	—	L5C_A0
P14	—	—	VSS	VSS	—	—
AN20	5 (BC)	2	IO	PB19C	PBCK0T	L6T_A0
AM20	5 (BC)	2	IO	PB19D	PBCK0C	L6C_A0
AK17	5 (BC)	2	IO	PB20A	—	L7T_D0
AL18	5 (BC)	2	IO	PB20B	—	L7C_D0
AL11	5 (BC)	—	VDDIO5	VDDIO5	—	—
AP22	5 (BC)	2	IO	PB20C	VREF_5_02	L8T_D0
AN21	5 (BC)	2	IO	PB20D	—	L8C_D0
AM22	5 (BC)	2	IO	PB21A	—	L9T_A0
AM21	5 (BC)	2	IO	PB21B	—	L9C_A0
AP23	5 (BC)	3	IO	PB21C	—	L10T_D0
AN22	5 (BC)	3	IO	PB21D	VREF_5_03	L10C_D0

Table 46. Heat Sink Vendors

Vendor	Location	Phone
Aavid Thermalloy	Concord, NH	(603) 224-9988
Chip Coolers	Warwick, RI	(800) 227-0254
IERC	Burbank, CA	(818) 842-7277
R-Theta	Buffalo, NY	(800) 388-5428
Sanyo Denki	Torrance, CA	(310) 783-5400
Wakefield Thermal Solutions	Pelham, NH	(800) 325-1426

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 47 lists eight parasitics associated with the ORCA packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

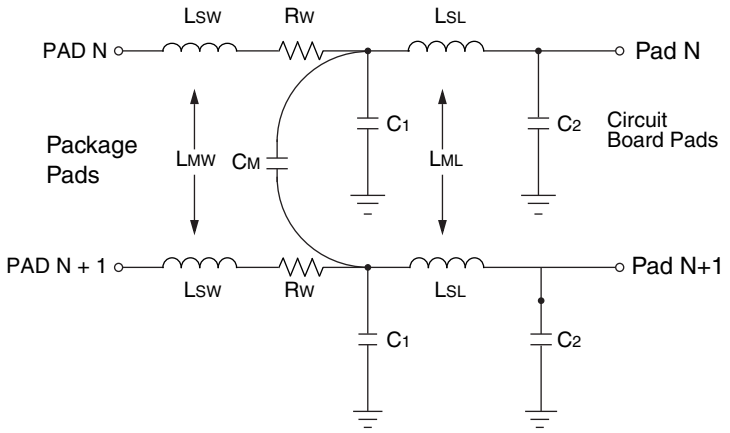
Four inductances in nH are listed: L_{SW} and L_{SL}, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead. Resistance values are in mΩ.

The parasitic values in Table 47 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C_1 and C_2 capacitors.

Table 47. ORCA Typical Package Parasitics

L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
3.8	1.3	250	1.0	1.0	0.3	2.8-5	0.5 -1

Figure 41. Package Parasitics



Package Outline Drawings

Package Outline Drawings for the 484-ball PBGAM (fpBGA) used for the ORT42G5 and 680-ball PBGAM (fpBGA) used for the ORT82G5 are available in the Package Diagrams section of the Lattice Semiconductor web site at www.latticesemi.com.