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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	372
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort82g5-1fn680i

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System Bus

An on-chip, multimaster, 8-bit system bus with 1-bit parity facilitates communication among the MPI, configuration logic, FPGA control, status registers, Embedded Block RAMs, as well as user logic. Utilizing the AMBA specification Rev 2.0 AHB protocol, the Embedded System Bus offers arbiter, decoder, master, and slave elements. Master and slave elements are also available for the user-logic and a slave interface is used for control and status of the embedded backplane transceiver portion of the device.

The system bus control registers can provide control to the FPGA such as signaling for reprogramming, reset functions, and PLL programming. Status registers monitor INIT, DONE, and system bus errors. An interrupt controller is integrated to provide up to eight possible interrupt resources. Bus clock generation can be sourced from the microprocessor interface clock, configuration clock (for slave configuration modes), internal oscillator, user clock from routing, or from the port clock (for JTAG configuration modes).

Phase-Locked Loops

Up to eight PLLs are provided on each Series 4 device, with four user PLLs generally provided for FPSCs. Programmable PLLs can be used to manipulate the frequency, phase, and duty cycle of a clock signal. Each PPLL is capable of manipulating and conditioning clocks from 20 MHz to 200 MHz. Frequencies can be adjusted from 1/8x to 8x, the input clock frequency. Each programmable PLL provides two outputs that have different multiplication factors but can have the same phase relationships. Duty cycles and phase delays can be adjusted in 12.5% of the clock period increments. An automatic input buffer delay compensation mode is available for phase delay. Each PPLL provides two outputs that can have programmable (12.5% steps) phase differences.

Embedded Block RAM

New 512 x 18 block-port RAM blocks are embedded in the FPGA core to significantly increase the amount of memory and complement the distributed PFU memories. The EBRs include two write ports, two read ports, and two byte lane enables which provide four-port operation. Optional arbitration between the two write ports is available, as well as direct connection to the high-speed system bus.

Additional logic has been incorporated to allow significant flexibility for FIFO, constant multiply, and two-variable multiply functions. The user can configure FIFO blocks with flexible depths of 512K, 256K, and 1K including asynchronous and synchronous modes and programmable status and error flags. Multiplier capabilities allow a multiple of an 8-bit number with a 16-bit fixed coefficient or vice versa (24-bit output), or a multiple of two 8-bit numbers (16-bit output). On-the-fly coefficient modifications are available through the second read/write port.

Two 16 x 8-bit CAMs per embedded block can be implemented in single match, multiple match, and clear modes. The EBRs can also be preloaded at device configuration time.

Configuration

The FPGAs functionality is determined by internal configuration RAM. The FPGAs internal initialization/configuration circuitry loads the configuration data at power up or under system control. The configuration data can reside externally in an EEPROM or any other storage media. Serial EEPROMs provide a simple, low pin-count method for configuring FPGAs.

The RAM is loaded by using one of several configuration modes. Supporting the traditional master/slave serial, master/slave parallel, and asynchronous peripheral modes, the Series 4 also utilizes its microprocessor interface and Embedded System Bus to perform both programming and readback. Daisy chaining of multiple devices and partial reconfiguration are also permitted.

Other configuration options include the initialization of the embedded-block RAM memories and FPSC memory as well as system bus options and bit stream error checking. Programming and readback through the JTAG (IEEE 1149.2) port is also available meeting In-System Programming (ISP™) standards (IEEE 1532 Draft).

Dual Port RAMs

In addition to the backplane interface blocks, there are two independent memory blocks in the ASB. Each memory block has a capacity of 4k words by 36 bits. It has one read port, one write port, and four byte-write-enable (active-low) signals. The read data from the memory block is registered so that it works as a pipelined synchronous memory block.

FPSC Configuration

Configuration of the ORT42G5 and ORT82G5 occurs in two stages: FPGA bitstream configuration and embedded core setup.

Prior to becoming operational, the FPGA goes through a sequence of states, including power up, initialization, configuration, start-up, and operation. The FPGA logic is configured by standard FPGA bit stream configuration means as discussed in the Series 4 FPGA data sheet.

After the FPGA configuration is complete, the options for the embedded core are set based on the contents of registers that are accessed through the FPGA system bus.

The system bus itself can be driven by an external PowerPC compliant microprocessor via the MPI block or via a user master interface in FPGA logic. A simple IP block that drives the system by using the user register interface and very little FPGA logic is available in the MPI/System Bus Technical Note. This IP block sets up the embedded core via a state machine and allows the ORT42G5 and ORT82G5 to work in an independent system without an external microprocessor interface.

Backplane Transceiver Core Detailed Description

The following sections describe the various logic blocks in the Embedded Core portion of the FPSC. The FPGA section of the FPSC is identical to an ORCA OR4E04 FPGA except that the pads on one edge of the FPGA chip are replaced by the Embedded Core. For a detailed description of the programmable logic functions, please see the ORCA Series 4 FPGA Data Sheet and related application and technical notes.

The major functional blocks in the Embedded Core include:

- Two SERializer-DESerializer (SERDES) blocks and Clock and Data Recovery (CDR) circuitry
- 8b/10b encoder/decoders
- Transmit pre-emphasis circuitry
- 4-to-1 multiplexers (MUX) and 1-to-4 demultiplexers (DEMUX)
- Fibre channel synchronization state machine
- XAUI link alignment state machine
- Alignment FIFOs
- Embedded 4K x 36 RAM blocks (independent from transceiver logic).

A top level block diagram of the Embedded Core Logic is shown in Figure 2. The Embedded RAM blocks are not shown. The external pins for the Embedded Core are listed later in this data sheet in Table 41 and the signals at the Transceiver Embedded Core/FPGA interface for the ORT42G5 are listed in Table 8, Table 9 and Table 11; and for the ORT82G5, in Table 8, Table 10 and Table 12.

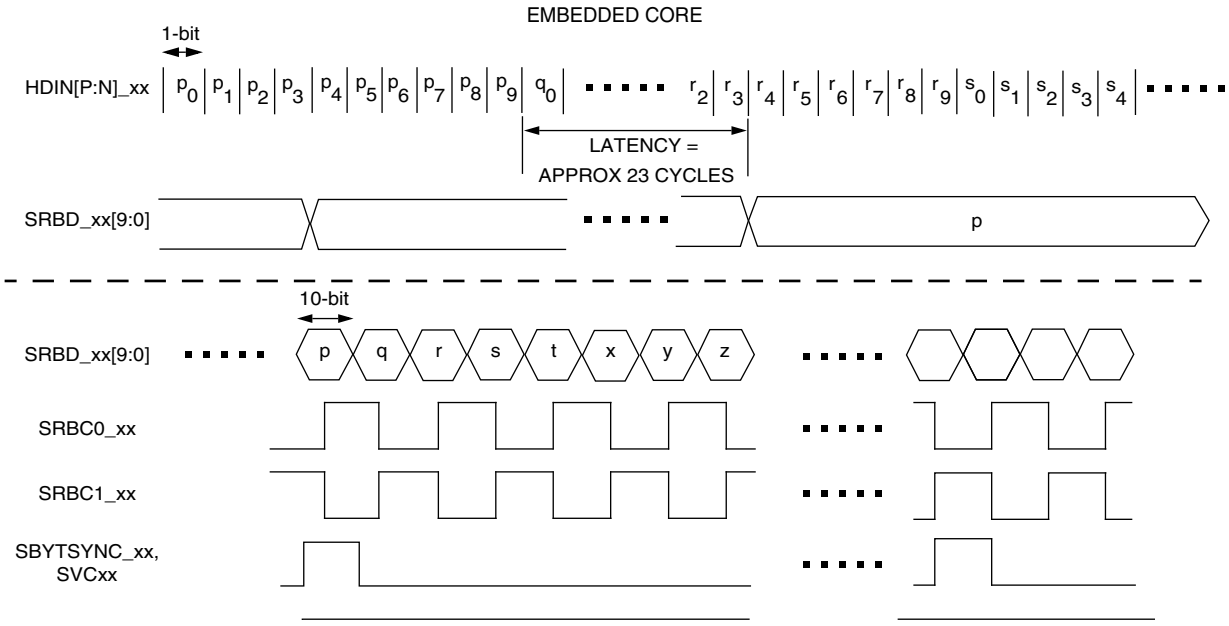
Receive CML Input Buffer and SERDES

The receiver section receives high-speed serial data at its differential CML input port. The receive input is an AC-coupled input. The received data is sent to the clock recovery section which generates a recovered clock and retimes the data. Valid data will be received after the receive PLL has locked to the input data frequency and phase.

The received serial data is converted to10-bit wide parallel data by the 1:10 demultiplexor. Clock recovery is performed by the SERDES block for each of the eight receive channels. This recovered data is then aligned to a 10-bit word boundary by detecting and aligning to a comma special character. Word alignment is done for either polarity of the comma character. The 10-bit code word is passed to the 8b/10b decoder, which provides an 8-bit byte of data, a special character indicator bit and a SBYTSYNC_xx signal (where again xx is a placeholder for AA,...,BD or AC, AD, BC, BD).

Data from a SERDES channel is sent to the DEMUX block in 10-bit raw form or 8-bit decoded form across the SRBD_xx [9:0] port with a latency of approximately 14-23 cycles (bit periods of the incoming data). Accompanying this data are the comma-character indicator (SBYTSYNC_xx), link-state indicator (SWDSYNC_xx), clocks (SRBC0_xx, and SRBC1_xx), and code-violation indicator (SCVxx). The two internal clocks operated at twice the reference clock frequency. Figure 7 shows the receive path timing for a single SERDES channel.

Figure 7. Receive Path Timing for a Single SERDES Channel



With the 8b10bR_xx control bit of the SERDES channel set to 1, the data presented at SRBD_xx[9:0] will be decoded characters. Bit 8 will indicate whether SRBDxx[7:0] represents an ordinary data character (bit 8 = 0), or whether SRBD_xx[7:0] represents a special character, like a comma. Bit 9 may be either a code violation indicator or one of seven out of synchronization state indicators, as described later.

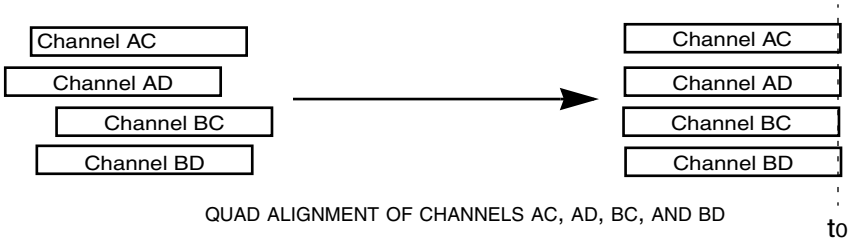
When 8b10bR is set to 0, the data at SRBD_xx[9:0] will not be decoded. The XAUI link-state machine should not be used in this mode of operation. When in XAUI mode, the MUX/DEMUX looks for /A/ (as defined in *IEEE* 802.3ae v.2.1) characters for channel alignment and requires the characters to be in decoded form for this to work

1:4 Demultiplexer (DEMUX)

The1:4 DEMUX has to accumulate four sets of characters presented to it at the SERDES receive interface and put these out at one time at the low-speed receive interface.

Another task of the 1:4 DEMUX is to recognize the synchronizing event and adjust the 4-byte boundary so that the synchronizing character leads off a new 4-byte word. In Fibre Channel mode, this synchronizing character is a comma. This feature will be referred to as DEMUX word alignment in other areas of this document. DEMUX word

Figure 12. Four Channel Alignment of SERDES Blocks A and B



ORT82G5 Multi-channel Alignment

The ORT82G5 has a total of eight channels (four per SERDES block). The incoming data of these channels can be synchronized in several ways or they can be independent of one other. Two channels within a SERDES block can be aligned together. Channel A and B and/or channel C and D can form a pair as shown in Figure 13. Alternately, all four channels of a SERDES block can be aligned together to form a communication channel with a bandwidth of 10 Gbps as shown in Figure 14. Finally, the alignment can be extended across both SERDES block to align all eight channels in ORT82G5 as shown in Figure 15. Individual channels within an alignment group can be disabled (i.e., powered down) without disrupting other channels.

Figure 13. Dual Channel Alignment

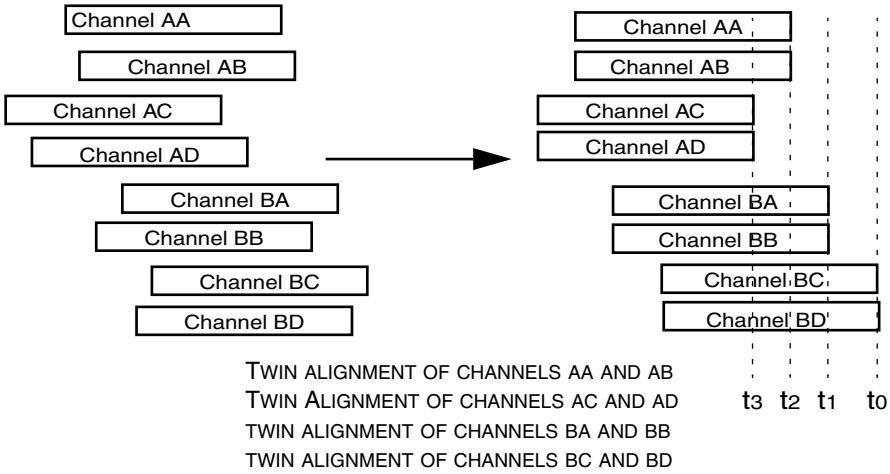
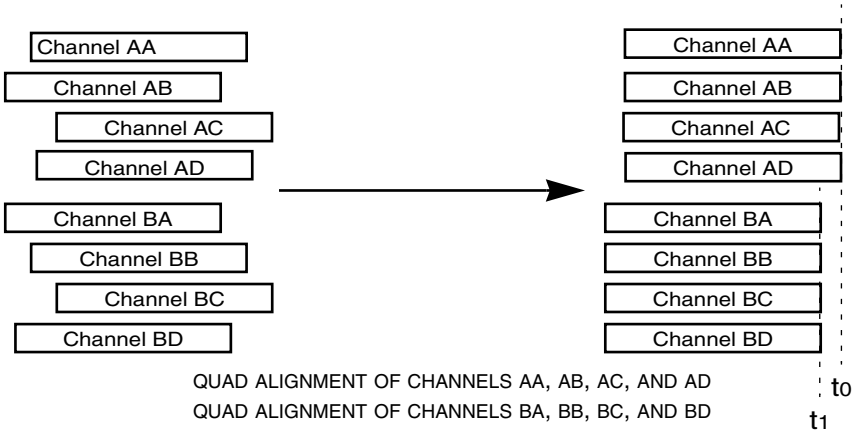


Figure 14. Alignment of SERDES Quads A and B



- FMPU_RESYNC2A2 for twin channel A[C:D]
- FMPU_RESYNC4B for quad channel B[A:D]
- FMPU_RESYNC2B1 for twin channel B[A:B]
- FMPU_RESYNC2B2 for twin channel B[C:D]

To resynchronize an independent channel (resetting the write and the read pointer of the FIFO) set the following bit to zero, and then set it to one:

- FMPU_RESYNC1_xx

ORT42G5 Alignment Sequence

1. Follow steps 1, 2 and 3 in the start up sequence described in a later section.

2. Initiate a SERDES software reset by setting the SWRST bit to 1 and then to 0. Note that, any changes to the SERDES configuration bits should be followed by a software reset.

3. Wait for 3 ms. REFCLK should be toggling by this time. During this time, configure the following registers.

Set the following bits in registers 30820, 30920:

- XAUI_MODE_xx-set to 1 for XAUI mode or keep the default value of 0 if the Fibre Channel state machine was selected.
- Enable channel alignment by setting FMPU_SYNMODE bits in registers 30811, 30911.
- FMPU_SYNMODE_xx. Set to appropriate values for 2 or 4 channel alignment based on Table 6.
- Set RCLKSEL[A:B] and TCKSEL[A:B] bits in register 30A00.
- RCKSEL[A:B]-choose clock source for 78 MHz RCK78x (Table 18).
- TCKSEL[A:B]-Choose clock source for 78 MHz TCK78x (Table 17).

Send data on serial links. Monitor the following status/alarm bits:

- Monitor the following alarm bits in registers 30020, 30030, 30120, 30130.
- LKI-PLL_xx lock indicator. A 1 indicates that PLL has achieved lock.
- Monitor the following status bits in registers 30804, 30904
- XAUISTAT_xx - In XAUI mode, they should be 10.

Monitor the following status bits in registers 30805, 30905

- DEMUXWAS_xx - They should be 1 indicating word alignment is achieved.
- CH24_SYNCxx - They should be 1 indicating channel alignment. This is cleared by resync.

4. Write a 1 to the appropriate resync registers 30820, 30920 or 30A02. Note that this assumes that the previous value of the resync bits are 0. The resync operation requires a rising edge. Two writes are required to the resync bits: write a 0 and then write a 1. It is highly recommended to precede a resync with a word alignment, especially in situations where a disturbance in the receive SERDES path can cause misalignment of data and OOS indications without bringing the FC/XAUI state machine to a loss of synch state. A word alignment is achieved by writing a 0 and then a 1 to the appropriate DOWDALIGNxx bits in registers 30810/30910.

Check out-of-sync and FIFO overflow status in registers 30814 (Bank A).

- SYNC2_A_OOS, SYNC2_A_OVFL - by 2 alignment.

Check out-of-sync status in registers 30914 (Bank B).

- SYNC2_B_OOS, SYNC2_B_OVFL - by 2 alignment.

Check out-of-sync status in registers 30A03.

- SYNC4_OOS, SYNC4_OVFL - by 4 alignment.
- If out-of-sync bit is 1, then rewrite a 1 to the appropriate resync registers and monitor the OOS bit again.
- If Out of Synchronization (OOS) bit is 0 but OVFL bit is 1, then check if the RX_FIFO_MIN value has been pro-

Table 8. Definition of Bits of MRWDxx[39:0] (Continued)

Bit Index	8b10bR=0	8b10bR=1	
	NOCHALGN[A:B]=1 CV_SELxx=0	NOCHALGN[A:B]=1 CV_SELxx=1	NOCHALGN[A:B]=0 CV_SELxx=1
12	bit 2 of 10-bit data 1	bit 2 of byte 1	bit 2 of byte 1
11	bit 1 of 10-bit data 1	bit 1 of byte 1	bit 1 of byte 1
10	bit 0 of 10-bit data 1	bit 0 of byte 1	bit 0 of byte 1
09	bit 9 of 10-bit data 0	CV_xx0, code violation, byte 0	VL (connected to ground)
08	bit 8 of 10-bit data 0	K_CTRL for byte 0	K_CTRL for byte 0
07	bit 7 of 10-bit data 0	bit 7 of byte 0	bit 7 of byte 0
06	bit 6 of 10-bit data 0	bit 6 of byte 0	bit 6 of byte 0
05	bit 5 of 10-bit data 0	bit 5 of byte 0	bit 5 of byte 0
04	bit 4 of 10-bit data 0	bit 4 of byte 0	bit 4 of byte 0
03	bit 3 of 10-bit data 0	bit 3 of byte 0	bit 3 of byte 0
02	bit 2 of 10-bit data 0	bit 2 of byte 0	bit 2 of byte 0
01	bit 1 of 10-bit data 0	bit 1 of byte 0	bit 1 of byte 0
00	bit 0 of 10-bit data 0	bit 0 of byte 0	bit 0 of byte 0

Table 9. Definition of Status Bits of MRWDxx that Vary for Different Channels for the ORT42G5

Channel Index	Bit Index	Name	Description
all	39	CH24_SYNCxx	Multi-channel alignment attempt complete if 1
AC	29	CV_AC_OR	Code violation in one or more of the received 10-bit groups for channel AC
AC	19	SYNC2_A_OOS	Dual channel synchronization of channels AC and AD not successful if 1
AD	29	CV_AD_OR	Code violation in one or more of the received 10-bit groups for channel AD
AD	19	SYNC4_OOS	Four channel synchronization not successful if 1
BC	29	CV_BC_OR	Code violation in one or more of the received 10-bit groups for channel BC
BC	19	SYNC2_B_OOS	Dual channel synchronization of channels BC and BD not successful if 1
BD	29	CV_BD_OR	Code violation in one or more of the received 10-bit groups for channel BD
BD	19	SYNC4_OOS	Eight channel synchronization not successful if 1

In the ORT42G5, SYNC2_[A, B]_OOS and SYNC4_OOS signals can be used with CH24_SYNC_xx to determine if the desired multi-channel alignment was successful. If, when CH24_SYNC_xx goes high with the corresponding OOS signal remaining low, the data being transferred across the core/FPGA interface is correctly aligned between channels. Note that only the signals corresponding to the selected alignment mode will be meaningful.

Table 10. Definition of Status Bits of MRWDxx that Vary for Different Channels for the ORT82G5

Channel Index	Bit Index	Name	Description
all	39	CH248_SYNCxx	Multi-channel alignment attempt complete if 1
AA	29	CV_AA_OR	Code violation in one or more of the received 10-bit groups for channel AA
AA	19	SYNC2_A1_OOS	Dual channel synchronization of channels AA and AB not successful if 1
AB	29	CV_AB_OR	Code violation in one or more of the received 10-bit groups for channel AB
AB	19	SYNC4_A_OOS	Quad channel synchronization of SERDES quad A not successful if 1
AC	29	CV_AC_OR	Code violation in one or more of the received 10-bit groups for channel AC
AC	19	SYNC2_A2_OOS	Dual channel synchronization of channels AC and AD not successful if 1
AD	29	CV_AD_OR	Code violation in one or more of the received 10-bit groups for channel AD
AD	19	SYNC8_OOS	Eight channel synchronization not successful if 1

Table 12. Transceiver Embedded Core/FPGA Interface Signal Description for the ORT82G5

FPGA/Embedded Core Interface Signal Name xx=... line remain (xx = [AA, ..., BD]	Input (I) to or Output (O) from Core	Signal Description
Transmit Path Signals		
TWDxx[31:0]	I	Transmit data – channel xx.
TCOMMAxx[3:0]	I	Transmit comma character – channel xx.
TBIT9xx[3:0]	I	Transmit force negative disparity – channel xx
TSYS_CLK_xx	I	Transmit low-speed clock to the FPGA – channel xx
TCK78[A:B]	O	Transmit low-speed clock to the FPGA – SERDES Quad [A:B].
Receive Path Signals		
MRWDxx[39:0]	O	Receive data – Channel xx (see Table 8 and Table).
RWCKxx	O	Low-speed receive clock—Channel xx.
RCK78[A:B]	O	Receive low-speed clock to FPGA—SERDES Quad [A:B].
RSYS_CLK_A1	I	Low-speed receive FIFO clock for channels AA, AB
RSYS_CLK_A2	I	Low-speed receive FIFO clock for channels AC, AD
RSYS_CLK_B1	I	Low-speed receive FIFO clock for channels BA, BB
RSYS_CLK_B2	I	Low-speed receive FIFO clock for channels BC, BD
CV_SELxx	I	Enable detection of code violations in the incoming data
SYS_RST_N	I	Synchronous reset of the channel alignment blocks.

Reference Clocks and Internal Clock Distribution

Reference Clock Requirements

There are two pairs of reference clock inputs on the ORT42G5 and ORT82G5. The differential reference clock is distributed to all channels in a block. Each channel has a differential buffer to isolate the clock from the other channels. The input clock is preferably a differential signal; however, the device can operate with a single-ended input. The input reference clock directly impacts the transmit data eye, so the clock should have low jitter. In particular, jitter components in the DC to 5 MHz range should be minimized. The required electrical characteristics for the reference clock are given in Table 38.

Note: In sections of this data sheet, the differential clocks are simply referred to as the reference clock as REFCLK_[A:B].

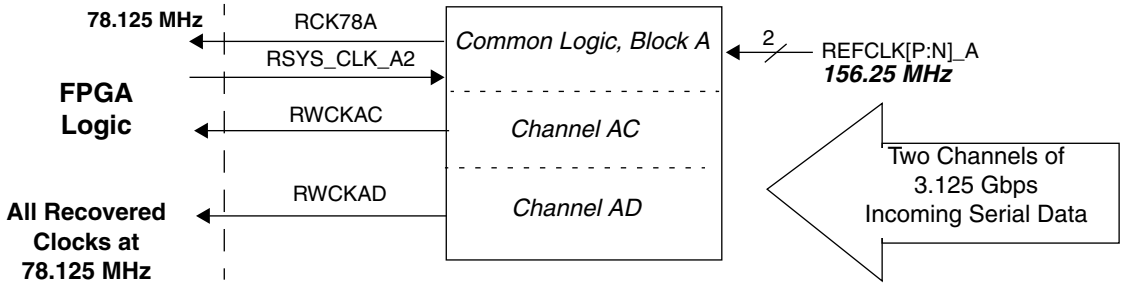
Synthesized and Recovered Clocks

The SERDES Embedded Core block contains its own dedicated PLLs for transmit and receive clock generation. The user provides a reference clock of the appropriate frequency, as described in the previous section. The transmitter PLL uses the REFCLK_[A,B] inputs to synthesize the internal high-speed serial bit clocks. The receiver PLLs extract the clock from the serial input data and retime the data with the recovered clock.

The receive PLL for each channel has two modes of operation - lock to reference and lock to data with retiming. When no data or invalid data is present on the HDINP_xx and HDINN_xx pins, the receive VCO will not lock to data and its frequency can drift outside of the nominal ±350 ppm range. Under this condition, the receive PLL will lock to REFCLK_[A,B] for a fixed time interval and then will attempt to lock to receive data. The process of attempting to lock to data, then locking to clock will repeat until valid input data exists. There is also a control register bit per channel to force the receive PLL to always lock to the reference clock.

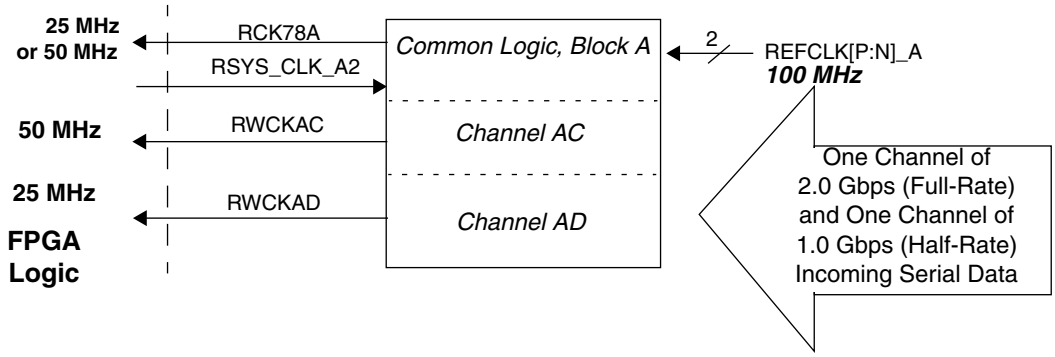
The high-speed transmit and receive serial data links can run at 0.6 to 3.7 Gbps, depending on the frequency of the reference clock and the state of the control bits from the internal transmit control register. The interface to the serializer/deserializer block runs at 1/10th the bit rate of the data lane. Additionally, the MUX/DEMUX logic converts the

Figure 20. Receive Clocking for a Single Block (Similar Connections Would Be Used for Block B)



The receive channel alignment bypass mode allows mixing of half and full line rates among the channels, as shown in Figure 21. The figure shows channel AC configured in full rate mode at 2.0 Gbps. Channel AD configured in half-rate mode at 1.0 Gbps. The receive alignment FIFO per channel cannot be used in this mode.

Figure 21. Receive Clocking for Mixed Line Rates



Each SERDES block can also be configured for any line rate (0.6 to 3.7 Gbps), since each block has its own reference clock input pins.

Multi-Channel Alignment Clocking Strategies for the ORT42G5

The data on the four channels in the ORT42G5 can be independent of each other or can be synchronized in two different ways. For example, two channels within a SERDES block can be aligned together, channel C and channel D. Alternatively, all four channels in a SERDES block can be aligned together to form a communication channel with a bandwidth of 10 Gbps. Individual channels within an alignment group can be disabled (i.e., powered down) without disrupting other channels. Clocking strategies for these various modes are described in the following paragraphs.

For dual alignment both channels must be sourced by the same clock. Either RWCKAC or RWCKAD can be connected to RSYS_CLK_A2. A clocking example for dual alignment is shown in Figure 22.

Test Modes

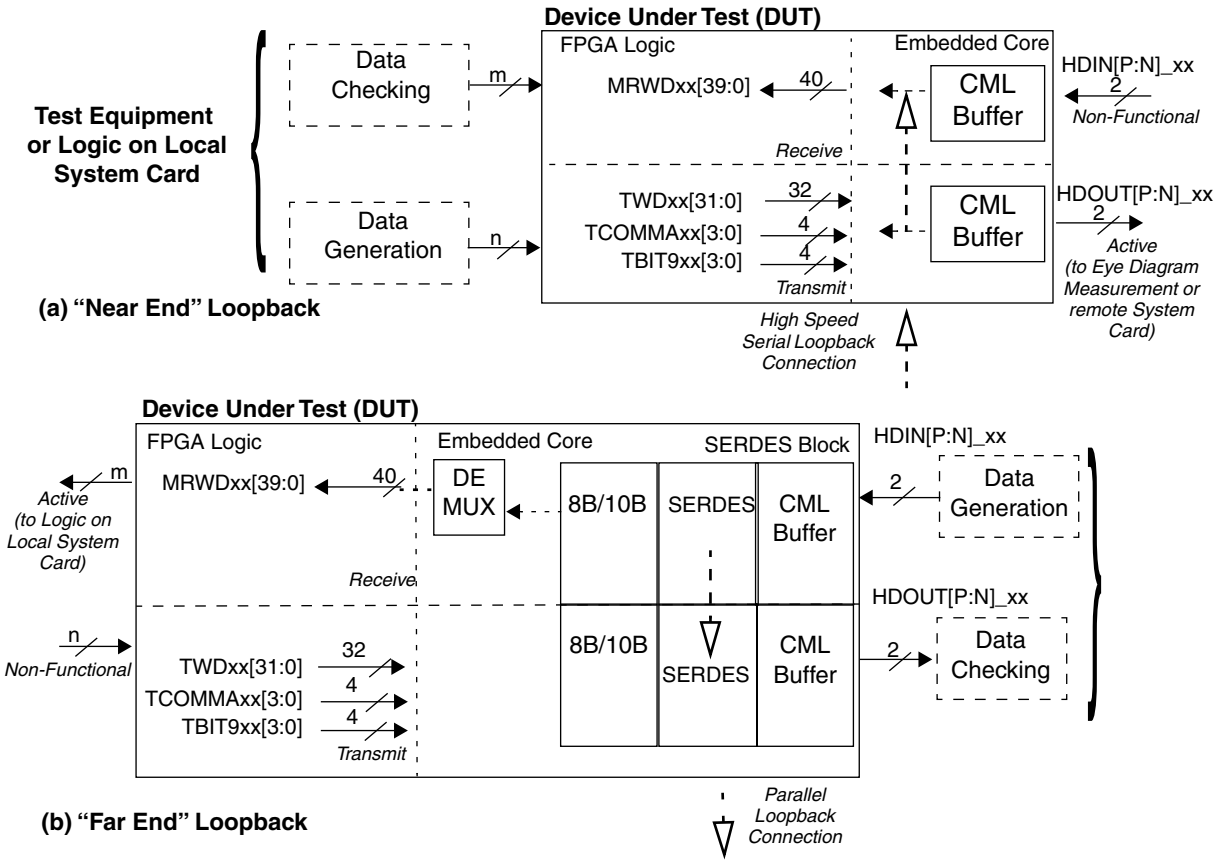
In addition to the operational logic described in the preceding sections, the Embedded Core contains logic to support various test modes - both for device validation and evaluation and for operating system level tests. The following sections discuss two of the test support logic blocks, supporting various loopback modes and SERDES characterization.

Loopback Testing

Loopback testing is performed by looping back (either internal to the Embedded Core, by configuring the FPGA logic or by external connections) transmitted data to the corresponding receiver inputs, or received data to the transmitter output. The loopback path may be either serial or parallel.

In general, loopback tests can be classified as “near end” or “far end.” In “near end” loopback (Figure 32(a)), data is generated and checked locally, i.e. by logic on, or connection of, test equipment to the same card as the FPSC. In “far end” loopback (Figure 32(b)), the generating and checking functions are performed remotely, either by test equipment or a remote system card.

Figure 32. “Near End” vs. “Far End” Loopback



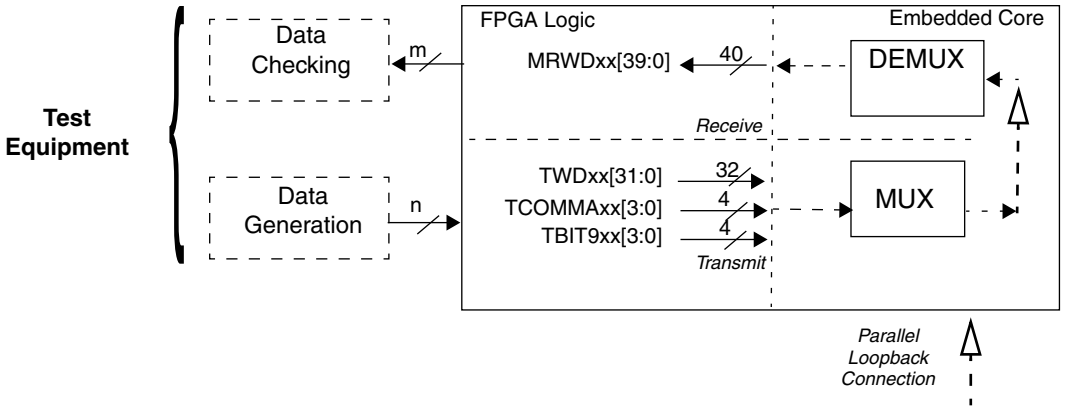
The loopback mode can also be characterized by the physical location of the loopback connection. There are three possible loopback modes supported by the Embedded Core logic:

- High-speed serial loopback at the CML buffer interface (near end)
- Parallel loopback at the SERDES boundary (far end)

Parallel Loopback at MUX/DEMUX Boundary, Excluding SERDES

This is a low-frequency test mode used to test the MUX/DEMUX logic block. As with the mode described in the previous section, the loopback path is at the interface between the SERDES blocks and the MUX and DEMUX blocks and uses the parallel 10-bit buses at these interfaces (see Figure 33). However, the loopback connection is made such that the output signals from the TX MUX block are used as the input signals to the RX SERDES block. In this loopback mode the MRWDxx[39:0], TWDxx[31:0], TCOMMAxx[3:0] and TBIT9xx[3:0] signal lines function normally and the high-speed serial input and output buffers are not used. Use of this mode also requires configuration of the FPGA logic to connect the MRWDxx[39:0], TWDxx[31:0], TCOMMAxx[3:0] and TBIT9xx[3:0] signal lines to external pins. The basic loopback path is shown in Figure 33.

Figure 33. Parallel Loopback at MUX/DEMUX Boundary, Excluding SERDES



This test mode is enabled by setting the pin PLOOP_TEST_ENN to 0. PASB_TESTCLK must be running in this mode at 4x frequency of RSYS_CLK[A2, B2] or TSYS_CLK_[AC, AD, BC, BD] for the ORT42G5 and RSYS_CLK[A1,A2,B1,B2] or TSYS_CLK_[AA, AB... BD] for the ORT82G5.

SERDES Characterization Test Mode (ORT82G5 Only)

The SERDES characterization mode is a test mode that allows for direct control and observation of the transmit and receive SERDES interfaces at chip ports. With these modes the SERDES logic and I/O can be tested one channel at a time in either the receive or transmit modes. The SERDES characterization mode is available for only one quad (quad B) of the ORT82G5.

The characterization test mode is configured by setting bits in the control registers via the system bus. There are four bits that set up the test mode. The transmit characterization test mode is entered when SCHAR_ENA=1 and SCHAR_TXSEL=1. Entering this mode will cause chip port inputs to directly control the SERDES low-speed transmit ports of one of the channels as shown in Table 23.

Table 23. SERDES Transmit Characterization Mode

Chip Port	SERDES Input
PSCHAR_CKIO0	TBCBx
PSCHAR_LDIO[9:0]	LDINBx[9:0]

The x in the table will be a single channel in SERDES quad B, selected by the SCHAR_CHAN control bits. The decoding of SCHAR_CHAN is shown in Table 24.

As mentioned earlier, both sections of a slice can be written independently / simultaneously, due to the independent CSW per section.

The same signal illustration above applies to slice B by changing _A to _B.

SDRAM A and SDRAM B in Figure 34 refer to the built-in sections A and B of one EAC RAM slice.

These SDRAMS should not be confused with the FPGA SDRAMS, which are generated through Module Generator in ispLEVER. The EAC SDRAMs are always built-in to the embedded core section of the ORT82G5/42G5 and their pins are accessed through the EAC interface. In order for these pins to be available at the interface in the generated HDL models from ispLEVER, the “Use the Extra Memory in FPSC Core” checkbox needs to be checked in the customization window (after hitting the "customize" button) in Module Generator, while generating the ORT82G5/42G5 core HDL. These signals will not otherwise show in the interface model.

Figure 35 and Figure 36 show, per slice, timing diagrams for both write and read accesses. These figures do not include the _x section, which refers to either slice A or B, even though this is implied. Signal names and functions are summarized in Table 26 and follow the general ORCA Series 4 naming conventions.

Figure 34. Block Diagram, Embedded Core Memory Slice

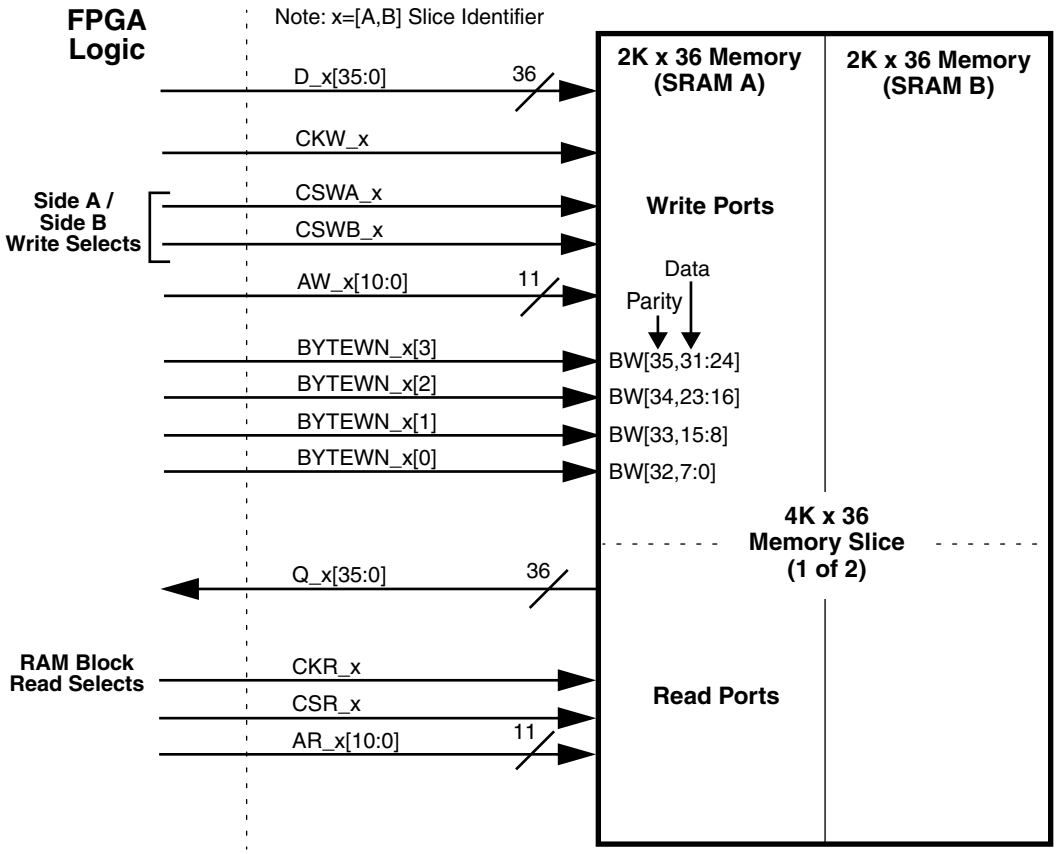


Table 30. ORT82G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Global Control Registers (Read Write) Act on all Four Channels in SERDES Quad A or SERDES Quad B.				
30005 - A 30105 - B	[0]	Reserved	See bit descrip.	Reserved, must be set to 0. Set to 0 on device reset.
	[1]	GMASK_[A:B]		Global Mask. When GMASK_[A:B] = 1, the transmit and receive alarms of all channels in the SERDES quad are prevented from generating an interrupt (i.e., they are masked or disabled). The GMASK_[A:B] bit overrides the individual MASK_xx bits. GMASK_[A:B] = 1 on device reset.
	[2]	GSWRST_[A:B]		Software reset bit. The GSWRST_[A:B] bit provides the same function as the hardware reset for the transmit and receive sections of all four channels, except that the device configuration settings are not affected when GSWRST_[A:B] is asserted. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. The GSWRST_[A:B] bit overrides the individual SWRST_xx bits. GSWRST_[A:B] = 0 on device reset.
	[3]	GPWRDNT_[A:B]		Powerdown Transmit Function. When GPWRDNT_[A:B] = 1, sections of the transmit hardware for all four channels of are powered down to conserve power. The GPWRDNT_[A:B] bit overrides the individual PWRDNT_xx bits. GPWRDNT_[A:B] = 0 on device reset.
	[4]	GPWRDNR_[A:B]		Powerdown Receive Function. When GPWRDNR_[A:B] = 1, sections of the receive hardware for all four channels are powered down to conserve power. The GPWRDNR_[A:B] bit overrides the individual PWRDNR_xx bits. GPWRDNR_[A:B] = 0 on device reset.
	[5]	Reserved		Reserved, 1 on device reset.
	[6]	Not used		Not used. 0 on reset.
	[7]	GTESTEN_[A:B]		Test Enable Control. When GTESTEN_[A:B] = 1, the transmit and receive sections of all four channels are placed in test mode. The GTESTEN_[A:B] bit overrides the individual TESTEN_xx bits. GTESTEN_[A:B] = 0 on device reset.
30006 - A 30106 - B	[0:4]	TestMode[A:B]	00	TestMode - See Test Mode section for settings
	[5]	Not used		Not used
	[6:7]	Reserved		Reserved
Control Registers (Read/Write), xx=[AA,...,BD]				
30800 - Ax 30900 - Bx	[0]xA [1]xB [2]xC [3]xD	ENBYSYNC_xx	00	ENBYSYNC_xx = 1 Enables Receiver Byte Synchronization for Channel xx. ENBYSYNC_xx = 0 on device reset.
	[4]xA [5]xB [6]xC [7]xD	LCKREFN_xx		LCKREFN_xx = 0 Locks the receiver PLL to ref reference clock for Channel xx. LCKREFN_xx =1 = Locks the receiver to data for Channel xx. NOTE: When LCKREFN_xx = 0, the corresponding LKI_xx bit is also 0. LCKREFN_xx = 0 on device reset.
30801 - Ax 30901 - Bx	[0]xA [1]xB [2]xC [3]xD	LOOPENB_xx		Enable Loopback Mode for Channel xx. When LOOPEN_xx=1, the transmitter high-speed output is looped back to the receiver high-speed input. This mode is similar to high-speed loopback mode enabled by TESTMODE_xx except that LOOPEN_xx disables the high-speed serial output. LOOPEN_xx=0 on device reset.
	[4]xA [5]xB [6]xC [7]xD	NOWDALIGN_xx		Word Align Disable Bit. When NOWDALIGN_xx=1, receiver word alignment is disabled for Channel xx. NOWDALIGN_xx=0 on device reset.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

The ORCA Series 4 FPSCs include circuitry designed to protect the chips from damaging substrate injection currents and to prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_{STG}	– 65	150	°C
Power Supply Voltage with Respect to Ground	V_{DD33}	– 0.3	4.2	V
	V_{DDIO}	– 0.3	4.2	V
	V_{DD15}, V_{DD_ANA}, V_{DDGB}	—	2.0	V
Input Signal with Respect to Ground	V_{IN}	V_{SS} – 0.3	V_{DD}IO + 0.3	V
Signal Applied to High-impedance Output	—	V_{SS} – 0.3	V_{DD}IO + 0.3	V
Maximum Package Body (Soldering) Temperature	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage with Respect to Ground[1]	V_{DD33}	3.0	3.6	V
	V_{DD15}	1.425	1.575	V
Input Voltages	V_{IN}	V_{SS} – 0.3	V_{DDIO} + 0.3	V
Junction Temperature	T_J	– 40	125	°C
SERDES Supply Voltage	V_{DD_ANA}, V_{DDGB}	1.425	1.575	V
SERDES CML I/O Supply Voltage	V_{DDIB}, V_{DDOB}	1.425	1.89	V

1. For FPGA Recommended Operating Conditions and Electrical Characteristics, see the Recommended Operating Conditions and Electrical Characteristics tables in the ORCA Series 4 FPGA data sheet (OR4E04) and the ORCA Series 4 I/O Buffer Technical Note. FPSC Standby Currents (IDDSB15 and IDDSB33) are tested with the Embedded Core in the powered down state.

SERDES Electrical and Timing Characteristics

Table 31. Absolute Maximum Ratings

Parameter	Conditions	Max.[1]	Units
ORT82G5 Power Dissipation	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 1.25 Gbit/s	195	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 2.50 Gbit/s	210	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 3.125 Gbit/s	225	mW
	8b/10b Encoder/Decoder (per Channel)	50	mW
ORT42G5 Power Dissipation	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 1.25 Gbit/s	265	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 2.50 Gbit/s	275	mW
	SERDES, MUX/DEMUX, Align FIFO and I/O (per channel), 3.125 Gbit/s	295	mW
	8b/10b Encoder/Decoder (per Channel)	50	mW

1. With all channels operating, 1.575V supply.

External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 38 specifies reference clock requirements, over the full range of operating conditions. The designer is encourage to read TN1040, *SERDES Reference Clock,* which discusses various aspects of this system element and its interconnection.

Table 38. Reference Clock Specifications (REFCLKP and REFCLKN)

Parameter	Min.	Typ.	Max.	Units
Frequency Range	60	—	185	MHz
Frequency Tolerance[1]	-350	—	350	ppm
Duty Cycle (Measured at 50% Amplitude Point)	40	50	60	%
Rise Time	—	500	1000	ps
Fall Time	—	500	1000	ps
P–N Input Skew	—	—	75	ps
Differential Amplitude	500	800	2 x V_{DDIB}	mV_{p-p}
Common Mode Level	$V_{single-ended/2}$	0.75	$V_{DD15} – (V_{single-ended/2})$	V
Single-Ended Amplitude	250	400	V_{DDIB}	mV_{p-p}
Input Capacitance (at REFCLKP)	—	—	5	pF
Input Capacitance (at REFCLKN)	—	—	5	pF

1. This specification indicates the capability of the high speed receiver CDR PLL to acquire lock when the reference clock frequency and incoming data rate are not synchronized.

Embedded Core Timing Characteristics

Table 39 summarizes the end-to-end latencies through the embedded core for the various modes. All latencies are given in clock cycles for system clocks at half the REFCLK_[A:B] frequency. For a REFCLK_[A:B] of 156.25 MHz, a system clock cycle is 6.4 ns.

Table 39. Signal Latencies, Embedded Core

Operating Mode	Signal Latency (max.)
Transmit Path	5 clock cycles
Receive Path	
Multi-Channel Alignment Bypassed[1]	4.5 clock cycles
With Multi-Channel Alignment[1]	13.5-22.5 clock cycles

1. With multi-channel alignment, the latency is largest when the skew between channels is at the maximum that can be correctly compensated for (18 clock cycles). The latency specified in the table is for data from the channel received first.

- Example connections are shown in Figure 40. The naming convention for the power supply sources shown in the figure are as follows:
  - Supply_1.5V – Tx-Rx digital, auxiliary power pins.
  - Supply_VDDIB – Input Rx buffer power pins.
  - Supply_VDDOB – Output Tx buffer power pins.
  - Supply_VDDANA – Tx analog power pins, Rx analog power pins, guard band power pins.

Figure 40. Power Supply Filtering

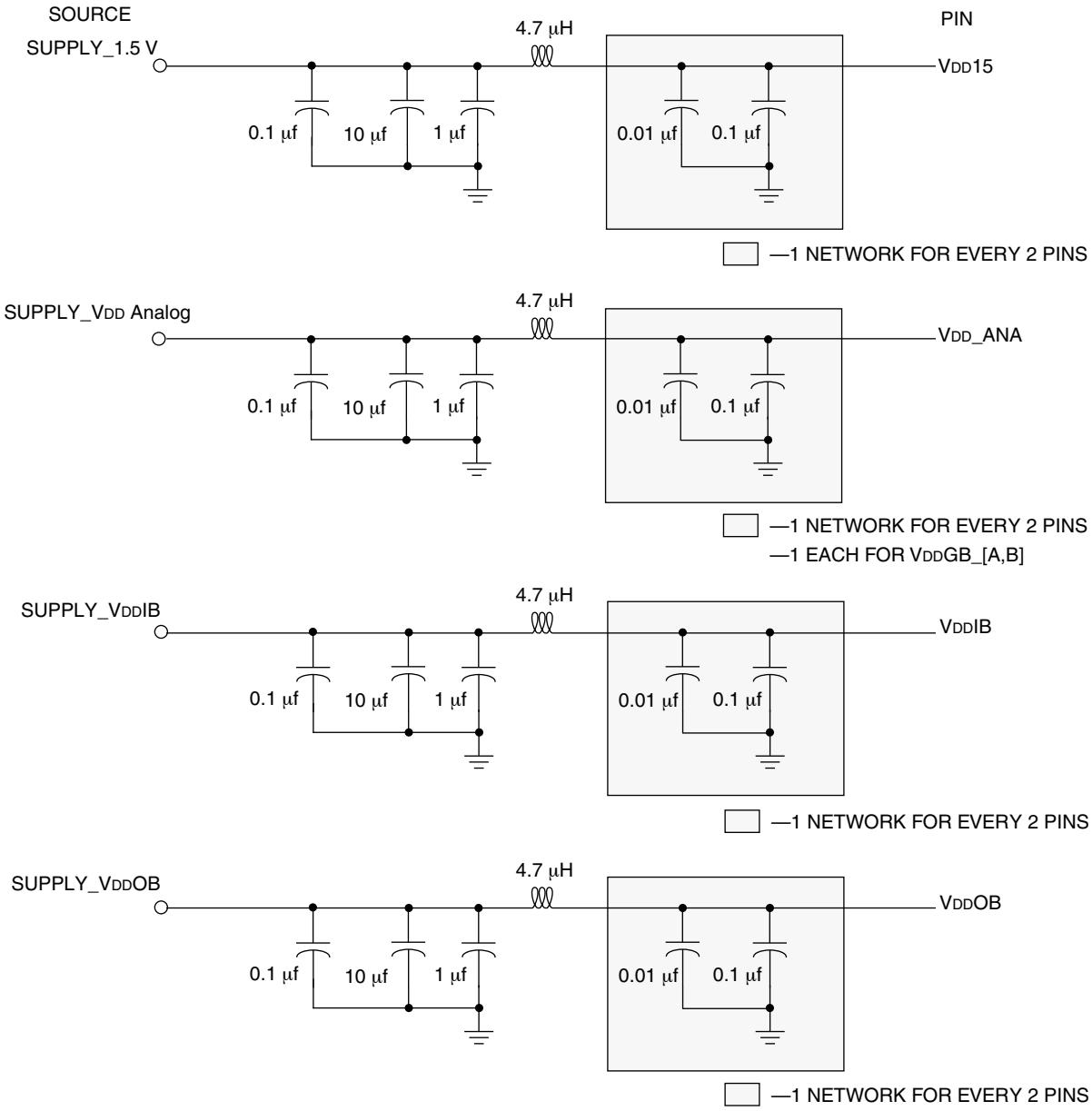


Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
N19	-	-	VDD_ANA	VDD_ANA	-	-
M19	-	-	VSS	VSS	-	-
P16	-	-	VDD_ANA	VDD_ANA	-	-
H21	-	-	I	HDINP_AC	-	HSP_9
R16	-	-	VSS	VSS	-	-
H22	-	-	I	HDINN_AC	-	HSN_9
P17	-	-	VDD_ANA	VDD_ANA	-	-
G20	-	-	VDDIB	VDDIB_AC	-	-
P18	-	-	VDD_ANA	VDD_ANA	-	-
P19	-	-	VDD_ANA	VDD_ANA	-	-
T17	-	-	VDD_ANA	VDD_ANA	-	-
T18	-	-	VDD_ANA	VDD_ANA	-	-
R17	-	-	VSS	VSS	-	-
G21	-	-	I	REFCLKP_A	-	HSP_10
G22	-	-	I	REFCLKN_A	-	HSN_10
F21	-	-	O	REXTN_A	-	-
F22	-	-	O	REXT_A	-	-
U18	-	-	VDD_ANA	VDD_ANA	-	-
E21	-	-	VDDGB_A	VDDGB_A	-	-
E22	-	-	VSS	VSS	-	-
D21	-	-	O	PSYS_RSSIG_ALL	-	-
D22	-	-	I	PSYS_DOBISTN	-	-
D20	-	-	VDD33	VDD33	-	-
K15	-	-	VDD15	VDD15	-	-
K10	-	-	VSS	VSS	-	-
L7	-	-	VDD15	VDD15	-	-
D19	-	-	I	PBIST_TEST_ENN	-	-
D18	-	-	I	PLOOP_TEST_ENN	-	-
L15	-	-	VDD15	VDD15	-	-
E17	-	-	I	PASB_PDN	-	-
K11	-	-	VSS	VSS	-	-
D17	-	-	VDD33	VDD33	-	-
M7	-	-	VDD15	VDD15	-	-
C21	-	-	I	PASB_RESETN	-	-
C22	-	-	I	PASB_TRISTN	-	-
K12	-	-	VSS	VSS	-	-
E16	-	-	I	PASB_TESTCLK	-	-
M15	-	-	VDD15	VDD15	-	-
C17	-	-	VDD33	VDD33	-	-
D16	1 (TC)	7	IO	PT36D	-	-
C16	1 (TC)	7	IO	PT36B	-	-
F14	1 (TC)	7	IO	PT35D	-	-
F15	1 (TC)	7	IO	PT35B	-	-
E14	1 (TC)	7	IO	PT34D	VREF_1_07	-

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
L11	-	-	VSS	VSS	-	-
N15	-	-	VDD15	VDD15	-	-
D10	1 (TC)	5	IO	PT18D	PTCK1C	L68C
C10	1 (TC)	5	IO	PT18C	PTCK1T	L68T
A12	1 (TC)	5	IO	PT17D	PTCK0C	L69C
B12	1 (TC)	5	IO	PT17C	PTCK0T	L69T
P6	-	-	VDD15	VDD15	-	-
A11	1 (TC)	5	IO	PT16D	VREF_1_05	L70C
B11	1 (TC)	5	IO	PT16C	-	L70T
L12	-	-	VSS	VSS	-	-
D9	1 (TC)	6	IO	PT15D	-	L71C
C9	1 (TC)	6	IO	PT15C	-	L71T
G15	1 (TC)	-	VDDIO1	VDDIO1	-	-
B10	1 (TC)	6	IO	PT14D	-	L72C
A10	1 (TC)	6	IO	PT14C	VREF_1_06	L72T
B9	0 (TL)	1	IO	PT13D	MPI_RTRY_N	L73C
A9	0 (TL)	1	IO	PT13C	MPI_ACK_N	L73T
D8	0 (TL)	1	IO	PT12D	M0	L74C
C8	0 (TL)	1	IO	PT12C	M1	L74T
A22	-	-	VSS	VSS	-	-
B8	0 (TL)	2	IO	PT12B	MPI_CLK	L75C
A8	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L75T
C7	0 (TL)	2	IO	PT11D	M2	L76C
D7	0 (TL)	2	IO	PT11C	M3	L76T
E9	0 (TL)	-	VDDIO0	VDDIO0	-	-
E6	0 (TL)	2	IO	PT11A	MPI_TEA_N	-
F6	-	-	VDD15	VDD15	-	-
B7	0 (TL)	3	IO	PT9D	VREF_0_03	L77C
A7	0 (TL)	3	IO	PT9C	-	L77T
A6	0 (TL)	3	IO	PT8D	D0	L78C
B6	0 (TL)	3	IO	PT8C	TMS	L78T
C6	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L79C
D6	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L79T
B1	-	-	VSS	VSS	-	-
A5	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L80C
B5	0 (TL)	4	IO	PT6C	D3	L80T
C5	0 (TL)	5	IO	PT5D	D1	L81C
D5	0 (TL)	5	IO	PT5C	D2	L81T
B2	-	-	VSS	VSS	-	-
A4	0 (TL)	5	IO	PT4D	TDI	L82C
B4	0 (TL)	5	IO	PT4C	TCK	L82T
E10	0 (TL)	-	VDDIO0	VDDIO0	-	-
B22	-	-	VSS	VSS	-	-
C4	0 (TL)	6	IO	PT2D	PLL_CK1C/PPLL	L83C

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AB20	—	—	Vss	Vss	—	—
C3	—	—	VDD33	VDD33	—	—
E4	—	—	O	PRD_DATA	RD_DATA/TDO	—
F5	—	—	I	PRESET_N	RESET_N	—
G5	—	—	I	PRD_CFG_N	RD_CFG_N	—
D3	—	—	I	PPRGRM_N	PRGRM_N	—
A2	0 (TL)	—	VDDIO0	VDDIO0	—	—
F4	0 (TL)	7	IO	PL2D	PLL_CK0C/HPPLL	L21C_A0
G4	0 (TL)	7	IO	PL2C	PLL_CK0T/HPPLL	L21T_A0
B3	0 (TL)	—	VDDIO0	VDDIO0	—	—
C2	0 (TL)	7	IO	PL3D	—	L22C_D0
B1	0 (TL)	7	IO	PL3C	VREF_0_07	L22T_D0
A1	—	—	Vss	VSS	—	—
J5	0 (TL)	7	IO	PL4D	D5	L23C_A0
H5	0 (TL)	7	IO	PL4C	D6	L23T_A0
B7	0 (TL)	—	VDDIO0	VDDIO0	—	—
E3	0 (TL)	8	IO	PL4B	—	L24C_A0
F3	0 (TL)	8	IO	PL4A	VREF_0_08	L24T_A0
C1	0 (TL)	8	IO	PL5D	HDC	L25C_D0
D2	0 (TL)	8	IO	PL5C	LDC_N	L25T_D0
A34	—	—	VSS	VSS	—	—
G3	0 (TL)	8	IO	PL5B	—	L26C_D0
H4	0 (TL)	8	IO	PL5A	—	L26T_D0
E2	0 (TL)	9	IO	PL6D	TESTCFG	L27C_D0
D1	0 (TL)	9	IO	PL6C	D7	L27T_D0
C5	0 (TL)	—	VDDIO0	VDDIO0	—	—
F2	0 (TL)	9	IO	PL7D	VREF_0_09	L28C_D0
E1	0 (TL)	9	IO	PL7C	A17/PPC_A31	L28T_D0
AA13	—	—	VSS	VSS	—	—
J4	0 (TL)	9	IO	PL7B	—	L29C_D0
K5	0 (TL)	9	IO	PL7A	—	L29T_D0
H3	0 (TL)	9	IO	PL8D	CS0_N	L30C_D0
G2	0 (TL)	9	IO	PL8C	CS1	L30T_D0
C9	0 (TL)	—	VDDIO0	VDDIO0	—	—
L5	0 (TL)	9	IO	PL8B	—	L31C_D0
K4	0 (TL)	9	IO	PL8A	—	L31T_D0
H2	0 (TL)	10	IO	PL9D	—	L32C_D0
J3	0 (TL)	10	IO	PL9C	—	L32T_D0
AA14	—	—	VSS	VSS	—	—
M5	0 (TL)	10	IO	PL9B	—	—
F1	0 (TL)	10	IO	PL10D	INIT_N	L33C_A0
G1	0 (TL)	10	IO	PL10C	DOUT	L33T_A0
K3	0 (TL)	10	IO	PL11D	VREF_0_10	L34C_D0
J2	0 (TL)	10	IO	PL11C	A16/PPC_A30	L34T_D0

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
D7	0 (TL)	—	VDDIO0	VDDIO0	—	—
C14	0 (TL)	1	IO	PT13B	—	L2C_A0
B14	0 (TL)	1	IO	PT13A	VREF_0_01	L2T_A0
A14	0 (TL)	1	IO	PT12D	M0	L3C_A0
A13	0 (TL)	1	IO	PT12C	M1	L3T_A0
AA20	—	—	Vss	Vss	—	—
E12	0 (TL)	2	IO	PT12B	MPI_CLK	L4C_A0
E13	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L4T_A0
C13	0 (TL)	2	IO	PT11D	M2	L5C_A0
C12	0 (TL)	2	IO	PT11C	M3	L5T_A0
B12	0 (TL)	2	IO	PT11B	VREF_0_02	L6C_A0
A12	0 (TL)	2	IO	PT11A	MPI_TEA_N	L6T_A0
D12	0 (TL)	3	IO	PT10D	—	L7C_D0
C11	0 (TL)	3	IO	PT10C	—	L7T_D0
B11	0 (TL)	3	IO	PT10B	—	—
A11	0 (TL)	3	IO	PT9D	VREF_0_03	L8C_A0
A10	0 (TL)	3	IO	PT9C	—	L8T_A0
AA21	—	—	Vss	Vss	—	—
B10	0 (TL)	3	IO	PT9B	—	—
E11	0 (TL)	3	IO	PT8D	D0	L9C_D0
D10	0 (TL)	3	IO	PT8C	TMS	L9T_D0
C10	0 (TL)	3	IO	PT8B	—	—
A9	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L10C_A0
B9	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L10T_A0
AA22	—	—	Vss	Vss	—	—
E10	0 (TL)	4	IO	PT7B	—	—
A8	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L11C_A0
B8	0 (TL)	4	IO	PT6C	D3	L11T_A0
D9	0 (TL)	4	IO	PT6B	VREF_0_04	L12C_D0
C8	0 (TL)	4	IO	PT6A	—	L12T_D0
E9	0 (TL)	5	IO	PT5D	D1	L13C_D0
D8	0 (TL)	5	IO	PT5C	D2	L13T_D0
AB13	—	—	Vss	Vss	—	—
A7	0 (TL)	5	IO	PT5B	—	L14C_A0
A6	0 (TL)	5	IO	PT5A	VREF_0_05	L14T_A0
C7	0 (TL)	5	IO	PT4D	TDI	L15C_D0
B6	0 (TL)	5	IO	PT4C	TCK	L15T_D0
E8	0 (TL)	5	IO	PT4B	—	L16C_A0
E7	0 (TL)	5	IO	PT4A	—	L16T_A0
A5	0 (TL)	6	IO	PT3D	—	L17C_A0
B5	0 (TL)	6	IO	PT3C	VREF_0_06	L17T_A0
AB14	—	—	Vss	Vss	—	—
C6	0 (TL)	6	IO	PT3B	—	L18C_A0
D6	0 (TL)	6	IO	PT3A	—	L18T_A0