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Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	372
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort82g5-2f680i

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ORCA ORT420	5 and ORT82G5	5 Data Sheet
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The transceivers are controlled and configured through the system bus in the FPGA logic and through the external 8-bit microprocessor interface of the FPGA. Each channel has associated dedicated registers that are readable and writable. There are also global registers for control of common circuitry and functions.

The SERDES performs 8b/10b encoding and decoding for each channel. The 8b/10b transmission code can support either Ethernet or Fibre Channel specifications for serial encoding/decoding, special characters, and error detection.

The user can disable the 8b/10b decoder to receive raw 10-bit words which will be rate reduced by the SERDES. If this mode is chosen, the user must bypass the multi-channel alignment FIFOs.

The SERDES block contains its own dedicated PLLs for both transmit and receive clock generation. The user provides a reference clock of the appropriate frequency. The receiver PLLs extract the clock from the serial input data and retime the data with the recovered clock.

MUX/DEMUX Block

The MUX/DEMUX block converts the data format for the high speed serial links to a wide, low-speed format for crossing the CORE/FPGA interface. The intermediate interface to the SERDES macrocell runs at 1/10th the bit rate of the data lane. The MUX/DEMUX converts the data rate and bus width so the interface to the FPGA core can run at 1/4th this intermediate frequency, giving a range of 25.0-92.5 MHz for the data rates into and out of the FPGA logic.

Multi-channel Alignment FIFOs

In the ORT82G5, the eight incoming data channels (four per SERDES block) can be independent of each other or can be synchronized in several ways. Two channels within a SERDES block can be aligned together; channels A and B and/or channels C and D. Alternatively, four channels in a SERDES block can be aligned together to form a communication channel with a bandwidth of 10 Gbps. Finally, the alignment can be extended across both SERDES blocks to align all eight channels. Individual channels within an alignment group can be disabled (i.e., powered down) without disrupting other channels.

In the ORT42G5, the four incoming data channels (two per SERDES block) can be independent of each other or can be synchronized in two ways. Two channels, channels C and D, within either SERDES block can be aligned together. Alternatively, all four channels can be aligned together to form a communication channel with a bandwidth of 10 Gbps. Individual channels within an alignment group can be disabled (i.e., powered down) without disrupting other channels.

XAUI and Fibre Channel Link State Machines

Two separate link state machines are included in the architecture. A XAUI link state machine is included in the embedded core modeled after the IEEE 802.3ae standard. A separate state machine for Fibre Channel is also implemented.

FPGA/Embedded Core Interface

In 8b/10b mode, the FPGA logic will receive/transmit 32-bits of data (up to 92.5 MHz) and 4 K_CTRL bits from/to the embedded core. There are 8 data streams in each direction plus additional timing, status and control signals.

Data sent to the FPGA can be aligned using comma (/K/) characters or /A/ character as specified either by Fibre Channel or by IEEE 802.3ae for XAUI based interfaces. The alignment character is made available to the FPGA along with the data. The special characters K28.1, K28.5 and K28.7 are treated as valid comma characters by the SERDES.

If the receive channel alignment FIFOs are bypassed, then each channel will provide its own receive clock in addition to data and comma character detect signals. If the 8b/10b decoders are bypassed, then 40-bit data streams are passed to the FPGA logic. No channel alignment can be done in 8b/10b bypass mode.

Transmit Path (FPGA to Backplane) Logic

The transmitter section accepts four groups of either 8-bit unencoded data or 10-bit encoded data at the parallel interface to the FPGA logic. It also uses the reference clock, REFCLK[P:N]_[A:B] to synthesize an internal high-speed serial bit clock. The serialized transmitted data are available at the differential CML output pins to drive either an optical transmitters, coaxial media or a circuit board backplane.

As shown in Figure 3, the basic blocks in the transmit path include:

Embedded Core/FPGA interface and 4:1 multiplexer

- Low speed parallel core/FPGA interface
- 4:1 multiplexer
- Transmit SERDES
- 8b/10b Encoder
- 10:1 Multiplexer
- CML Output Buffer

Detailed descriptions of the logic blocks are given in following sections. Detailed descriptions of transmit clock distribution, including the transmit PLL are given in later sections of this data sheet.

Figure 3. Basic Logic Blocks, Transmit Path, Single Channel (Typical Reference Clock Frequency)







XAUI Link Synchronization Function

For each lane, the receive section of the XAUI link state machine incorporates a synchronization state machine that monitors the status of the 10-bit alignment. A 10-bit alignment is done in the SERDES based on a comma character such as K28.5. A comma (0011111 or its complement 1100000) is a unique pattern in the 10-bit space that cannot appear across the boundary between any two valid 10-bit code-groups. This property makes the comma useful for delimiting code-groups in a serial stream. This mechanism incorporates a hysteresis to prevent false synchronization and loss of synchronization due to infrequent bit errors. For each lane, the sync_complete signal is disabled until the lane achieves synchronization. The synchronization state diagram is shown in Figure 10. This state machine is modeled after draft *IEEE* 802.3ae, version 2.1 but will also operate with version 4.1 implementations. Table 4 and Table 5 describe the state variables used in Figure 10. The XAUI state machine does not have any control over the SERDES byte aligner. It is the user's responsibility to control the byte aligner through software access of register map addresses 30800 and 30900.

Note that it takes four idle ordered sets (e.g. K28.5, Dxx.y, Dxx.y, Dxx.y) to bring the state machine from a loss_of_sync to a synch_acq'd_1 state. When back-to-back commas are used instead, it takes a total of five commas to achieve the same result as with idle ordered sets.

Function	Description
sync_complete	Indication that alignment code-group alignment has been established at the boundary indicated by the most recently received comma.
cg_comma	Indication that a valid code-group, with correct running disparity, containing a comma has been received.
cg_good	Indication that a valid code-group with the correct running disparity has been received.
cg_bad	Indication that an invalid code-group has been received.
no_comma	Indication that comma timer has expired. The timer is initialized upon receipt of a comma.

 Table 4. XAUI Link Synchronization State Diagram – Functions

Figure 12. Four Channel Alignment of SERDES Blocks A and B



ORT82G5 Multi-channel Alignment

The ORT82G5 has a total of eight channels (four per SERDES block). The incoming data of these channels can be synchronized in several ways or they can be independent of one other. Two channels within a SERDES block can be aligned together. Channel A and B and/or channel C and D can form a pair as shown in Figure 13. Alternately, all four channels of a SERDES block can be aligned together to form a communication channel with a bandwidth of 10 Gbps as shown in Figure 14. Finally, the alignment can be extended across both SERDES block to align all eight channels in ORT82G5 as shown in Figure 15. Individual channels within an alignment group can be disabled (i.e., powered down) without disrupting other channels.

Figure 13. Dual Channel Alignment



Figure 14. Alignment of SERDES Quads A and B



Figure 15. Alignment of all Eight SERDES Channels.



Note that any channel within an alignment group can be removed from that alignment group by setting FMPU_STR_EN_xx to 0. The disabling of any channel(s) within an alignment group will not affect the operation of the remaining active channels. If the active channels are synchronized, that synchronization will be maintained and no data loss will occur.

For every alignment group, there are both an OVFL and an OOS status register bit. The OVFL bit is set when alignment FIFO overflow occurs. The OOS bit is flagged when the down counter in the synchronization algorithm has reached a value of 0 and alignment characters from all channels within an alignment group have not been received. In the memory map section for the ORT42G5 the bits indicating OOS and OVFL are referred to as SYNC2_[A:B]_OOS and SYNC4_OOS and the bits indicating OVFL are SYNC2_[A:B]_OVFL and SYNC4_OVFL.

In the memory map section for the ORT82G5, the bits indicating OOS and OVFL are referred to as SYNC2_[A1,A2,B1,B2]_OOS, SYNC4_[A:B]_OOS and SYNC8_OOS and the bits indicating OVFL are SYNC2_[A1,A2,B1,B2]_OVFL, SYNC4_[A:B]_OVFL and SYNC8_OVFL.

Alignment can also be done between the receive channels on two ORT82G5 devices. Each of the two devices needs to provide its aligned K_CTRL or other alignment character to the other device, which will delay reading from a second alignment FIFO until all channels requesting alignment on the current device and all channels requesting alignment on the other device are aligned (as indicated on the K_CTRL character). These second alignment FIFOs will be implemented in FPGA logic on the ORT82G5. This scheme also requires that the reference clock for both devices be driven by the same signal.

XAUI Lane Alignment Function (Lane Deskew)

In XAUI mode, the receive section in each lane uses the /A/ code group to compensate for lane-to-lane skew. The mechanism restores the timing relationship between the 4 lanes by lining up the /A/ characters into a column. Figure 16 shows the alignment of four lanes based on /A/ character. A minimum spacing of 16 code-groups implies that at least \pm 80 bits of skew compensation capability should be provided, which the devices significantly exceed.



Figure 16. Deskew Lanes by Aligning /A/ Columns

Mixing Half-rate, Full-rate Modes

When channel alignment is enabled, all receive channels within an alignment group should be configured at the same rate. For example, in the ORT82G5 channels AA, AB, can be configured for twin alignment and full-rate mode, while channels AC, AD that form an alignment group can be configured for half-rate mode. In block alignment mode, each receive block can be configured in either half or full-rate mode.

When channel alignment is disabled within a block, any receive channel within the block can be used in half-rate or full-rate mode. The clocking strategy for half-rate mode in both scenarios (channel alignment enabled or disabled) is described in the Reference Clocks and Internal Clock Distribution sections later in this data sheet.

Multi-channel Alignment Configuration

ORT42G5 Configuration

At startup, the legacy SERDES channel logic must be powered down and removed from any multi-channel alignment groups:

- Setting bit 1 to one in registers at locations 30002, 30012, 30102, 30112, 30003, 30013, 30103 and 30113 powers down the legacy logic. (Note that the reset value for these bits is 0.)
- Setting bits 4 and 5 to zero (reset condition) in the register at locations 30810 and 30910 removes the legacy logic from any alignment group.

Register settings for multi-channel alignment are shown in Table 6.

Table 6. Multichannel Alignment Modes

Register Bits FMPU_SYNMODE_[A:B][0:7]	Mode
0000000	No multichannel alignment.
00001010	Twin channel alignment.
00001111	Four channel alignment.

To align two channels in SERDES A:

• FMPU_SYNMODE_A = 00001010 (Register Location 30811)

To align two channels in SERDES B:

• FMPU_SYNMODE_B = 00001010 (Register Location 30911)

To align all four channels:

• FMPU_SYNMODE_A = 00001111 (Register Location 30811)

• FMPU_SYNMODE_B = 11111111 (Register Location 30911)

To enable/disable multi-channel alignment of individual channels within a multi-channel alignment group:

- FMPU_STR_EN_xx = 1 enabled
- FMPU_STR_EN_xx = 0 disabled
- (Register Location 30810 and 30910, where xx is one of AC, AD, BC or BD.)

To resynchronize a multichannel alignment group set the following bit to zero, and then set it to one.

- FMPU_RESYNC4 for four channels, AC, AD, BC and BD. (Register Location 30A02, bit 2)
- FMPU_RESYNC2A for dual channels, AC and AD. (Register Location 30820, bit 5)
- FMPU_RESYNC2B for block channels, BC and BD. (Register Location 30920, bit 5)

To resynchronize an independent channel (resetting the write and the read pointer of the FIFO) set the following bit to zero, and then set it to one.

FMPU_RESYNC1_xx (Register Locations 30820 and 30920, bits 2 and 3, where xx is one of AC, AD, BC or BD).

ORT82G5 Configuration

Register settings for multi-channel alignment are shown in Table 7.

Table 7. Multi-channel Alignment Modes

Register Bits FMPU_SYNMODE_xx[0:1]	Mode
00	No multi-channel alignment.
10	Twin channel alignment.
01	Quad channel alignment.
11	Eight channel alignment.

Note: Where xx is one of A[A:D] and B[A:D].

To align all eight channels:

- FMPU_SYNMODE_A[A:D] = 11
- FMPU_SYNMODE_B[A:D] = 11

To align all four channels in SERDES A:

• FMPU_SYNMODE_A[A:D] = 01

To align two channels in SERDES A:

- FMPU_SYNMODE_A[A:B] = 10 for channel AA and AB
- FMPU_SYNMODE_A[C:D] = 10 for channel AC and AD

A similar alignment can be defined for SERDES B.

To enable/disable synchronization signal of individual channel within a multi-channel alignment group:

- FMPU_STR_EN_xx = 1 enabled
- FMPU_STR_EN_xx = 0 disabled

where xx is one of A[A:D] and B[A:D].

To resynchronize a multi-channel alignment group set the following bit to zero, and then set it to one:

- FMPU_RESYNC8 for eight channel A[A:D] and B[A:D]
- FMPU_RESYNC4A for quad channel A[A:D]
- FMPU_RESYNC2A1 for twin channel A[A:B]

Start Up Sequence for the ORT42G5

The following sequence is required by the ORT42G5 device. For information required for simulation that may be different than this sequence, see the ORT42G5 Design Kit.

- 1. Initiate a hardware reset by making PASB_RESETN low. Keep this low during FPGA configuration of the device. The device will be ready for operation 3 ms after the low to high transition of PASB_RESETN.
- 2. At startup, the legacy SERDES channel logic must be powered down and removed from any multi-channel alignment groups:
 - Setting bit 1 to one in registers at locations 30002, 30012, 30102, 30112, 30003, 30013, 30103 and 30113 powers down the legacy logic. (Note that the reset value for these bits is 0.)
 - Setting bits 4 and 5 to zero (reset condition) in the register at locations 30810 and 30910 removes the legacy logic from any alignment group.
- 3. Configure the following SERDES internal and external registers. Note that after device initialization, all alarm and status bits should be read once to clear them. A subsequent read will provide the valid state.

Set the following bits in register 30800:

- Bits LCKREFN_[AC and AD] to 1, which implies lock to data.
- Bits ENBYSYNC_[AC and AD] to 1 which enables dynamic alignment to comma.

Set the following bits in register 30801:

- Bits LOOPENB_[AC and AD] to 1 if high-speed serial loopback is desired.

Set the following bits in register 30900:

- Bits LCKREFN_[BC and BD] to 1 which implies lock to data.
- Bits ENBYSYNC_[BC and BD] to 1 which enables dynamic alignment to comma.

Set the following bits in register 30901:

- Bits LOOPENB_[BC and BD] to 1 if high-speed serial loopback is desired.

Set the following bits in registers 30022, 30032, 30122, 30132:

- TXHR set to 1 if TX half-rate is desired.
- 8b10bT set to 1 if 8b10b encoding is desired.

Set the following bits in registers 30023, 30033, 30123, 30133:

- RXHR Set to 1 if RX half-rate is desired.
- 8b10bR set to 1 if 8b10b decoding is desired.
- LINKSM set to 1 if the Fibre Channel state machine is desired.

Assert GSWRST bit by writing 1's to both SERDES blocks. Deassert GSWRST bit by writing 0's to both SER-DES blocks. Wait 3 ms. If higher speed serial loopback has been selected, the receive PLLs will use this time to lock to the new serial data.

Monitor the following alarm bits in registers 30020, 30030, 30120, 30130: – LKI, PLL lock indicator. 1 indicates that PLL has achieved lock.

4. If 8b/10b mode is enabled, enable link synchronization by periodically sending the following sequence three times:

- K28.5 D21.4 D21.5 D21.5 or any other idle ordered set (starting with a /comma/) in FC mode.

- /comma/ characters for the XAUI state machine and /A/ characters for word and channel alignment in XAUI mode.

As mentioned earlier, both sections of a slice can be written independently / simultaneously, due to the independent CSW per section.

The same signal illustration above applies to slice B by changing _A to _B.

SDRAM A and SDRAM B in Figure 34 refer to the built-in sections A and B of one EAC RAM slice.

These SDRAMS should not be confused with the FPGA SDRAMS, which are generated through Module Generator in ispLEVER. The EAC SDRAMs are always built-in to the embedded core section of the ORT82G5/42G5 and their pins are accessed through the EAC interface. In order for these pins to be available at the interface in the generated HDL models from ispLEVER, the "Use the Extra Memory in FPSC Core" checkbox needs to be checked in the customization window (after hitting the "customize" button) in Module Generator, while generating the ORT82G5/42G5 core HDL. These signals will not otherwise show in the interface model.

Figure 35 and Figure 36 show, per slice, timing diagrams for both write and read accesses. These figures do not include the _x section, which refers to either slice A or B, even though this is implied. Signal names and functions are summarized in Table 26 and follow the general ORCA Series 4 naming conventions.

Figure 34. Block Diagram, Embedded Core Memory Slice



which follows the Power PC convention where address bit 0 is the MSb and address bit 31 is the LSb. The MPI maps bits MPI_ADDR[14:31] to bits [17:0] of the system address bus. The User Master Interface (UMI) has an 18bit address bus and uses the opposite notation, where address line 17 is the MSb and address line 0 is the LSb. The UMI maps bits um_addr[17:0] to bits [17:0] of the system address bus. Because of the address mapping done by the MPI and UMI, the same hexadecimal address value is valid for both interfaces.

The UMI, internal and microprocessor interface data buses have both 32-bit data and 4-bit parity fields and the data fields are mapped 1:1 to each other, i.e., bit 0 is bit 0 for all three buses. The bit ordering is specific to the targeted functional block. In the memory map, only bits [0:7] are specified and the convention followed for sub-field descriptions is to map the bits in the description directly to the bit order given in the bit column. For example, to select channel C as the source for the transmit and receive clocks, the register at location 30A00 should have bits 0, 2, 4 and 6 set to zero and bits 1, 3, 5 and 7 set to one.

In the example in the previous paragraph, the bits being set are control bits and are independent of the MSb/LSb convention used. The resulting bit pattern 01010101 maps to the hexadecimal value AA if the left-most bit is considered the LSb and to 55 if the right-most bit is considered the LSb. In some cases, however, the data represents the value of a specific parameter, such as a size or threshold level, and the value may be stored at more than one address location, since each location can hold only 8 bits of data. For a given register, either the MSb or the LSb bit position is specified explicitly in the memory map. If the parameter value extends over multiple register locations, the relative bit or byte ordering is also specified. For additional information on the MPI and the system bus, see Technical Note TN1017, ORCA Series 4 MPI/System Bus.

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Ala	ırm Re	gisters (Read Only, Cle	ar on R	ead), xx = [AC, AD, BC or BD]
30020 - AC	[0]	Reserved	00	Reserved
30030 - AD	[1]	LKI_xx		Receive PLL Lock Indication, Channel xx. LKI_xx = 1 indicates the receive PLL is locked.
30120 - BC 30130 - BD	[2]	Not used	-	Reserved
[3] Not u	Not used		Reserved	
	[4:7]	Not used		Not used
SERDES Ala	irm Ma	sk Registers (Read/Wr	ite), xx :	= [AC, AD, BC or BD]
30021 - AC	[0]	Reserved	FF	Reserved, must be set to 1. Set to 1 on device reset.
30031 - AD	[1]	MLKI_xx		Mask Receive PLL Lock Indication, Channel xx.
30121 - BC	[2]	Reserved		Reserved. Must be set to 1. Set to 1 on device reset.
30131 - BD	[3]	Reserved	-	Reserved. Must be set to 1. Set to 1 on device reset.
	[4]	Reserved		Reserved. Must be set to 1. Set to 1 on device reset.
	[5]	Reserved		Reserved. Must be set to 1. Set to 1 on device reset.
	[6]	Reserved	1	Reserved. Must be set to 1. Set to 1 on device reset.
	[7]	Reserved	1	Reserved. Must be set to 1. Set to 1 on device reset.

Table 28. ORT42G5 Memory Map

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute			Reset Value	
Address	Bit	Name	(0x)	Description
Control Reg	isters	(Read/Write), xx=[AC, A	D, BC o	r BD]
30800 - Ax	[0]	—	00	Reserved for future use
30900 - Bx	[1]	_		Reserved for future use
	[2]	ENBYSYNC_xC		ENBYSYNC_xC= 1 Enables Receiver Byte Synchronization for Channel xC. ENBYSYNC_xC = 0 on device reset.
	[3]	ENBYSYNC_xD		ENBYSYNC_xD = 1 Enables Receiver Byte Synchronization for Channel xA. ENBYSYNC_xD = 0 on device reset.
	[4]	—	1	Reserved for future use
	[5]	—	1	Reserved for future use
	[6]	LCKREFN_xC		LCKREFN_xC = 0 Locks the receiver PLL to reference clock for Channel xC.
				LCKREFN_xC =1 = Locks the receiver to data for Channel xx. NOTE: When LCKREFN_xx = 0, the corresponding LKI_xx bit is also 0. LCKREFN_xC = 0 on device reset.
	[7]	LCKREFN_xD		LCKREFN_xD = 0 Locks the receiver PLL to reference clock for Channel xD. LCKREFN_xD =1 = Locks the receiver to data for Channel xA. NOTE: When LCKREFN_xx = 0, the corresponding LKI_xx bit is also 0. LCKREFN_xD = 0 on device reset.
30801 - Ax	[0]	_	00	Reserved for future use
30901 - Bx	[1]	—	1	Reserved for future use
	[2]	LOOPENB_xC		Enable Loopback Mode for Channel xC. When LOOPEN_xC=1, the transmitter high-speed output is looped back to the receiver high-speed input. This mode is similar to high-speed loopback mode enabled by TESTMODE_xx except that LOOPEN_xx disables the high-speed serial output. LOOPEN_xC=0 on device reset.
	[3]	LOOPENB_xD		Enable Loopback Mode for Channel xD. When LOOPEN_xD=1, the transmitter high-speed output is looped back to the receiver high-speed input. This mode is similar to high-speed loopback mode enabled by TESTMODE_xx except that LOOPEN_xx disables the high-speed serial output. LOOPEN_xD=0 on device reset.
	[4]	—]	Reserved for future use
	[5]	—]	Reserved for future use
	[6]	NOWDALIGN_xC		Word Align Disable Bit. When NOWDALIGN_xC=1, receiver word alignment is disabled for Channel xC. NOWDALIGN_xC=0 on device reset.
	[7]	NOWDALIGN_xD		Word Align Disable Bit. When NOWDALIGN_xD=1, receiver word alignment is disabled for Channel xD. NOWDALIGN_xD=0 on device reset.

ORT82G5 Memory Map

Each ORT82G5 SERDES block has eight independent channels. Each channel is identified by both a quad identifier, A or B, and a channel identifier, A, B, C or D. The registers in ORT82G5 are 8-bit memory locations, which can be classified into Status Register and Control Register.

Status Register

Read-only register to convey the status information of various operations within the FPSC core. An example is the state of the XAUI link-state-machine.

Control Register

Read-write register to set up the control inputs that define the operation of the FPSC core.

Reserved addresses for the FPSC register blocks are shown in Table 29.

Table 29. Structural Register Elements

Address (0x)	Description
300xx	SERDES A, internal registers.
301xx	SERDES B, internal registers.
308xx	Channel A [A:D] registers (external to SERDES blocks).
309xx	Channel B [A:D] registers (external to SERDES blocks).
30A0x	Global registers (external to SERDES blocks).

Table 30 details the memory map for the FPSC portion of the ORT82G5 device. In both Table 29 and Table 30, the addresses are given as 18-bit hexadecimal (18'h) values. The address may be sourced either through the Microprocessor interface or a User Master Interface. The MicroProcessor Interface (MPI) address bus is a 32-bit bus which follows the Power PC convention where address bit 0 is the MSb and address bit 31 is the LSb. The MPI maps bits MPI_ADDR[14:31] to bits [17:0] of the system address bus. The User Master Interface (UMI) has an 18-bit address bus and uses the opposite notation, where address line 17 is the MSb and address line 0 is the LSb. The UMI maps bits um_addr[17:0] to bits [17:0] of the system address bus. Because of the address mapping done by the MPI and UMI, the same hexadecimal address value is valid for both interfaces.

The UMI, internal and microprocessor interface data buses have both 32-bit data and 4-bit parity fields and the data fields are mapped 1:1 to each other, i.e., bit 0 is bit 0 for all three buses. The bit ordering is specific to the targeted functional block. In the memory map, only bits [0:7] are specified and the convention followed for sub-field descriptions is to map the bits in the description directly to the bit order given in the bit column. For example, to select channel C as the source for the transmit and receive clocks, the register at location 30A00 should have bits 0, 2, 4 and 6 set to zero and bits 1, 3, 5 and 7 set to one.

In the example in the previous paragraph, the bits being set are control bits and are independent of the MSb/LSb convention used. The resulting bit pattern 01010101 maps to the hexadecimal value AA if the left-most bit is considered the LSb and to 55 if the right-most bit is considered the LSb. In some cases, however, the data represents the value of a specific parameter, such as a size or threshold level, and the value may be stored at more than one address location, since each location can hold only 8 bits of data. For a given register, either the MSb or the LSb bit position is specified explicitly in the memory map. If the parameter value extends over multiple register locations, the relative bit or byte ordering is also specified. For additional information on the MPI and the system bus, see Technical Note TN1017, ORCA Series 4 MPI/System Bus.

Table 30. ORT82G5 Memo	ory Map (Continued)
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(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30003 - AA 30013 - AB 30023 - AC 30033 - AD	[0]	RXHR_xx	20	Receive Half Rate Selection Bit, Channel xx. When RXHR_xx =1, HDIN_xx's baud rate = (REFCLK[A:B]*10) and RCK78[A:B]=(REF- CLK[A:B]/4); when RXHR_xx=0, HDIN_xx's baud rate = (REF- CLK[A:B]*20) and RCK78[A:B]=(REFCLK/2). RXHR_xx = 0 on device reset.
30103 - BA 30113 - BB 30123 - BC	[1]	PWRDNR_xx		Receiver Power Down Control Bit, Channel xx. When $PWRDNR_xx = 1$, sections of the receive hardware are powered down to conserve power. $PWRDNR_xx = 0$ on device reset.
00100 - 00	[2]	Reserved		Reserved. Set to 1 on device reset.
	[3]	8b10bR_xx		Receive $8b/10b$ Decoder Enable Bit, Channel xx. When $8b10bR = 1$, the $8b/10b$ decoder in the receive path is enabled. Otherwise, the data is passed undecoded. $8b10bR_xx = 0$ on device reset.
	[4]	LINKSM_xx		Link State Machine Enable Bit, Channel xx. When LINKSM_xx = 1, the receiver Fiber Channel link state machine is enabled. Otherwise, the Fibre Channel link state machine is disabled. Note: LINKSM_xx is ignored when XAUI_MODE_xx=1. LINKSM_xx = 0 on device reset.
	[5:7]	Not used		Not used.
SERDES Cor	nmon Trans	smit and Receive C	hannel	Configuration Registers (Read/Write), xx=[AA,,BD]
30004 - AA	[0]	Reserved	See bit descrip.	Reserved, must be set to 0. Set to 0 on device reset.
30004 - AA 30014 - AB 30024 - AC 30034 - AD 30104 - BA 30114 - BB 30124 - BC 30134 - BD	[1]	MASK_xx		Transmit and Receive Alarm Mask Bit, Channel xx. When MASK_xx = 1, the transmit and receive alarms of a channel are prevented from gener- ating an interrupt (i.e., they are masked or disabled). The MASK_xx bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK_xx = 1 on device reset.
	[2]	SWRST_xx		Transmit and Receive Software Reset Bit, Channel xx. When SWRST_ss = 1, this bit provides the same function as the hardware reset, except that all configuration register settings are unaltered. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. SWRST = 0 on device reset.
	[3:6]	Not used		Not used. 0 on reset.
	[7]	TESTEN_xx		Transmit and Receive Test Enable Bit, Channel xx. When TESTEN_xx = 1, the transmit and receive sections are placed in test mode. The TestMode_[A:B][4:0] bits in the Global Control Registers specify the particular test, and must also be set. Note: When the global test enable bit GTESTEN_[A:B] = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN_[A:B] = 1, all channels are set to test mode regardless of their TESTEN setting. TESTEN_xx = 0 on device reset.

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Glo	bal Control	Registers (Read V	Vrite) Ac	t on all Four Channels in SERDES Quad A or SERDES Quad B.
30005 - A	[0]	Reserved	See	Reserved, must be set to 0. Set to 0 on device reset.
30105 - B	[1]	GMASK_[A:B]	bit descrip.	Global Mask. When GMASK_[A:B] = 1, the transmit and receive alarms of all channels in the SERDES quad are prevented from generating an interrupt (i.e., they are masked or disabled). The GMASK_[A:B] bit overrides the individual MASK_xx bits. GMASK_[A:B] = 1 on device reset.
	[2]	GSWRST_[A:B]		Software reset bit. The GSWRST_[A:B] bit provides the same function as the hardware reset for the transmit and receive sections of all four channels, except that the device configuration settings are not affected when GSWRST_[A:B] is asserted. This is not a self-clearing bit. Once set, this bit must be manually set and cleared. The GSWRST_[A:B] bit overrides the individual SWRST_xx bits. GSWRST_[A:B] = 0 on device reset.
	[3]	GPWRDNT_[A:B]		Powerdown Transmit Function. When GPWRDNT_[A:B] = 1, sections of the transmit hardware for all four channels of are powered down to conserve power. The GPWRDNT_[A:B] bit overrides the individual PWRDNT_xx bits. GPWRDNT_[A:B] = 0 on device reset.
	[4]	GPWRDNR_[A:B]		Powerdown Receive Function. When GPWRDNR_[A:B] = 1, sections of the receive hardware for all four channels are powered down to conserve power. The GPWRDNR_[A:B] bit overrides the individual PWRDNR_xx bits. GPWRDNR_[A:B] = 0 on device reset.
	[5]	Reserved		Reserved, 1 on device reset.
	[6]	Not used		Not used. 0 on reset.
	[7]	GTESTEN_[A:B]		Test Enable Control. When GTESTEN_[A:B] = 1, the transmit and receive sections of all four channels are placed in test mode. The GTESTEN_[A:B] bit overrides the individual TESTEN_xx bits. GTESTEN_[A:B] = 0 on device reset.
30006 - A	[0:4]	TestMode[A:B]	00	TestMode - See Test Mode section for settings
30106 - B	[5]	Not used		Not used
	[6:7]	Reserved		Reserved
Control Regi	isters (Read	/Write), xx=[AA,,	BD]	
30800 - Ax 30900 - Bx	[0]xA [1]xB [2]xC [3]xD	ENBYSYNC_xx	00	ENBYSYNC_xx = 1 Enables Receiver Byte Synchronization for Channel xx. ENBYSYNC_xx = 0 on device reset.
	[4]xA [5]xB [6]xC [7]xD	LCKREFN_xx		LCKREFN_xx = 0 Locks the receiver PLL to ref reference clock for Channel xx. LCKREFN_xx =1 = Locks the receiver to data for Channel xx. NOTE: When LCKREFN_xx = 0, the corresponding LKI_xx bit is also 0. LCKREFN_xx = 0 on device reset.
30801 - Ax 30901 - Bx	[0]xA [1]xB [2]xC [3]xD	LOOPENB_XX		Enable Loopback Mode for Channel xx. When LOOPEN_xx=1, the transmitter high-speed output is looped back to the receiver high-speed input. This mode is similar to high-speed loopback mode enabled by TESTMODE_xx except that LOOPEN_xx disables the high-speed serial output. LOOPEN_xx=0 on device reset.
	[4]xA [5]xB [6]xC [7]xD	NOWDALIGN_xx		Word Align Disable Bit. When NOWDALIGN_xx=1, receiver word align- ment is disabled for Channel xx. NOWDALIGN_xx=0 on device reset.

Table 30. ORT82G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30805 - Ax 30905 - Bx	[0]xA [1]xB [2]xC [3]xD	DEMUXWAS_xx	00	Status of Word Alignment. When DEMUX_WAS_xx=1, word alignment is achieved for Channel xx. DEMUX_WAS_xx=0 on device reset.
	[4]xA [5]xB [6]xC [7]xD	CH248_SYNC_xx		Status of Channel Alignment. When CH248_SYNC_xx=1, multi-channel alignment is achieved for Channel xx. CH248_SYNC_xx=0 on device reset.
30814 - Ax 30914 - Bx	[0] xA & AB [1] xC & xD	SYNC2_[A:B][1:2] OVFL	00	Multi-Channel Overflow Status. When SYNC2_[A:B][1:2]OVFL=1, dual- channel synchronization FIFO overflow has occurred. SYNC2_[A:B][1:2]OVFL=0 on device reset.
	[2]	SYNC4_ [A:B]OVFL		Multi-Channel Overflow Status. When SYNC4_[A:B]OVFL=1, quad- channel synchronization FIFO overflow has occurred. SYNC4_[A:B]OVFL=0 on device reset.
	[3] xA & AB [4] xC & xD	SYNC2_[A:B][1:2] OOS		Multi-Channel Out-Of-Sync Status. When SYNC2_[A:B][1:2] OOS=1, dual-channel synchronization has failed. SYNC2_[A:B][1:2] OOS=0 on device reset.
	[5]	SYNC4_[A:B]_OO S		Multi-Channel Out-Of-Sync Status. When SYNC4_[A:B]_OOS=1, quad- channel synchronization has failed. SYNC4_[A:B]_OOS=0 on device reset.
	[6:7]	Reserved for future	use.	
Common Co	ontrol Regis	ters (Read/Write)		
30A00	[0:1]	TCKSELA	00	Transmit Clock Select. Controls source of 78 MHz TCK78 for SERDES quad A 00 = Channel AA 10 = Channel AB 01 = Channel AC 11 = Channel AD
	[2:3	RCKSELA		Receive Clock Select. Controls source of 78 MHz RCK78 for SEDRES quad A 00 = Channel AA 10 = Channel AB 01 = Channel AC 11 = Channel AD
	[4:5]	TCKSELB		Transmit Clock Select. Controls source of 78 MHz TCK78 for SERDES quad B 00 = Channel BA 10 = Channel BB 01 = Channel BC 11 = Channel BD
	[6:7]	RCKSELB		Receive Clock Select. Controls source of 78 MHz RCK78 for SERDES quad B 00 = Channel BA 10 = Channel BB 01 = Channel BC 11 = Channel BD
30A01	[0:4]	—	00	Reserved for future use
	[5:7]	RX_FIFO_MIN		LSb's for the threshold for low address in RX_FIFOs. RX_FIFO_MIN, Bit 5 is LSb. Useful values for RX_FIFO_MIN [0:4] are 0 to 17(decimal).

High Speed Data Transmitter

Table 32 specifies serial data output buffer parameters measured on devices with typical and worst case process parameters and over the full range of operation conditions.

Table 32. Serial Output Timing and Levels (CML I/O)

Parameter	Min.	Тур.	Max.	Units
Rise Time (20%—80%)	50	80	110	ps
Fall Time (80%—20%)	50	80	110	ps
Common Mode	VDDOB - 0.30	VDDOB - 0.25	VDDOB - 0.15	V
Differential Swing (Full Amplitude) ¹	600	700	1000	mVp-p
Differential Swing (Half Amplitude) ¹	300	350	500	mVp-p
Output Load (external)	—	86	_	Ω

1. Differential swings measured at the end of 3 inches of FR-4 and 12 inches of coax cable.

Transmitter output jitter is a critical parameter to systems with high speed data links. Table 33 and Table 34 specify the transmitter output jitter for typical and worst case devices over the full range of operating conditions.

Table 33. Channel Output Jitter (3.125 Gbps)

Parameter	Device	Min.	Typ. ¹	Max. ¹	Units
Deterministic	ORT42G5	—	0.12	0.21	Ulp-p
Deterministic	ORT82G5	—	0.12	0.16	Ulp-p
Bandom	ORT42G5		0.05	0.10	Ulp-p
	ORT82G5	_	0.05	0.08	Ulp-p
Total ^{2, 3}	ORT42G5	—	0.17	0.31	Ulp-p
	ORT82G5		0.17	0.24	Ulp-p

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., 0°C to 85°C, 1.425V to 1.575V supply.

2. Wavecrest SIA-3000 instrument used to measure one-sigma (rms) random jitter component value. This value is multiplied by 14 to provide the peak-to-peak value that corresponds to a BER of 10⁻¹².

3. Total jitter measurement performed with Wavecrest SIA-3000 at a BER of 10⁻¹². See instrument documentation and other Wavecrest publications for a detailed discussion of jitter types included in this measurement.

Table 34. Channel Output Jitter (2.5 Gbps)

Parameter	Device	Min.	Typ. ¹	Max. ¹	Units
Deterministic	ORT42G5		0.11	0.13	Ulp-p
Deterministic	ORT82G5		0.11	0.13	Ulp-p
Bandom	ORT42G5	—	0.05	0.14	Ulp-p
	ORT82G5		0.05	0.07	Ulp-p
Total ^{2, 3}	ORT42G5		0.16	0.27	Ulp-p
	ORT82G5	—	0.16	0.20	Ulp-p

1. With PRBS 2^7-1 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., 0°C to 85°C, 1.425V to 1.575V supply.

2. Wavecrest SIA-3000 instrument used to measure one-sigma (rms) random jitter component value. This value is multiplied by 14 to provide the peak-to-peak value that corresponds to a BER of 10⁻¹².

Total jitter measurement performed with Wavecrest SIA-3000 at a BER of 10⁻¹². See instrument documentation and other Wavecrest publications for a detailed discussion of jitter types included in this measurement.

Lattice Semiconductor

- Example connections are shown in Figure 40. The naming convention for the power supply sources shown in the figure are as follows:
 - Supply_1.5V Tx-Rx digital, auxiliary power pins.
 - Supply_VDDIB Input Rx buffer power pins.
 - Supply_VDDOB Output Tx buffer power pins.
 - Supply_VDDANA Tx analog power pins, Rx analog power pins, guard band power pins.

Figure 40. Power Supply Filtering



484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
E15	1 (TC)	8	Ю	PT34B	-	-
D15	1 (TC)	8	Ю	PT33D	-	L53C
C15	1 (TC)	8	Ю	PT33C	VREF_1_08	L53T
E12	1 (TC)	-	VDDIO1	VDDIO1	-	-
C18	1 (TC)	8	Ю	PT32D	-	L54C
C19	1 (TC)	8	Ю	PT32C	-	L54T
K13	-	-	VSS	VSS	-	-
B21	1 (TC)	9	Ю	PT31D	-	L55C
A21	1 (TC)	9	Ю	PT31C	VREF_1_09	L55T
E13	1 (TC)	-	VDDIO1	VDDIO1	-	-
D14	1 (TC)	9	IO	PT30D	-	L56C
C14	1 (TC)	9	IO	PT30C	-	L56T
K14	-	-	VSS	VSS	-	-
B20	1 (TC)	9	Ю	PT29D	-	L57C
A20	1 (TC)	9	Ю	PT29C	-	L57T
N7	-	-	VDD15	VDD15	-	-
B19	1 (TC)	1	10	PT28D	-	L58C
A19	1 (TC)	1	10	PT28C	-	L58T
L8	-	-	VSS	VSS	-	-
D13	1 (TC)	1	IO	PT27D	VREF_1_01	L59C
C13	1 (TC)	1	IO	PT27C	-	L59T
E18	1 (TC)	-	VDDIO1	VDDIO1	-	-
A18	1 (TC)	1	10	PT27B	-	L60C
B18	1 (TC)	1	10	PT27A	-	L60T
A17	1 (TC)	2	IO	PT26D	-	L61C
B17	1 (TC)	2	IO	PT26C	VREF_1_02	L61T
L9	-	-	VSS	VSS	-	-
D12	1 (TC)	2	Ю	PT25D	-	L62C
C12	1 (TC)	2	Ю	PT25C	-	L62T
E19	1 (TC)	-	VDDIO1	VDDIO1	-	-
A16	1 (TC)	3	IO	PT24D	-	L63C
B16	1 (TC)	3	IO	PT24C	VREF_1_03	L63T
A15	1 (TC)	3	Ю	PT23D	-	L64C
B15	1 (TC)	3	Ю	PT23C	-	L64T
F16	1 (TC)	-	VDDIO1	VDDIO1	-	-
E11	1 (TC)	3	IO	PT22D	-	-
L10	-	-	VSS	VSS	-	-
D11	1 (TC)	4	Ю	PT21D	-	L65C
C11	1 (TC)	4	Ю	PT21C	-	L65T
A14	1 (TC)	4	Ю	PT20D	-	L66C
B14	1 (TC)	4	IO	PT20C	-	L66T
A13	1 (TC)	4	IO	PT19D	-	L67C
B13	1 (TC)	4	Ю	PT19C	VREF_1_04	L67T
G14	1 (TC)	-	VDDIO1	VDDIO1	-	-

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

Technical Support Assistance

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Revision History

Date	Version	Change Summary			
—	—	Previous Lattice releases.			
July 2008	07.0	BM680 conversion to F680 per PCN#09A-08.			