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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	372
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort82g5-3f680c

Programmable Features

- High-performance programmable logic:
  - 0.16 µm 7-level metal technology.
  - Internal performance of >250 MHz.
  - Over 400K usable system gates.
  - Meets multiple I/O interface standards.
  - 1.5V operation (30% less power than 1.8V operation) translates to greater performance.
- Traditional I/O selections:
  - LVTTL (3.3V) and LVCMOS (2.5V and 1.8V) I/Os.
  - Per pin-selectable I/O clamping diodes provide 3.3V PCI compliance.
  - Individually programmable drive capability: 24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
  - Two slew rates supported (fast and slew-limited).
  - Fast-capture input latch and input Flip-Flop (FF)/latch for reduced input setup time and zero hold time.
  - Fast open-drain drive capability.
  - Capability to register 3-state enable signal.
  - Off-chip clock drive capability.
  - Two-input function generator in output path.
- New programmable high-speed I/O:
  - Single-ended: GTL, GTL+, PECL, SSTL3/2 (class I and II), HSTL (Class I, III, IV), ZBT, and DDR.
  - Double-ended: LVDS, bused-LVDS, and LVPECL. Programmable (on/off) internal parallel termination (100 Ω) is also supported for these I/Os.
- New capability to (de)multiplex I/O signals:
  - New DDR on both input and output at rates up to 350 MHz (700 MHz effective rate).
  - New 2x and 4x downlink and uplink capability per I/O (i.e., 50 MHz internal to 200 MHz I/O).
- Enhanced twin-block Programmable Function Unit (PFU):
  - Eight 16-bit Look-Up Tables (LUTs) per PFU.
  - Nine user registers per PFU, one following each LUT, and organized to allow two nibbles to act independently, plus one extra for arithmetic operations.
  - New register control in each PFU has two independent programmable clocks, clock enables, local SET/RESET, and data selects.
  - New LUT structure allows flexible combinations of LUT4, LUT5, new LUT6, 4 → 1 MUX, new 8 → 1 MUX, and ripple mode arithmetic functions in the same PFU.
  - 32 x 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the Supplemental Logic and Interconnect Cell (SLIC) decoders as bank drivers.
  - Soft-Wired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU through fast internal routing which reduces routing congestion and improves speed.
  - Flexible fast access to PFU inputs from routing.
  - Fast-carry logic and routing to all four adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Abundant high-speed buffered and nonbuffered routing resources provide 2x average speed improvements over previous architectures.
- Hierarchical routing optimized for both local and global routing with dedicated routing resources. This results in faster routing times with predictable and efficient performance.
- SLIC provides eight 3-statable buffers, up to a 10-bit decoder, and PAL®-like AND-OR-Invert (AOI) in each programmable logic cell.
- New 200 MHz embedded block-port RAM blocks, two read ports, two write ports, and two sets of byte lane enables. Each embedded RAM block can be configured as:

FPGA Logic Overview

The ORCA Series 4 architecture is a new generation of SRAM-based programmable devices from Lattice. It includes enhancements and innovations geared toward today's high-speed systems on a single chip. Designed with networking applications in mind, the Series 4 family incorporates system-level features that can further reduce logic requirements and increase system speed. ORCA Series 4 devices contain many new patented enhancements and are offered in a variety of packages and speed grades.

The hierarchical architecture of the logic, clocks, routing, RAM, and system-level blocks create a seamless merge of FPGA and ASIC designs. Modular hardware and software technologies enable System-on-Chip integration with true plug-and-play design implementation.

The architecture consists of four basic elements: Programmable Logic Cells (PLCs), Programmable I/O cells (PIOs), Embedded Block RAMs (EBRs), plus supporting system-level features. These elements are interconnected with a rich routing fabric of both global and local wires. An array of PLCs is surrounded by common interface blocks which provide an abundant interface to the adjacent PLCs or system blocks. Routing congestion around these critical blocks is eliminated by the use of the same routing fabric implemented within the programmable logic core.

Each PLC contains a PFU, SLIC, local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU, but decoders, PAL-like functions, and 3-state buffering can be performed in the SLIC. The PIOs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, uplink and downlink functions, and other functions on two output signals.

Large blocks of 512 x 18 block-port RAM complement the existing distributed PFU memory. The RAM blocks can be used to implement RAM, ROM, FIFO, multiplier, and CAM. Some of the other system-level functions include the MPI, PLLs, and the Embedded System Bus (ESB).

PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) LUTs, eight latches/FFs, and one additional Flip-Flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-block fashion; two sets of four LUTs and FFs that can be controlled independently. Each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth FF for pipelining.

Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The FFs (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The FFs also have programmable clock polarity, clock enables, and local set/reset.

The SLIC is connected from PLC routing resources and from the outputs of the PFU. It contains eight 3-state, bidirectional buffers, and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT to perform PAL-like functions. The 3-state drivers in the SLIC and their direct connections from the PFU outputs make fast, true, 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

Programmable I/O

The Series 4 PIO addresses the demand for the flexibility to select I/Os that meet system interface requirements. I/Os can be programmed in the same manner as in previous ORCA devices, with the additional new features which allow the user the flexibility to select new I/O types that support High-Speed Interfaces.

Each PIO contains four programmable I/O pads and is interfaced through a common interface block to the FPGA array. The PIO is split into two pairs of I/O pads with each pair having independent clock enables, local set/reset, and global set/reset. On the input side, each PIO contains a programmable latch/Flip-Flop which enables very fast latching of data from any pad. The combination provides for very low setup requirements and zero hold times for

Additional Information

Contact your local Lattice representative for additional information regarding the ORCA Series 4 FPGA devices, or visit the Lattice web site at www.latticesemi.com.

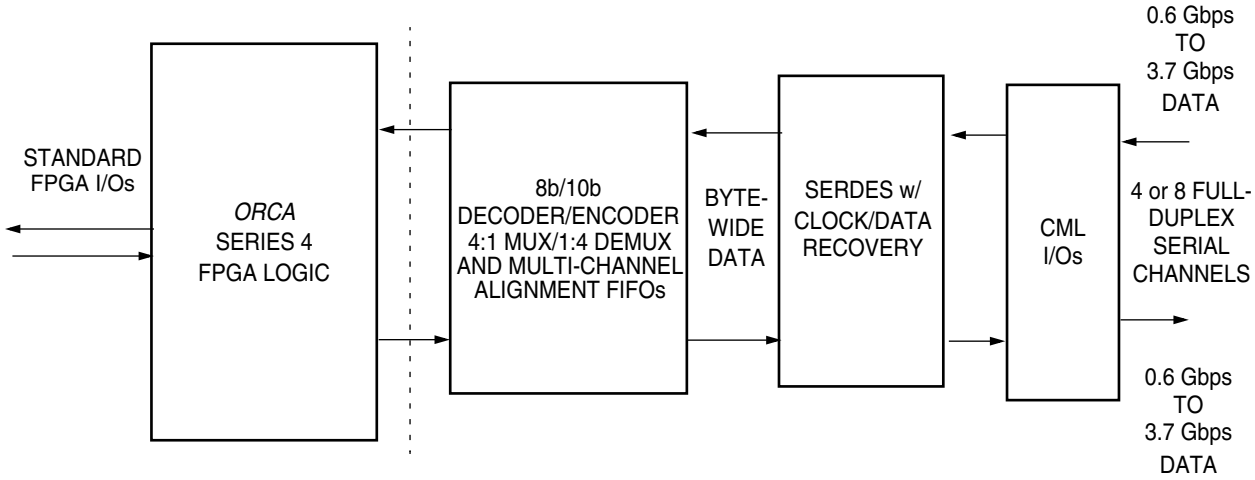
ORT42G5/ORT82G5 Overview

The ORT42G5 and ORT82G5 FPSCs provide high-speed backplane transceivers combined with FPGA logic. They are based on the 1.5V OR4E04 ORCA FPGA and have 36 x 36 arrays of Programmable Logic Cells (PLCs). The embedded core, which contains the backplane transceivers is attached to the right side of the device and is integrated directly into the FPGA array. A top level diagram of the basic chip configuration is shown in Figure 1.

Embedded Core Overview

The embedded core portions of the ORT42G5 and ORT82G5 contain respectively four or eight Clock and Data Recovery (CDR) macrocells and Serialize/Deserialize (SERDES) blocks and support 8b/10b (*IEEE* 802.3.2002) encoded serial links. It is intended for high-speed serial backplane data transmission. Figure 1 shows the ORT42G5 and ORT82G5 top level block diagram and the basic data flow. Boundary scan for the ORT42G5/ORT82G5 only includes programmable I/Os and does not include any of the embedded block I/Os.

Figure 1. ORT42G5/ORT82G5 Top Level Block Diagram



The serial channels can each operate at up to 3.7 Gbps (2.96 Gbps data rate) with a full-duplex synchronous interface with built-in clock recovery (CDR). The 8b/10b encoding provides guaranteed ones density for the CDR, byte alignment, and error detection. The core is also capable of frame synchronization and physical link monitoring and contains independent 4k x 36 RAM blocks. Overviews of the various blocks in the embedded core are presented in the following paragraphs.

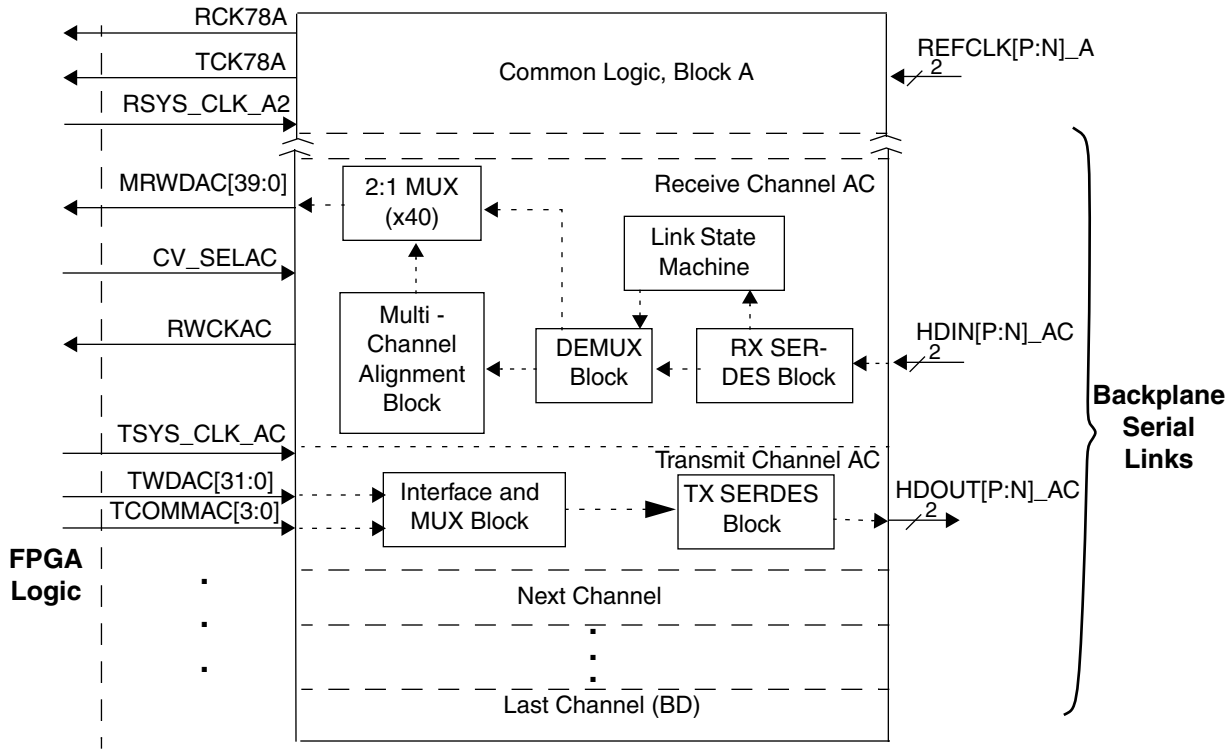
Serializer and Deserializer (SERDES)

The SERDES portion of the core contains two transceiver blocks for serial data transmission at a selectable data rate of 0.6 to 3.7 Gbps. Each SERDES channel features high-speed 8b/10b parallel I/O interfaces to other core blocks and high-speed CML interfaces to the serial links.

The SERDES circuitry consists of receiver, transmitter, and auxiliary functional blocks. The receiver accepts high-speed (up to 3.7 Gbps) serial data. Based on data transitions, the receiver locks an analog receive PLL for each channel to retime the data, then demultiplexes the data down to parallel bytes and an accompanying clock.

The transmitter operates in the reverse direction. Parallel bytes are multiplexed up to 3.7 Gbps serial data for off-chip communication. The transmitter generates the necessary 3.7 GHz clocks for operation from a lower speed reference clock.

Figure 2. Top Level Block Diagram, Embedded Core Logic (Channel AC)



The Embedded Core provides transceiver functionality for four or eight serial data channels and is organized into two blocks, each supporting two or four channels. Each channel is identified by both a block identifier [A:B] and a channel identifier [A:D]. In the ORT42G5 only the channel identifiers C and D are used. (This naming convention follows that of the ORT82G5).

The data channels can operate independently or they can be combined together (aligned) to achieve higher bit rates. The mode operation of the core is defined by a set of control registers, which can be written through the system bus interface. Also, the status of the core is stored in a set of status registers, which can be read through the system bus interface.

The transmitter section for each channel accepts 40 bits of data or 32 bits of data and eight control/status bits from the FPGA logic and optionally encodes the data using 8b/10b encoding. It also accepts the low-speed reference clock at the REFCLK input and uses this clock to synthesize the internal high-speed serial bit clock. The data is then serialized and the serialized data are available at the differential CML output terminated in 86 Ω to drive either an optical transmitter or coaxial media or circuit board/backplane.

The receiver section receives high-speed serial data at its differential CML input port. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. The retimed data are also deserialized and optionally 8b/10b decoded. The receiver also optionally recognizes the comma characters or code violations and aligns the bit stream to the proper word boundary. The resulting parallel data is optionally passed to the multi-channel alignment block before it is presented to the FPGA logic.

8b/10b Encoding and Decoding

In 8b/10b mode, the FPGA logic will receive/transmit 32 bits of data and 4 K_CTRL bits from/to the embedded core. In the transmit direction, four additional input bits force a negative disparity present state. The embedded core logic will encode the data to or decode the data from a 10-bit format according to the FC-PH ANSI X3.230:1994 standard (which is also the encoding used by the IEEE 802.3ae Ethernet standard). This encoding/decoding scheme also allows for the transmission of special characters and supports error detection.

Transmit Path (FPGA to Backplane) Logic

The transmitter section accepts four groups of either 8-bit unencoded data or 10-bit encoded data at the parallel interface to the FPGA logic. It also uses the reference clock, REFCLK[P:N]_[A:B] to synthesize an internal high-speed serial bit clock. The serialized transmitted data are available at the differential CML output pins to drive either an optical transmitters, coaxial media or a circuit board backplane.

As shown in Figure 3, the basic blocks in the transmit path include:

Embedded Core/FPGA interface and 4:1 multiplexer

- Low speed parallel core/FPGA interface
- 4:1 multiplexer

Transmit SERDES

- 8b/10b Encoder
- 10:1 Multiplexer
- CML Output Buffer

Detailed descriptions of the logic blocks are given in following sections. Detailed descriptions of transmit clock distribution, including the transmit PLL are given in later sections of this data sheet.

Figure 3. Basic Logic Blocks, Transmit Path, Single Channel (Typical Reference Clock Frequency)

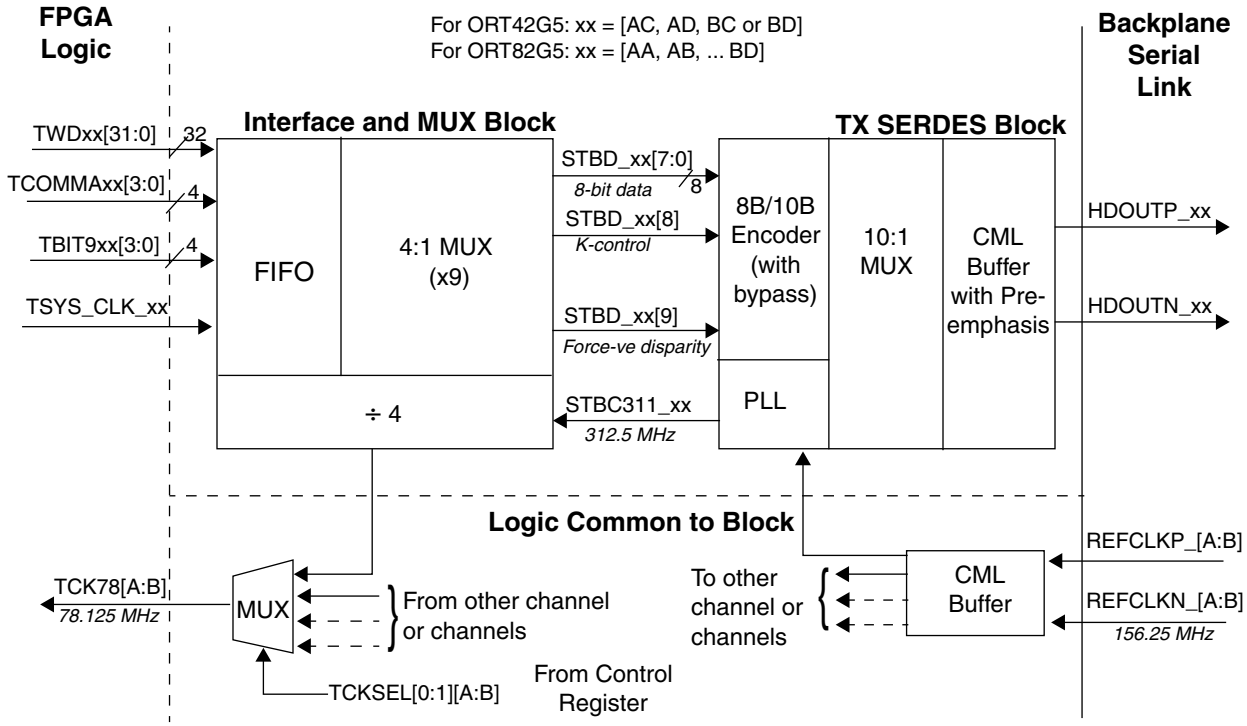
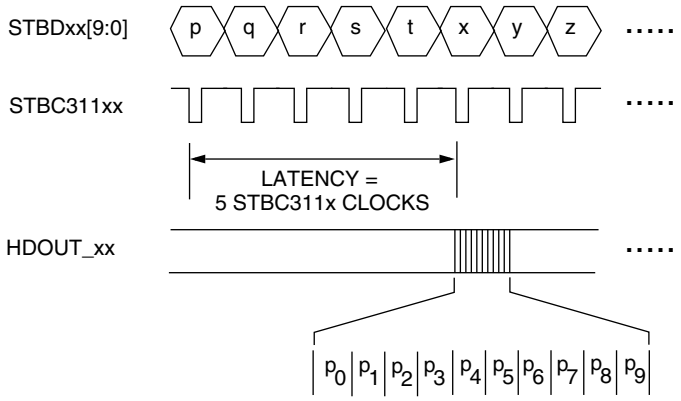


Figure 5. Transmit Path Timing - Single SERDES Channel



Each block also sends a clock to the FPGA logic. This clock, TCK78[A,B], is sourced from one of the four MUX blocks and has the same frequency as TSYS_CLK_xx, but arbitrary phase. Within each MUX block, the low frequency clock output is obtained by dividing by 4 the SERDES STBC311x clock which is used internally to synchronize the transmit data words. TCKSEL control bits select the channel to source TCK78[A:B].

The internal signals STBDxx[9:0] (where xx is represents AA...BD or AC, AD, BC, BD) from the MUX block carry unencoded character data and control bits. The 10th bit (STBDxx[9]) of each data lane into the SERDES is used to force a negative disparity present state.

8b/10b Encoder and 1:10 Multiplexer

The 8b/10b encoder encodes the incoming 8-bit data into a 10-bit format as described previously. The input signals to the block, STBDxx[7:0] are used for the 8-bit unencoded data. STBDxx[8] is used as the K_control input to indicate whether the 8 data bits need to be encoded as special characters (K_control = 1) or as data characters (K_control = 0). When STBDxx[9:0] = 1, a negative disparity present state is forced. When the encoder is bypassed STBDxx[9:0] serve as the data bits for the 10-bit unencoded data.

Within the definition of the 8b/10b transmission code, the bit positions of the 10-bit encoded transmission characters are labeled as a, b, c, d, e, i, f, g, h, and j in that order. Bit a corresponds to STBDxx[0], bit b to STBDxx[1], bit c to STBDxx[2], bit d to STBDxx[3], bit e to STBDxx[4], bit i to STBDxx[5], bit f to STBDxx[6], bit g to STBDxx[7], bit h to STBDxx[8], and bit j to STBDxx[9].

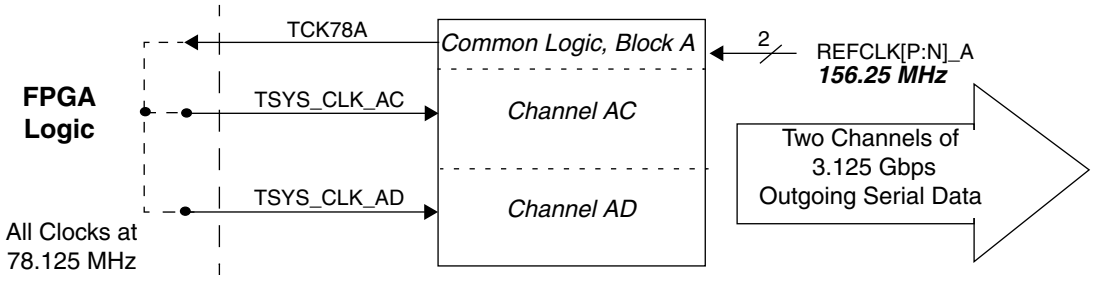
The 10-bit wide parallel data is converted to serial data by the 10:1 Multiplexer. The serial data are then sent to the CML output buffer and are transmitted serially with STBDxx[0] transmitted first and STBDxx[9] transmitted last.

CML Output Buffer

The transmitter's CML output buffer is terminated on-chip in 86 ohms to optimize the data eye as well as to reduce the number of discrete components required. The differential output swing reaches a maximum of 1.2 V_{PP} in the normal amplitude mode. A half amplitude mode can be selected via configuration register bit HAMP_xx. Half amplitude mode can be used to reduce power dissipation when the transmission medium has minimal attenuation or for testing of the integrity (loss) of the physical medium.

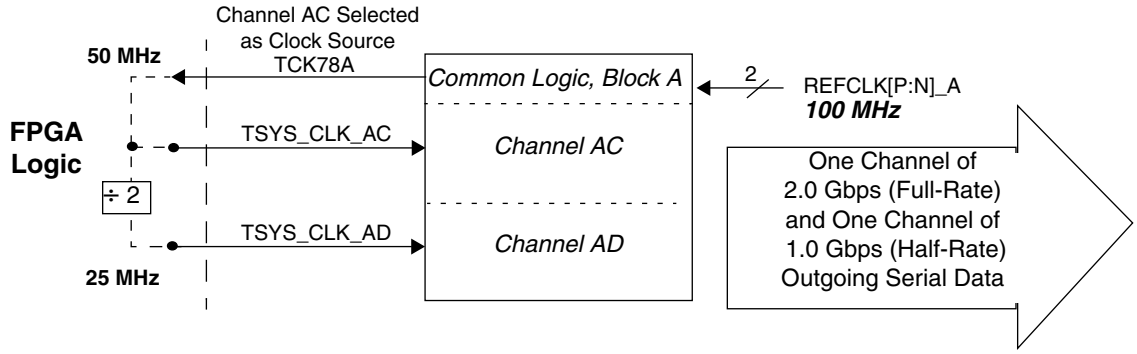
A programmable preemphasis circuit is provided to boost the high frequencies in the transmit data signal to maximize the data eye opening at the far-end receiver. Preemphasis is particularly useful when the data are transmitted over backplanes or low-quality coax cables which have a frequency-dependent amplitude loss. For example, for FR4 material at 2.5 GHz, the attenuation compared to the 1.0 GHz value is about 3 dB. The attenuation is a result of skin effect loss of the PCB conductor and the dielectric loss of the PCB substrate. This attenuation causes intersymbol interface which results in the closing of the data eye opening at the receiver.

Figure 18. Transmit Clocking for a Single Block (Similar Connections Would Be Used for Block B)



If the transmit line rate is mixed between half and full rate among the channels, then the scheme shown in Figure 19 can be used. The figure shows TSYS_CLK_AC being sourced by TCK78A and TSYS_CLK_AD being sourced by TCK78A/2 (the division is done in FPGA logic). Similar clocking would be used for Block B.

Figure 19. Mixed Rate Transmit Clocking for a Single Block (Similar Connections Would Be Used for Block B)



Receive Clock Source Selection and Recommended Clock Distribution

In the receive path, one clock per block of two channels, called RCK78[A:B], is sent to the FPGA logic. The control register bits RCKSEL[A:B] is used to select the clock source for these clocks. The selection of the source for RCK78[A:B] is controlled by this bit as shown in Table 15.

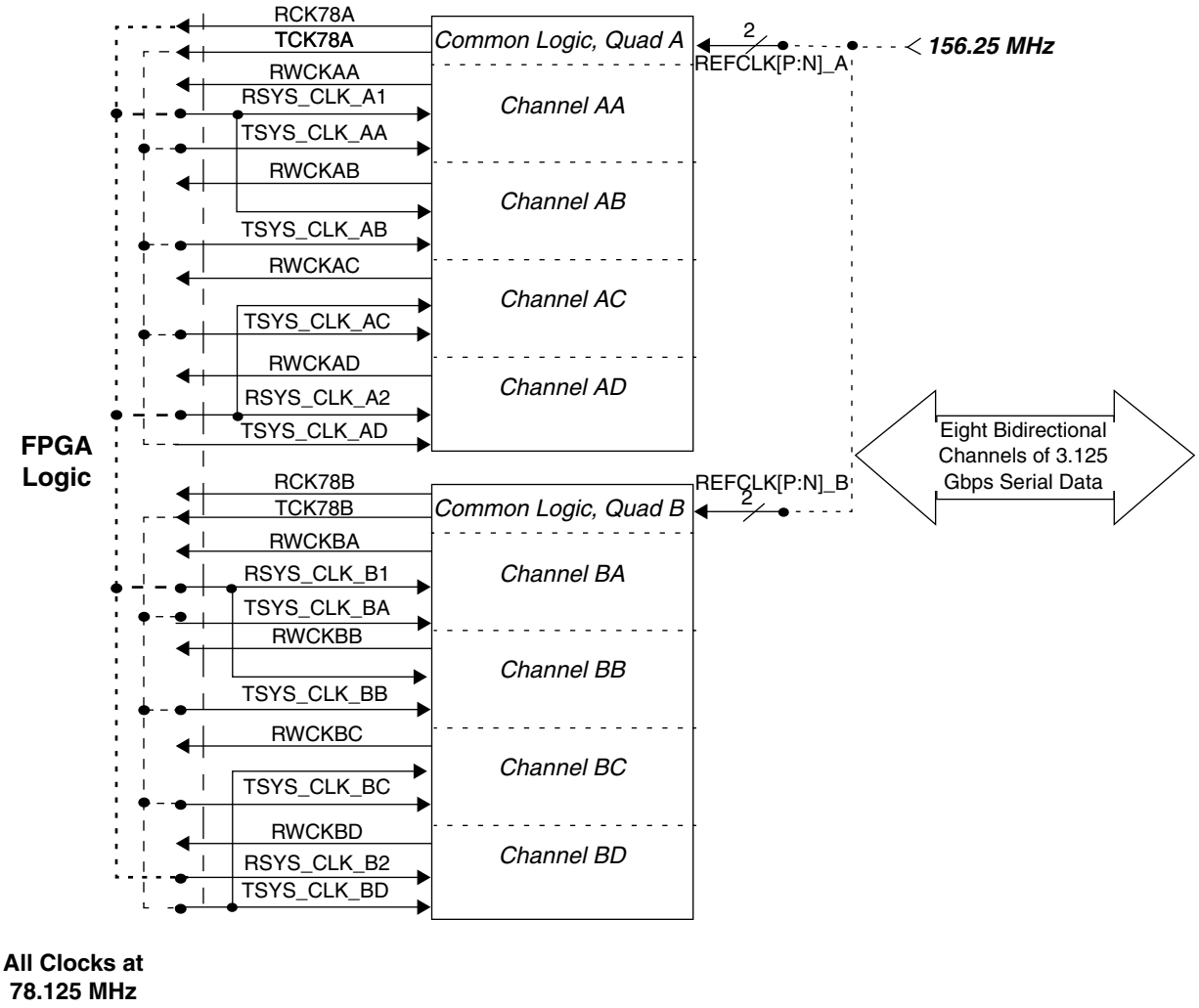
Table 15. RCK78[A:B] Source Selection

RCKSEL[A:B]	Clock Source
0	Channel C
1	Channel D

In the receive channel alignment bypass mode the data and recovered clocks for the four channels are independent. The data for each channel are synchronized to the recovered clock from that channel.

Figure 21 shows the recommended receive clocking for a single block.

Figure 31. Clocking for Eight Channel Alignment



Reset Operation

The SERDES block can be reset in one of three different ways as follows: on power up, using the hardware reset, or via the microprocessor interface. The power up reset process begins when the power supply voltage ramps up to approximately 80% of the nominal value of 1.5V. Following this event, the device will be ready for normal operation after 3 ms.

A hardware reset is initiated by making the PASB_RESETN low for at least two microprocessor clock cycles. The device will be ready for operation 3 ms after the low to high transition of the PASB_RESETN. This reset function affects all SERDES channels and resets all microprocessor and internal registers and counters.

Using the software reset option, each channel can be individually reset by setting SWRST (bit 2) to a logic 1 in the channel configuration register. The device will be ready 3 ms after the SWRST bit is deasserted. Similarly, all four channels per quad SERDES can be reset by setting the global reset bit GSWRST. The device will be ready for normal operation 3 ms after the GSWRST bit is deasserted. Note that the software reset option resets only SERDES internal registers and counters. The microprocessor registers are not affected. It should also be noted that the embedded block cannot be accessed until after FPGA configuration is complete.

Register Address	Bit Value	Bit Name	Comments
30801, 30901	Bit 0 =1 (Channel A) Bit 1 = 1 (Channel B) Bit 2 = 1 (Channel C) Bit 3 = 1 (Channel D)	LOOPENB_xx	Set any of the bits 0-3 to 1 to do serial loopback on the corresponding channel.* The high speed serial outputs will not be active.

*This test mode can also be set using TESTEN_xx in place of LOOPENB_xx. In that case, Test Mode must be set to 00000.

Parallel Loopback at the SERDES Boundary

In this parallel loopback differential data are received at the HDINP_xx and HDINN_xx pins and are retransmitted at the HDOUTP_xx and HDOUTN_xx pins. The loopback path is at the interface between the SERDES blocks and the MUX and DEMUX blocks and uses the parallel 10-bit buses at these interfaces (see Figure 32b). The loopback connection is made such that the input signals to the TX SERDES block is the same as the output signals from the RX SERDES block. In this parallel loopback mode, the MRWDxx[39:0] signal lines remain active and the TWDxx[31:0], TCOMMAxx[3:0] and TBIT9xx[3:0] signal lines are not used. This mode is normally used for tests where serial test data is received from and transmitted to either test equipment or via a serial backplane to a remote card and is the basic loopback path shown earlier in Figure 32(b).

The data rate selection bits TXHR and RXHR in the channel configuration registers must be configured to carry the same value. Also, the 8b/10b encoder and decoder are excluded from the loopback path by setting the 8b10bT and 8b10bR configuration bits to 0. Table 21 and Table 22 illustrate the control interface register configuration for the parallel loopback.

Table 21. Parallel Loopback at the SERDES Boundary Configuration Bit Definitions

Register Address (Hex)	Bit Value	Bit Name	Comments
30022, 30032, 30122, 30132	Bit 0 = 0 or 1	TXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 7 = 0	8b10bT	Set to 0 The 8b/10b encoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to 0.
30023, 30033, 30123, 30133	Bit 0 = 0 or 1	RXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 3 = 0	8b10bR	Set to 0.The 8b/10b decoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to 0.
30005, 30105	Bit 7 = 1	GTESTEN	SET to 1 if the loopback is done globally on both channels.
30026, 30036, 30126, 30136	Bits[4:0]	Testmode	Set to 00001

Table 22. Parallel Loopback at the SERDES Boundary Configuration Bit Definitions for the ORT82G5

Register Address (Hex)	Bit Value	Bit Name	Comments
30002, 30012, 30022, 30032, 30102, 30112, 30122, 30132	Bit 0 = 0 or 1	TXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 7 = 0	8b10bT	Set to 0 The 8b/10b encoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to 0.
30003, 30013, 30023, 30033, 30103, 30113, 30123, 30133	Bit 0 = 0 or 1	RXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
	Bit 3 = 0	8b10bR	Set to 0.The 8b/10b decoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to 0.
30005, 30105	Bit 7 = 1	GTESTEN	SET to 1 if the loopback is done globally on all four channels.
30006, 30016, 30026, 30036, 30106, 30116, 30126, 30136	Bits[4:0]	Testmode	Set to 00001

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30933	[0:3]	—	00	Reserved for future use.
	[4:5]	—		Reserved for future use.
	[6]	—		Reserved for future use.
	[7]	—		Reserved for future use.
Status Registers (Read Only, Clear on Read), xx = [AC, AD, BC or BD]				
30804 - Ax 30904 - Bx	[0:1]	—	00	Reserved for future use.
	[2:3]	—		Reserved for future use.
	[4:5]	XAUISTAT_xC		XAUI Status Register. Status of XAUI link state machine for Channel xC 00 – No synchronization, 10 – Synchronization done, 11 – Not used, 01 – no_comma (see XAUI state machine) and at least one CV detected. XAUISTAT_xC[0:1] = 00 on device reset.
	[6:7]	XAUISTAT_xD		XAUI Status Register. Status of XAUI link state machine for Channel xD 00 – No synchronization, 10 – Synchronization done, 11 – Not used, 01 – no_comma (see XAUI state machine) and at least one CV detected. XAUISTAT_xD[0:1] = 00 on device reset.
30805 - Ax 30905 - Bx	[0]]	—	00	Reserved for future use.
	[1]	—		Reserved for future use.
	[2]	DEMUXWAS_xC		Status of Word Alignment. When DEMUX_WAS_xC=1, word alignment is achieved for Channel xC. DEMUX_WAS_xC=0 on device reset.
	[3]	DEMUXWAS_xD		Status of Word Alignment. When DEMUX_WAS_xD=1, word alignment is achieved for Channel xD. DEMUX_WAS_xD=0 on device reset.
	[4]	—		Reserved for future use.
	[5]	—		Reserved for future use.
	[6]	CH24_SYNC_xC		Status of Channel Alignment. When CH24_SYNC_xC=1, multi-channel alignment is achieved for Channel xC. CH24_SYNC_xC=0 on device reset.
	[7]	CH24_SYNC_xD		Status of Channel Alignment. When CH24_SYNC_xD=1, multi-channel alignment is achieved for Channel xD. CH24_SYNC_xD=0 on device reset.
30814 - A 30914 - B	[0]	—	00	Reserved for future use.
	[1]	SYNC2_[A:B]_OVFL		Multi-Channel Overflow Status. When SYNC2_[A:B]_OVFL=1, twin channel synchronization FIFO overflow has occurred. SYNC2_[A:B]_OVFL=0 on device reset.
	[2:3]	—		Reserved for future use.
	[4]	SYNC2_[A:B]_OOS		Multi-Channel Out-Of-Sync Status. When SYNC2_[A:B]_OOS=1, twin channel synchronization has failed. SYNC2_[A:B]_OOS=0 on device reset.
	[5:7]	—		Reserved for future use.

Table 30. ORT82G5 Memory Map

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
SERDES Alarm Registers (Read Only), xx=[AA,...,BD]				
30000 - AA 30010 - AB 30020 - AC 30030 - AD 30100 - BA 30110 - BB 30120 - BC 30130 - BD	[0]	Reserved	00	Reserved
	[1]	LKI_xx		Receive PLL Lock Indication, Channel xx. LKI_xx = 1 indicates the receive PLL is locked.
	[2]	Reserved		Reserved
	[3]	Reserved		Reserved
	[4:7]	Not used		Not used
SERDES Alarm Mask Registers (Read/Write), xx=[AA,...,BD]				
30001 - AA 30011 - AB 30021 - AC 30031 - AD 30101 - BA 30111 - BB 30121 - BC 30131 - BD	[0]	Reserved	FF	Reserved, must be set to 1. Set to 1 on device reset.
	[1]	MLKI_xx		Mask Receive PLL Lock Indication, Channel xx.
	[2]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
	[3]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
	[4]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
	[5]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
	[6]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
	[7]	Reserved		Reserved, must be set to 1. Set to 1 on device reset.
SERDES Common Transmit and Receive Channel Configuration Registers (Read/Write), xx=[AA,...,BD]				
30002 - AA 30012 - AB 30022 - AC 30032 - AD 30102 - BA 30112 - BB 30122 - BC 30132 - BD	[0]	TXHR_xx	00	Transmit Half Rate Selection Bit, Channel xx. When TXHR_xx = 1, HDOUT_xx's baud rate = (REFCLK[A:B]*10) and TCK78[A:B] =(REFCLK[A:B]/4); when TXHR_xx=0, HDOUT_xx's baud rate = (REFCLK[A:B]*20) and TCK78[A:B]=(REFCLK[A:B]/2). TXHR_xx = 0 on device reset.
	[1]	PWRDNT_xx		Transmit Powerdown Control Bit, Channel xx. When PWRDNT_xx = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT_xx = 0 on device reset.
	[2]	PE0_xx		Transmit Preemphasis Selection Bit 0, Channel xx. PE0_xx and PE1_xx select one of three preemphasis settings for the transmit section. PEO_xx=PE1_xx = 0, Preemphasis is 0% PEO_xx=1, PE1_xx = 0 or PEO_xx=0, PE1_xx = 1, Preemphasis is 12.5% PEO_xx=PE1_xx = 1, Preemphasis is 25%. PEO_xx=PE1_xx = 0 on device reset.
	[3]	PE1_xx		
	[4]	HAMP_xx		Transmit Half Amplitude Selection Bit, Channel xx. When HAMP_xx = 1, the transmit output buffer voltage swing is limited to half its normal amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP_xx = 0 on device reset.
	[5]	Reserved		Reserved. Must be set to 0. Set to 0 on device reset.
	[6]	Reserved		Reserved
	[7]	8b10bT_xx		Transmit 8b/10b Encoder Enable Bit, Channel xx. When 8b10bT_xx = 1, the 8b/10b encoder in the transmit path is enabled. Otherwise, the data is passed unencoded. 8b10bT_xx = 0 on device reset.

Table 30. ORT82G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
30805 - Ax 30905 - Bx	[0]xA [1]xB [2]xC [3]xD	DEMUXWAS_xx	00	Status of Word Alignment. When DEMUX_WAS_xx=1, word alignment is achieved for Channel xx. DEMUX_WAS_xx=0 on device reset.
	[4]xA [5]xB [6]xC [7]xD	CH248_SYNC_xx		Status of Channel Alignment. When CH248_SYNC_xx=1, multi-channel alignment is achieved for Channel xx. CH248_SYNC_xx=0 on device reset.
30814 - Ax 30914 - Bx	[0] xA & AB [1] xC & xD	SYNC2_[A:B][1:2] OVFL	00	Multi-Channel Overflow Status. When SYNC2_[A:B][1:2]OVFL=1, dual-channel synchronization FIFO overflow has occurred. SYNC2_[A:B][1:2]OVFL=0 on device reset.
	[2]	SYNC4_ [A:B]OVFL		Multi-Channel Overflow Status. When SYNC4_[A:B]OVFL=1, quad-channel synchronization FIFO overflow has occurred. SYNC4_[A:B]OVFL=0 on device reset.
	[3] xA & AB [4] xC & xD	SYNC2_[A:B][1:2] OOS		Multi-Channel Out-Of-Sync Status. When SYNC2_[A:B][1:2] OOS=1, dual-channel synchronization has failed. SYNC2_[A:B][1:2] OOS=0 on device reset.
	[5]	SYNC4_[A:B]_OOS		Multi-Channel Out-Of-Sync Status. When SYNC4_[A:B]_OOS=1, quad-channel synchronization has failed. SYNC4_[A:B]_OOS=0 on device reset.
	[6:7]	Reserved for future use.		
Common Control Registers (Read/Write)				
30A00	[0:1]	TCKSELA	00	Transmit Clock Select. Controls source of 78 MHz TCK78 for SERDES quad A 00 = Channel AA 10 = Channel AB 01 = Channel AC 11 = Channel AD
	[2:3	RCKSELA		Receive Clock Select. Controls source of 78 MHz RCK78 for SEDRES quad A 00 = Channel AA 10 = Channel AB 01 = Channel AC 11 = Channel AD
	[4:5]	TCKSELB		Transmit Clock Select. Controls source of 78 MHz TCK78 for SERDES quad B 00 = Channel BA 10 = Channel BB 01 = Channel BC 11 = Channel BD
	[6:7]	RCKSELB		Receive Clock Select. Controls source of 78 MHz RCK78 for SERDES quad B 00 = Channel BA 10 = Channel BB 01 = Channel BC 11 = Channel BD
30A01	[0:4]	—	00	Reserved for future use
	[5:7]	RX_FIFO_MIN		LSb's for the threshold for low address in RX_FIFOs. RX_FIFO_MIN, Bit 5 is LSb. Useful values for RX_FIFO_MIN [0:4] are 0 to 17(decimal).

Pin Descriptions

This section describes the pins found on the Series 4 FPGAs. Any pin not described in this table is a user-programmable I/O. During configuration, the user-programmable I/Os are 3-stated with an internal pull-up resistor. If any pin is not used (or not bonded to a package pin), it is also 3-stated with an internal pull-up resistor after configuration. The pin descriptions in Table and throughout this data sheet show active-low signals with an overscore. The package pinout tables that follow, show this as a signal ending with _N. For example $\overline{\text{LDC}}$ and LDC_N are equivalent.

Table 40. Pin Descriptions

Symbol	I/O	Description
Dedicated Pins		
VDD33	—	3.3V positive power supply. This power supply is used for 3.3V configuration RAMs and internal PLLs. When using PLLs, this power supply should be well isolated from all other power supplies on the board for proper operation.
VDD15	—	1.5V positive power supply for internal logic.
VDDIO	—	Positive power supply used by I/O banks.
VSS	—	Ground.
PTEMP	I	Temperature sensing diode pin. Dedicated input.
$\overline{\text{RESET}}$	I	During configuration, $\overline{\text{RESET}}$ forces the restart of configuration and a pull-up is enabled. After configuration, $\overline{\text{RESET}}$ can be used as a general FPGA input or as a direct input, which causes all PLC latches/FFs to be asynchronously set/reset.
CCLK	O	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in.
	I	In the slave or readback after configuration, CCLK is input synchronous with the data on DIN or D[7:0]. CCLK is an output for daisy-chain operation when the lead device is in master, peripheral, or system bus modes.
DONE	I	As an input, a low level on DONE delays FPGA start-up after configuration.[1]
	O	As an active-high, open-drain output, a high level on this signal indicates that configuration is complete. DONE has an optional pull-up resistor.
PRGRM	I	$\overline{\text{PRGRM}}$ is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up.
RD_CFG	I	This pin must be held high during device initialization until the $\overline{\text{INIT}}$ pin goes high. This pin always has an active pull-up. During configuration, $\overline{\text{RD\_CFG}}$ is an active-low input that activates the TS_ALL function and 3-states all of the I/O. After configuration, $\overline{\text{RD\_CFG}}$ can be selected (via a bit stream option) to activate the TS_ALL function as described above, or, if readback is enabled via a bit stream option, a high-to-low transition on $\overline{\text{RD\_CFG}}$ will initiate readback of the configuration data, including PFU output states, starting with frame address 0.
RD_DATA/TDO	O	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary-scan, TDO is test data out.
$\overline{\text{CFG\_IRQ}}$/MPI_IRQ	O	During JTAG, slave, master, and asynchronous peripheral configuration assertion on this $\overline{\text{CFG\_IRQ}}$ (active-low) indicates an error or errors for block RAM or FPSC initialization. MPI active-low interrupt request output, when the MPI is used.
LVDS_R	—	Reference resistor connection for controlled impedance termination of Series 4 FPGA LVDS inputs.
Special-Purpose Pins		
M[3:0]	I	During powerup and initialization, M0—M3 are used to select the configuration mode with their values latched on the rising edge of $\overline{\text{INIT}}$. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O.[1]
PLL_CK[0:7][TC]	I	Semi-dedicated PLL clock pins. During configuration they are 3-stated with a pull up.
	I/O	These pins are user-programmable I/O pins if not used by PLLs after configuration.
P[TBLR]CLK[1:0][TC]	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.
	I/O	After configuration these pins are user programmable I/O, if not used for clock inputs.

This section describes device I/O signals to/from the embedded core.

Table 41. FPSC Function Pin Descriptions

Symbol	I/O	Description
Common Signals for Both SERDES Quad A and B		
PASB_RESETN	I	Active low reset for the embedded core. All non-SERDES specific registers (addresses 308***, 309***, 30A***) in the embedded core are not reset.[1]
PASB_TRISTN	I	Active low 3-state for embedded core output buffers.[1]
PASB_PDN	I	Active low power down of all SERDES blocks and associated I/Os.[1]
PASB_TESTCLK	I	Clock input for BIST and loopback test.[1]
PBIST_TEST_ENN	I	Selection of PASB_TESTCLK input for BIST test.[1]
PLOOP_TEST_ENN	I	Selection of PASB_TESTCLK input for loopback test.[1]
PMP_TESTCLK	I	Clock input for microprocessor in test mode.[1]
PMP_TESTCLK_ENN	I	Selection of PMP_TESTCLK in test mode.[1]
PSYS_DOBISTN	I	Input to start BIST test.[1]
PSYS_RSSIG_ALL	O	Output result of BIST test.
SERDES Quad A and B Pins		
REFCLKN_A	I	CML reference clock input—SERDES quad A.
REFCLKP_A	I	CML reference clock input—SERDES quad A.
REFCLKN_B	I	CML reference clock input—SERDES quad B.
REFCLKP_B	I	CML reference clock input—SERDES quad B.
REXT_A	—	Reference resistor – SERDES quad A.
REXT_B	—	Reference resistor – SERDES quad B.
REXTN_A	—	Reference resistor – SERDES quad -. A 3.32 K W ± 1% resistor must be connected across REXT_B and REXTN_B. This resistor should handle a current of 300 µA.
REXTN_B	—	Reference resistor – SERDES quad B. A 3.32 K Ω ± 1% resistor must be connected across REXT_B and REXTN_B. This register should handle a current of 300 µA
HDINN_AA (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad A, channel A.
HDINP_AA (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad A, channel A.
HDINN_AB (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad A, channel B.
HDINP_AB (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad A, channel B.
HDINN_AC	I	High-speed CML receive data input – SERDES quad A, channel C.
HDINP_AC	I	High-speed CML receive data input – SERDES quad A, channel C.
HDINN_AD	I	High-speed CML receive data input – SERDES quad A, channel D.
HDINP_AD	I	High-speed CML receive data input – SERDES quad A, channel D.
HDINN_BA (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad B, channel A.
HDINP_BA (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad B, channel A.
HDINN_BB (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad B, channel B.
HDINP_BB (ORT82G5 only)	I	High-speed CML receive data input – SERDES quad B, channel B.
HDINN_BC	I	High-speed CML receive data input – SERDES quad B, channel C.
HDINP_BC	I	High-speed CML receive data input – SERDES quad B, channel C.
HDINN_BD	I	High-speed CML receive data input – SERDES quad B, channel D.
HDINP_BD	I	High-speed CML receive data input – SERDES quad B, channel D.
SERDES quad A and B Pins		
HDOUTN_AA (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad A, channel A.
HDOUTP_AA (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad A, channel A.
HDOUTN_AB (ORT82G5 only)	O	High-speed CML transmit data output – SERDES quad A, channel B.

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
G9	-	-	VSS	VSS	-	-
L3	7 (CL)	5	IO	PL21D	A10/PPC_A24	L10C
L4	7 (CL)	5	IO	PL21C	A9/PPC_A23	L10T
L5	7 (CL)	5	IO	PL22D	A8/PPC_A22	-
F10	-	-	VDD15	VDD15	-	-
G10	-	-	VSS	VSS	-	-
M3	7 (CL)	6	IO	PL24D	PLCK1C	L11C
M4	7 (CL)	6	IO	PL24C	PLCK1T	L11T
N4	7 (CL)	6	IO	PL25C	A7/PPC_A21	-
M2	7 (CL)	6	IO	PL26D	A6/PPC_A20	L12C
M1	7 (CL)	6	IO	PL26C	A5/PPC_A19	L12T
N3	7 (CL)	7	IO	PL27D	WR_N/MPI_RW	-
F11	-	-	VDD15	VDD15	-	-
N5	7 (CL)	8	IO	PL28D	A4/PPC_A18	-
M5	7 (CL)	-	VDDIO7	VDDIO7	-	-
N2	7 (CL)	8	IO	PL29D	A3/PPC_A17	L13C
N1	7 (CL)	8	IO	PL29C	A2/PPC_A16	L13T
G11	-	-	VSS	VSS	-	-
P2	7 (CL)	8	IO	PL30D	A1/PPC_A15	L14C
P1	7 (CL)	8	IO	PL30C	A0/PPC_A14	L14T
F12	-	-	VDD15	VDD15	-	-
P3	7 (CL)	8	IO	PL31D	DP0	L15C
P4	7 (CL)	8	IO	PL31C	DP1	L15T
R4	6 (BL)	1	IO	PL32D	D8	L16C
R3	6 (BL)	1	IO	PL32C	VREF_6_01	L16T
R2	6 (BL)	1	IO	PL33D	D9	L17C
R1	6 (BL)	1	IO	PL33C	D10	L17T
G12	-	-	VSS	VSS	-	-
T3	6 (BL)	2	IO	PL34D	-	-
P5	6 (BL)	-	VDDIO6	VDDIO6	-	-
T2	6 (BL)	2	IO	PL34B	-	L18C
T1	6 (BL)	2	IO	PL34A	-	L18T
U1	6 (BL)	3	IO	PL35B	D11	L19C
U2	6 (BL)	3	IO	PL35A	D12	L19T
R5	6 (BL)	-	VDDIO6	VDDIO6	-	-
V1	6 (BL)	3	IO	PL36B	VREF_6_03	L20C
V2	6 (BL)	3	IO	PL36A	D13	L20T
G13	-	-	VSS	VSS	-	-
W2	6 (BL)	4	IO	PL37B	-	L21C
W1	6 (BL)	4	IO	PL37A	VREF_6_04	L21T
Y1	6 (BL)	4	IO	PL39D	PLL_CK7C/HPPLL	L22C
Y2	6 (BL)	4	IO	PL39C	PLL_CK7T/HPPLL	L22T
U3	-	-	I	PTEMP	PTEMP	-
F13	-	-	VDD15	VDD15	-	-

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
N19	-	-	VDD_ANA	VDD_ANA	-	-
M19	-	-	VSS	VSS	-	-
P16	-	-	VDD_ANA	VDD_ANA	-	-
H21	-	-	I	HDINP_AC	-	HSP_9
R16	-	-	VSS	VSS	-	-
H22	-	-	I	HDINN_AC	-	HSN_9
P17	-	-	VDD_ANA	VDD_ANA	-	-
G20	-	-	VDDIB	VDDIB_AC	-	-
P18	-	-	VDD_ANA	VDD_ANA	-	-
P19	-	-	VDD_ANA	VDD_ANA	-	-
T17	-	-	VDD_ANA	VDD_ANA	-	-
T18	-	-	VDD_ANA	VDD_ANA	-	-
R17	-	-	VSS	VSS	-	-
G21	-	-	I	REFCLKP_A	-	HSP_10
G22	-	-	I	REFCLKN_A	-	HSN_10
F21	-	-	O	REXTN_A	-	-
F22	-	-	O	REXT_A	-	-
U18	-	-	VDD_ANA	VDD_ANA	-	-
E21	-	-	VDDGB_A	VDDGB_A	-	-
E22	-	-	VSS	VSS	-	-
D21	-	-	O	PSYS_RSSIG_ALL	-	-
D22	-	-	I	PSYS_DOBISTN	-	-
D20	-	-	VDD33	VDD33	-	-
K15	-	-	VDD15	VDD15	-	-
K10	-	-	VSS	VSS	-	-
L7	-	-	VDD15	VDD15	-	-
D19	-	-	I	PBIST_TEST_ENN	-	-
D18	-	-	I	PLOOP_TEST_ENN	-	-
L15	-	-	VDD15	VDD15	-	-
E17	-	-	I	PASB_PDN	-	-
K11	-	-	VSS	VSS	-	-
D17	-	-	VDD33	VDD33	-	-
M7	-	-	VDD15	VDD15	-	-
C21	-	-	I	PASB_RESETN	-	-
C22	-	-	I	PASB_TRISTN	-	-
K12	-	-	VSS	VSS	-	-
E16	-	-	I	PASB_TESTCLK	-	-
M15	-	-	VDD15	VDD15	-	-
C17	-	-	VDD33	VDD33	-	-
D16	1 (TC)	7	IO	PT36D	-	-
C16	1 (TC)	7	IO	PT36B	-	-
F14	1 (TC)	7	IO	PT35D	-	-
F15	1 (TC)	7	IO	PT35B	-	-
E14	1 (TC)	7	IO	PT34D	VREF_1_07	-

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
W31	—	—	VSS	VSS	—	—
V30	—	—	VDDOB	VDDOB_BD	—	—
W33	—	—	O	HDOUTN_BD	—	—
H33	—	—	VSS	VSS	—	—
W34	—	—	O	HDOUTP_BD	—	—
V31	—	—	VDDOB	VDDOB_BD	—	—
H34	—	—	VSS	VSS	—	—
J32	—	—	VSS	VSS	—	—
U31	—	—	VDDOB	VDDOB_AD	—	—
T34	—	—	O	HDOUTP_AD	—	—
M32	—	—	VSS	VSS	—	—
T33	—	—	O	HDOUTN_AD	—	—
U30	—	—	VDDOB	VDDOB_AD	—	—
T31	—	—	VSS	VSS	—	—
R34	—	—	I	HDINP_AD	—	—
N32	—	—	VSS	VSS	—	—
R33	—	—	I	HDINN_AD	—	—
T30	—	—	VDDIB	VDDIB_AD	—	—
U32	—	—	VSS	VSS	—	—
R31	—	—	VDDOB	VDDOB_AC	—	—
P34	—	—	O	HDOUTP_AC	—	—
U33	—	—	VSS	VSS	—	—
P33	—	—	O	HDOUTN_AC	—	—
R30	—	—	VDDOB	VDDOB_AC	—	—
P31	—	—	VSS	VSS	—	—
N34	—	—	I	HDINP_AC	—	—
U34	—	—	VSS	VSS	—	—
N33	—	—	I	HDINN_AC	—	—
P30	—	—	VDDIB	VDDIB_AC	—	—
V32	—	—	VSS	VSS	—	—
M34	—	—	O	HDOUTP_AB	—	—
V33	—	—	VSS	VSS	—	—
M33	—	—	O	HDOUTN_AB	—	—
N31	—	—	VDDOB	VDDOB_AB	—	—
M31	—	—	VSS	VSS	—	—
L34	—	—	I	HDINP_AB	—	—
V34	—	—	VSS	VSS	—	—
L33	—	—	I	HDINN_AB	—	—
N30	—	—	VDDIB	VDDIB_AB	—	—
K34	—	—	O	HDOUTP_AA	—	—
K33	—	—	O	HDOUTN_AA	—	—
M30	—	—	VDDOB	VDDOB_AA	—	—
L32	—	—	VDD_ANA	VDD_ANA	—	—
L31	—	—	VSS	VSS	—	—

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
B24	1 (TC)	3	IO	PT23B	—	—
D20	1 (TC)	3	IO	PT22D	—	L15C_A0
D19	1 (TC)	3	IO	PT22C	—	L15T_A0
N14	—	—	Vss	Vss	—	—
E19	1 (TC)	3	IO	PT22B	—	L16C_A0
E18	1 (TC)	3	IO	PT22A	—	L16T_A0
C21	1 (TC)	4	IO	PT21D	—	L17C_A0
C20	1 (TC)	4	IO	PT21C	—	L17T_A0
A25	1 (TC)	4	IO	PT21B	—	L18C_A0
A24	1 (TC)	4	IO	PT21A	—	L18T_A0
B23	1 (TC)	4	IO	PT20D	—	L19C_A0
A23	1 (TC)	4	IO	PT20C	—	L19T_A0
N15	—	—	Vss	Vss	—	—
E17	1 (TC)	4	IO	PT20B	—	L20C_A0
E16	1 (TC)	4	IO	PT20A	—	L20T_A0
B22	1 (TC)	4	IO	PT19D	—	L21C_A0
B21	1 (TC)	4	IO	PT19C	VREF_1_04	L21T_A0
C18	1 (TC)	4	IO	PT19B	—	L22C_A0
C19	1 (TC)	4	IO	PT19A	—	L22T_A0
N20	—	—	Vss	Vss	—	—
A22	1 (TC)	5	IO	PT18D	PTCK1C	L23C_A0
A21	1 (TC)	5	IO	PT18C	PTCK1T	L23T_A0
N21	—	—	Vss	Vss	—	—
D17	1 (TC)	5	IO	PT18B	—	L24C_A0
D18	1 (TC)	5	IO	PT18A	—	L24T_A0
B20	1 (TC)	5	IO	PT17D	PTCK0C	L25C_A0
B19	1 (TC)	5	IO	PT17C	PTCK0T	L25T_A0
A20	1 (TC)	5	IO	PT17B	—	L26C_A0
A19	1 (TC)	5	IO	PT17A	—	L26T_A0
A18	1 (TC)	5	IO	PT16D	VREF_1_05	L27C_A0
B18	1 (TC)	5	IO	PT16C	—	L27T_A0
Y21	—	—	Vss	Vss	—	—
C17	1 (TC)	5	IO	PT16B	—	L28C_D0
D16	1 (TC)	5	IO	PT16A	—	L28T_D0
A17	1 (TC)	6	IO	PT15D	—	L29C_D0
B16	1 (TC)	6	IO	PT15C	—	L29T_D0
E15	1 (TC)	6	IO	PT15B	—	L30C_A0
E14	1 (TC)	6	IO	PT15A	—	L30T_A0
A16	1 (TC)	6	IO	PT14D	—	L31C_A0
A15	1 (TC)	6	IO	PT14C	VREF_1_06	L31T_A0
Y22	—	—	Vss	Vss	—	—
D14	1 (TC)	6	IO	PT14B	—	—
C16	0 (TL)	1	IO	PT13D	MPI_RTRY_N	L1C_A0
C15	0 (TL)	1	IO	PT13C	MPI_ACK_N	L1T_A0

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
U21	—	—	VDD15	VDD15	—	—
U22	—	—	VDD15	VDD15	—	—
V13	—	—	VDD15	VDD15	—	—
V14	—	—	VDD15	VDD15	—	—
V15	—	—	VDD15	VDD15	—	—
V20	—	—	VDD15	VDD15	—	—
V21	—	—	VDD15	VDD15	—	—
V22	—	—	VDD15	VDD15	—	—
W13	—	—	VDD15	VDD15	—	—
W14	—	—	VDD15	VDD15	—	—
W15	—	—	VDD15	VDD15	—	—
W20	—	—	VDD15	VDD15	—	—
W21	—	—	VDD15	VDD15	—	—
W22	—	—	VDD15	VDD15	—	—
Y16	—	—	VDD15	VDD15	—	—
Y17	—	—	VDD15	VDD15	—	—
Y18	—	—	VDD15	VDD15	—	—
Y19	—	—	VDD15	VDD15	—	—
T32	—	—	NC	NC	—	—
W32	—	—	NC	NC	—	—

Package Thermal Characteristics Summary

There are three thermal parameters that are in common use: Θ_{JA}, ψ_{JC}, and Θ_{JC}. It should be noted that all the parameters are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

Θ_{JA}

This is the thermal resistance from junction to ambient (theta-JA, R-theta, etc.):

$$\Theta_{JA} = \frac{T_J - T_A}{Q} \quad (1)$$

where T_J is the junction temperature, T_A, is the ambient air temperature, and Q is the chip power.

Experimentally, Θ_{JA} is determined when a special thermal test die is assembled into the package of interest, and the part is mounted on the thermal test board. The diodes on the test chip are separately calibrated in an oven. The package/board is placed either in a JEDEC natural convection box or in the wind tunnel, the latter for forced convection measurements. A controlled amount of power (Q) is dissipated in the test chip's heater resistor, the chip's temperature (T_J) is determined by the forward drop on the diodes, and the ambient temperature (T_A) is noted. Note that Θ_{JA} is expressed in units of °C/W.

ψ_{JC}

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance and it is defined by:

$$\psi_{JC} = \frac{T_J - T_C}{Q} \quad (2)$$