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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

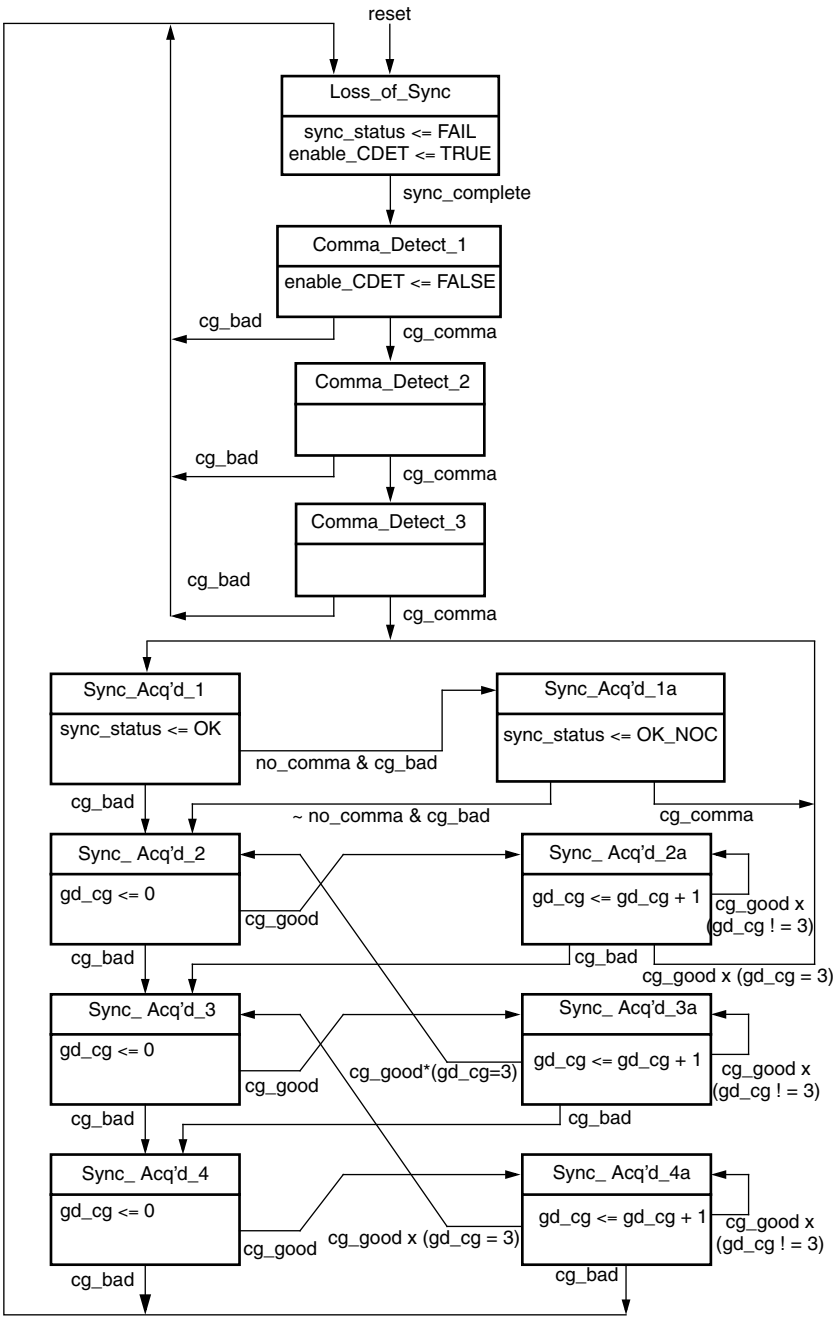
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	10368
Total RAM Bits	113664
Number of I/O	372
Number of Gates	643000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort82g5-3fn680c

Table 5. XAUI Link Synchronization State Diagram Notation – Variables

Variable	Description
sync_status	FAIL: Lane is not synchronized (correct 10-bit alignment has not been established). OK: Lane is synchronized. OK_NOC: Lane is synchronized but a comma character has not been detected in the past 200 code groups.
enable_CDET	TRUE: Align subsequent 10-bit words to the boundary indicated by the next received comma. FALSE: Maintain current 10-bit alignment.
gd_cg	Current number of consecutive cg_good indications.

Figure 10. XAUI Link Synchronization State Diagram



- FMPU_SYNMODE_B = 11111111 (Register Location 30911)

To enable/disable multi-channel alignment of individual channels within a multi-channel alignment group:

- FMPU_STR_EN_xx = 1 enabled
- FMPU_STR_EN_xx = 0 disabled
- (Register Location 30810 and 30910, where xx is one of AC, AD, BC or BD.)

To resynchronize a multichannel alignment group set the following bit to zero, and then set it to one.

- FMPU_RESYNC4 for four channels, AC, AD, BC and BD. (Register Location 30A02, bit 2)
- FMPU_RESYNC2A for dual channels, AC and AD. (Register Location 30820, bit 5)
- FMPU_RESYNC2B for block channels, BC and BD. (Register Location 30920, bit 5)

To resynchronize an independent channel (resetting the write and the read pointer of the FIFO) set the following bit to zero, and then set it to one.

FMPU_RESYNC1_xx (Register Locations 30820 and 30920, bits 2 and 3, where xx is one of AC, AD, BC or BD).

ORT82G5 Configuration

Register settings for multi-channel alignment are shown in Table 7.

Table 7. Multi-channel Alignment Modes

Register Bits FMPU_SYNMODE_xx[0:1]	Mode
00	No multi-channel alignment.
10	Twin channel alignment.
01	Quad channel alignment.
11	Eight channel alignment.

Note: Where xx is one of A[A:D] and B[A:D].

To align all eight channels:

- FMPU_SYNMODE_A[A:D] = 11
- FMPU_SYNMODE_B[A:D] = 11

To align all four channels in SERDES A:

- FMPU_SYNMODE_A[A:D] = 01

To align two channels in SERDES A:

- FMPU_SYNMODE_A[A:B] = 10 for channel AA and AB
- FMPU_SYNMODE_A[C:D] = 10 for channel AC and AD

A similar alignment can be defined for SERDES B.

To enable/disable synchronization signal of individual channel within a multi-channel alignment group:

- FMPU_STR_EN_xx = 1 enabled
- FMPU_STR_EN_xx = 0 disabled

where xx is one of A[A:D] and B[A:D].

To resynchronize a multi-channel alignment group set the following bit to zero, and then set it to one:

- FMPU_RESYNC8 for eight channel A[A:D] and B[A:D]
- FMPU_RESYNC4A for quad channel A[A:D]
- FMPU_RESYNC2A1 for twin channel A[A:B]

grammed to a value > 0. (Default value is 0.) Change the value to 0 and check the OVFL bit again.

If OOS and OVFL are 1, then rewrite a 1 to the appropriate resync registers. The resync operation requires a rising edge. Two writes are required to the resync bits: write a 0 and then write a 1.

ORT82G5 Alignment Sequence

1. Follow steps 1 and 2 in the start-up sequence described in a later section.

2. Initiate a SERDES software reset by setting the SWRST bit to 1 and then to 0. Note that any changes to the SERDES configuration bits should be followed by a software reset.

3. Wait for 3 ms. REFCLK should be toggling by this time. During this time, configure the following registers.

Set the following bits in registers 30820, 30920

- XAUI_MODE_xx-set to 1 for XAUI mode or keep the default value of 0 if the Fibre Channel state machine was selected.
- Enable channel alignment by setting FMPU_SYNMODE bits in registers 30811, 30911.
- FMPU_SYNMODE_xx. Set to appropriate values for 2, 4, or 8 alignment based on Table 7.
- Set RCLKSEL[A:B] and TCKSEL[A:B] bits in registers 30A00.
- RCKSEL[A:B] – Choose clock source for 78 MHz RCK78x (Table 18).
- TCKSEL[A:B] – Choose clock source for 78 MHz TCK78x (Table 17). Send data on serial links.

Monitor the following status/alarm bits:

- Monitor the following alarm bits in registers 30000, 30010, 30020, 30030, 30100, 30110, 30120, 30130.
- LKI-PLL_xx lock indicator. A 1 indicates that PLL has achieved lock.

Monitor the following status bits in registers 30804, 30904:

- XAUISTAT_xx - In XAUI mode, they should be 10.

Monitor the following status bits in registers 30805, 30905

- DEMUXWAS_xx-They should be 1 indicating word alignment is achieved.
- CH248_SYNCxx-They should be 1 indicating channel alignment. This is cleared by resync.

4. Write a 1 to the appropriate resync registers 30820, 30920 or 30A02. Note that this assumes that the previous value of the resync bits are 0. The resync operation requires a rising edge. Two writes are required to the resync bits: write a 0 and then write a 1. It is highly recommended to precede a resync with a word alignment, especially in situations where a disturbance in the receive SERDES path can cause misalignment of data and OOS indications without bringing the FC/XAUI state machine to a loss of synch state. A word alignment is achieved by writing a 0 and then a 1 to the appropriate DOWDALIGNxx bits in registers 30810/30910.

Check out-of-sync and FIFO overflow status in registers 30814 (Bank A).

- SYNC4_A_OOS, SYNC4_A_OVFL-by 4 alignment.
- SYNC2_A2_OOS, SYNC_A2_OVFL or SYNC2_A1_OOS, SYNC2_A1_OVFL-by 2 alignment.
- Check out-of-sync status in registers 30914 (Bank B).
- SYNC4_B_OOS, SYNC4_B_OVFL-by 4 alignment.
- SYNC_B2_OOS, SYNC2_B2_OVFL or SYNC2_B1_OOS, SYNC_B1_OVFL-by 2 alignment.
- Check out-of-sync status in register 30A03
- SYNC8_OOS, SYNC8_OVFL-by 8 alignment.
- If out-of-sync bit is 1, then rewrite a 1 to the appropriate resync registers and monitor the OOS bit again. If Out of Synchronization (OOS) bit is 0 but OVFL bit is 1, then check if the RX_FIFO_MIN value has been programmed to a value > 0. (Default value is 0.) Change the value to 0 and check the OVFL bit again. If OOS and OVFL are 1, then rewrite a 1 to the appropriate resync registers. The resync operation requires a rising edge. Two writes are required to the resync bits: write a 0 and then write a 1.

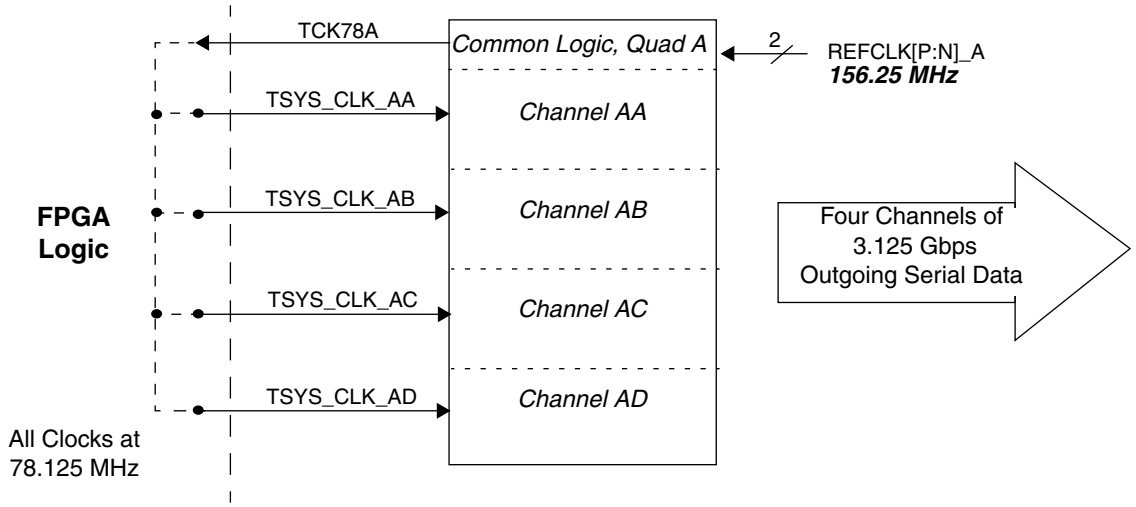
Table 17. TCK78[A:B] Source Selection

TCKSEL0	TCKSEL1	Clock Source
0	0	Channel A
1	0	Channel B
0	1	Channel C
1	1	Channel D

Recommended Transmit Clock Distribution for the ORT82G5

As an example of the recommended clock distribution approach, TSYS_CLK_A[A:D] can be sourced by TCK78A as shown in Figure 25 if the transmit line rate are common for all four channels in a quad. Similar clocking would be used for Quad B.

Figure 25. Transmit Clocking for a Single Block (Similar Connections Would Be Used for Block B)



If the transmit line rate is mixed between half and full rate among the channels, then the scheme shown in Figure 26 can be used. The figure shows TSYS_CLK_AA and TSYS_CLK_AB being sourced by TCK78A and TSYS_CLK_AC and TSYS_CLK_AD being sourced by TCK78A/2 (the division is done in FPGA logic). Similar clocking would be used for Quad B.

Start Up Sequence for the ORT42G5

The following sequence is required by the ORT42G5 device. For information required for simulation that may be different than this sequence, see the ORT42G5 Design Kit.

1. Initiate a hardware reset by making PASB_RESETN low. Keep this low during FPGA configuration of the device. The device will be ready for operation 3 ms after the low to high transition of PASB_RESETN.

2. At startup, the legacy SERDES channel logic must be powered down and removed from any multi-channel alignment groups:

   - Setting bit 1 to one in registers at locations 30002, 30012, 30102, 30112, 30003, 30013, 30103 and 30113 powers down the legacy logic. (Note that the reset value for these bits is 0.)
   - Setting bits 4 and 5 to zero (reset condition) in the register at locations 30810 and 30910 removes the legacy logic from any alignment group.

3. Configure the following SERDES internal and external registers. Note that after device initialization, all alarm and status bits should be read once to clear them. A subsequent read will provide the valid state.

   Set the following bits in register 30800:
   – Bits LCKREFN_[AC and AD] to 1, which implies lock to data.
   – Bits ENBYSYNC_[AC and AD] to 1 which enables dynamic alignment to comma.

   Set the following bits in register 30801:
   – Bits LOOPENB_[AC and AD] to 1 if high-speed serial loopback is desired.

   Set the following bits in register 30900:
   – Bits LCKREFN_[BC and BD] to 1 which implies lock to data.
   – Bits ENBYSYNC_[BC and BD] to 1 which enables dynamic alignment to comma.

   Set the following bits in register 30901:
   – Bits LOOPENB_[BC and BD] to 1 if high-speed serial loopback is desired.

   Set the following bits in registers 30022, 30032, 30122, 30132:
   – TXHR set to 1 if TX half-rate is desired.
   – 8b10bT set to 1 if 8b10b encoding is desired.

   Set the following bits in registers 30023, 30033, 30123, 30133:
   – RXHR Set to 1 if RX half-rate is desired.
   – 8b10bR set to 1 if 8b10b decoding is desired.
   – LINKSM set to 1 if the Fibre Channel state machine is desired.

   Assert GSWRST bit by writing 1's to both SERDES blocks. Deassert GSWRST bit by writing 0's to both SERDES blocks. Wait 3 ms. If higher speed serial loopback has been selected, the receive PLLs will use this time to lock to the new serial data.

   Monitor the following alarm bits in registers 30020, 30030, 30120, 30130:
   – LKI, PLL lock indicator. 1 indicates that PLL has achieved lock.

4. If 8b/10b mode is enabled, enable link synchronization by periodically sending the following sequence three times:
   – K28.5 D21.4 D21.5 D21.5 or any other idle ordered set (starting with a /comma/) in FC mode.
   – /comma/ characters for the XAUI state machine and /A/ characters for word and channel alignment in XAUI mode.

Test Modes

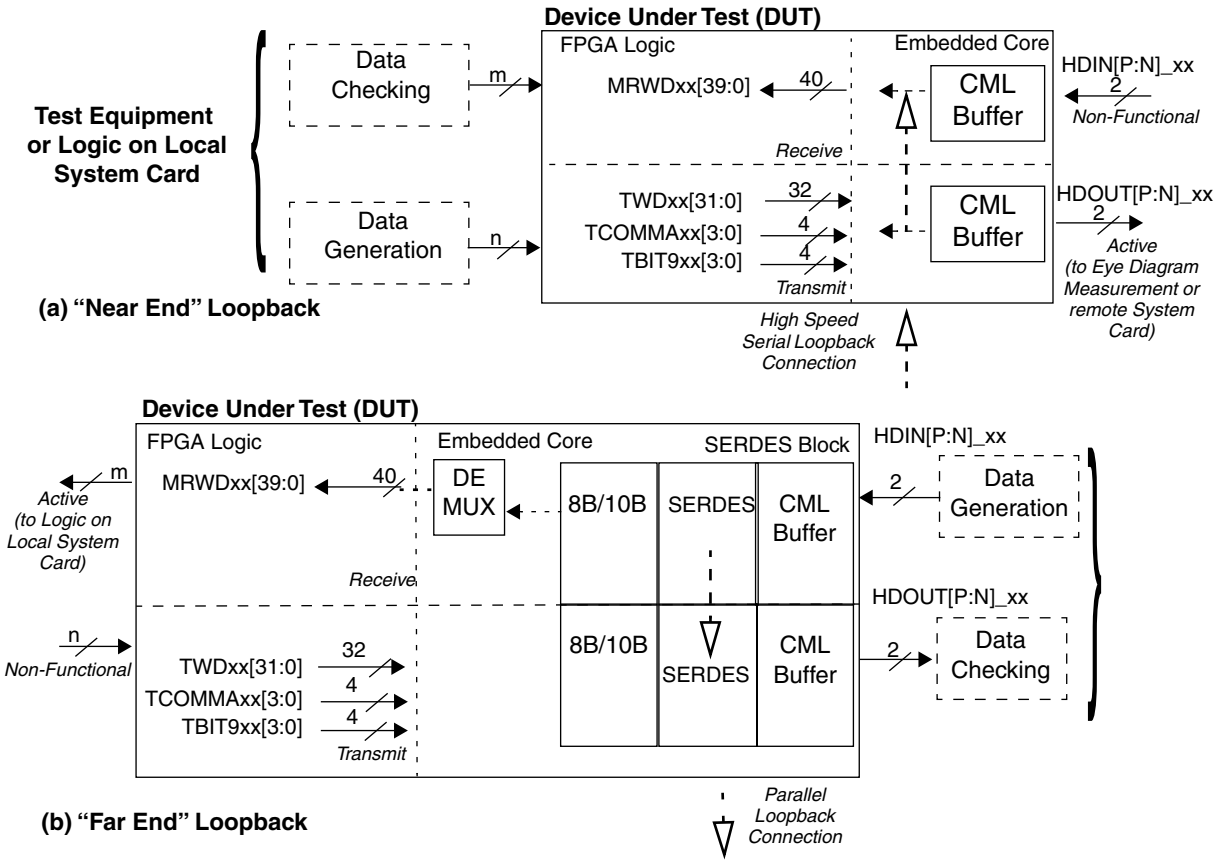
In addition to the operational logic described in the preceding sections, the Embedded Core contains logic to support various test modes - both for device validation and evaluation and for operating system level tests. The following sections discuss two of the test support logic blocks, supporting various loopback modes and SERDES characterization.

Loopback Testing

Loopback testing is performed by looping back (either internal to the Embedded Core, by configuring the FPGA logic or by external connections) transmitted data to the corresponding receiver inputs, or received data to the transmitter output. The loopback path may be either serial or parallel.

In general, loopback tests can be classified as “near end” or “far end.” In “near end” loopback (Figure 32(a)), data is generated and checked locally, i.e. by logic on, or connection of, test equipment to the same card as the FPSC. In “far end” loopback (Figure 32(b)), the generating and checking functions are performed remotely, either by test equipment or a remote system card.

Figure 32. “Near End” vs. “Far End” Loopback



The loopback mode can also be characterized by the physical location of the loopback connection. There are three possible loopback modes supported by the Embedded Core logic:

- High-speed serial loopback at the CML buffer interface (near end)
- Parallel loopback at the SERDES boundary (far end)

Table 24. Decoding of SCHAR_CHAN

SCHAR_CHAN0	SCHAR_CHAN1	Channel
0	0	BA
1	0	BB
0	1	BC
1	1	BD

The receive characterization test mode is entered when SCHAR_ENA=1 and SCHAR_TXSEL=0, In this mode, one of the channels of SERDES outputs is observed at chip ports as shown in Table 25. The channel that is observed is also based on the decoding of SCHAR_CHAN as shown in Table 25.

Table 25. SERDES Receive Characterization Mode

SERDES Output	Chip Port
BYTSYNCBx	PSCHAR_BYTSYNC
WDSYNCBx	PSCHAR_WDSYNC
CVOBx	PSCHAR_CV
LDOUTBx[9:0]	PSCHAR_LDIO[9:0]
RBC0Bx	PSCHAR_CKIO0
RBC1Bx	PSCHAR_CKIO1

Embedded Core Block RAM

There are two independent memory blocks (labeled A and B) built-into the Embedded ASIC Core (EAC). Each memory block has a capacity of 4K words by 36 bits. These two memory blocks (also called “slices”) are in addition to the block RAMs found in the FPGA portion of the ORT82G5.

Although the memory blocks/slices are in the EAC part of the chip, they do not interact with the rest of the EAC circuits, but are standalone memories designed specifically to increase RAM capacity in the ORT82G5 chip. They can be used by logic implemented in the FPGA portion of the FPSC. Figure 34 represents one of the two available memory slices built into the EAC. The index “x” refers to the memory slice (x=A for slice A, x=B for slice B). Each memory slice is organized into two sections, which are also labeled as A and B. In Figure 34, SDRAM A is one section of slice x, and SDRAM B is another section of slice x. Data can be written to both sections of a slice independently. However, a read access can access only one of sections A or B at any given time (CSR_x=0 selects section A, CSR_x=1 selects section B).

The 36 bits written to or read from the memory slice are composed of 32 bits of data (bits 31:24, 23:16, 15:8, 7:0), and 4 bits of parity (bits 35,34,33,32). The core performs no parity checking functions. The data read from the memory is registered so that it works as a pipelined synchronous memory block.

For illustration purposes, assuming that the memory slice in Figure 34 is slice A (x=A), then certain signals apply to both sections of slice A. These include D_A[35:0], CKW_A, AW_A[10:0], BYTEWN_A[3:0], Q_A[35:0], CKR_A, CSR_A, and AR_A[10:0]. The BYTEWN_A[3:0] are byte and parity write enable bits for each byte and parity bit of data being written.

BYTEWN_A[3] is associated with D_A[35,31:24].
BYTEWN_A[2] is associated with D_A[34,23:16].
BYTEWN_A[1] is associated with D_A[33,15:8].
BYTEWN_A[0] is associated with D_A[32,7:0].

The signals that are unique to each section of slice A are:

CSWA_A --enables writing to section A of slice A
CSWB_A -- enables writing to section B of slice A

Table 28. ORT42G5 Memory Map (Continued)

(0x) Absolute Address	Bit	Name	Reset Value (0x)	Description
Common Control Registers (Read/Write)				
30A00	[0:1]	TCKSELA	00	Transmit Clock Select. Controls source of 78 MHz TCK78 for SERDES quad A 01 = Channel AC 11 = Channel AD
	[2:3]	RCKSELA		Receive Clock Select. Controls source of 78 MHz RCK78 for SERDES quad A 01 = Channel AC 11 = Channel AD
	[4:5]	TCKSELB		Transmit Clock Select. Controls source of 78 MHz TCK78 for SERDES quad B 01 = Channel BC 11 = Channel BD
	[6:7]	RCKSELB		Receive Clock Select. Controls source of 78 MHz RCK78 for SERDES quad B 01 = Channel BC 11 = Channel BD
30A01	[0:4]	—	00	Reserved for future use
	[5:7]	RX_FIFO_MIN		LSb's for the threshold for low address in RX_FIFOs. RX_FIFO_MIN, Bit 5 is LSb.*
30A02	[0:1]	RX_FIFO_MIN	00	MSb's for the threshold for low address in RX_FIFOs. RX_FIFO_MIN, Bit 1 is MSb.*
	[2]	FMPU_RESYNC4		Resynchronize a four-channel group. When FPMPU_RESYNC4 transitions from 0 to 1, the entire four-channel group is resynchronized. FMPU_RESYNC4 = 0 on device reset
	[3:7]	—		Reserved for future use
Common Status Registers				
30A03	[0]	SYNC4_OVFL	00	Read-Only Multi-Channel Overflow Status. When SYNC4_OVFL=1, 4-channel synchronization FIFO overflow has occurred. SYNC4_OVFL=0 on device reset.
	[1]	SYNC4_OOS		Read-Only Multi-Channel Out-Of-Sync Status. When SYNC4_OOS=1, 4-channel synchronization has failed. SYNC4_OOS=0 on device reset.
	[2:7]	—		Reserved for future use.

* Useful values for RX_FIFO_MIN [0:4] are 0 to 17(decimal)

External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 38 specifies reference clock requirements, over the full range of operating conditions. The designer is encourage to read TN1040, *SERDES Reference Clock,* which discusses various aspects of this system element and its interconnection.

Table 38. Reference Clock Specifications (REFCLKP and REFCLKN)

Parameter	Min.	Typ.	Max.	Units
Frequency Range	60	—	185	MHz
Frequency Tolerance[1]	-350	—	350	ppm
Duty Cycle (Measured at 50% Amplitude Point)	40	50	60	%
Rise Time	—	500	1000	ps
Fall Time	—	500	1000	ps
P–N Input Skew	—	—	75	ps
Differential Amplitude	500	800	2 x V_{DDIB}	mV_{p-p}
Common Mode Level	$V_{single-ended/2}$	0.75	$V_{DD15} – (V_{single-ended/2})$	V
Single-Ended Amplitude	250	400	V_{DDIB}	mV_{p-p}
Input Capacitance (at REFCLKP)	—	—	5	pF
Input Capacitance (at REFCLKN)	—	—	5	pF

1. This specification indicates the capability of the high speed receiver CDR PLL to acquire lock when the reference clock frequency and incoming data rate are not synchronized.

Embedded Core Timing Characteristics

Table 39 summarizes the end-to-end latencies through the embedded core for the various modes. All latencies are given in clock cycles for system clocks at half the REFCLK_[A:B] frequency. For a REFCLK_[A:B] of 156.25 MHz, a system clock cycle is 6.4 ns.

Table 39. Signal Latencies, Embedded Core

Operating Mode	Signal Latency (max.)
Transmit Path	5 clock cycles
Receive Path	
Multi-Channel Alignment Bypassed[1]	4.5 clock cycles
With Multi-Channel Alignment[1]	13.5-22.5 clock cycles

1. With multi-channel alignment, the latency is largest when the skew between channels is at the maximum that can be correctly compensated for (18 clock cycles). The latency specified in the table is for data from the channel received first.

Pin Descriptions

This section describes the pins found on the Series 4 FPGAs. Any pin not described in this table is a user-programmable I/O. During configuration, the user-programmable I/Os are 3-stated with an internal pull-up resistor. If any pin is not used (or not bonded to a package pin), it is also 3-stated with an internal pull-up resistor after configuration. The pin descriptions in Table and throughout this data sheet show active-low signals with an overscore. The package pinout tables that follow, show this as a signal ending with _N. For example $\overline{\text{LDC}}$ and LDC_N are equivalent.

Table 40. Pin Descriptions

Symbol	I/O	Description
Dedicated Pins		
VDD33	—	3.3V positive power supply. This power supply is used for 3.3V configuration RAMs and internal PLLs. When using PLLs, this power supply should be well isolated from all other power supplies on the board for proper operation.
VDD15	—	1.5V positive power supply for internal logic.
VDDIO	—	Positive power supply used by I/O banks.
VSS	—	Ground.
PTEMP	I	Temperature sensing diode pin. Dedicated input.
$\overline{\text{RESET}}$	I	During configuration, $\overline{\text{RESET}}$ forces the restart of configuration and a pull-up is enabled. After configuration, $\overline{\text{RESET}}$ can be used as a general FPGA input or as a direct input, which causes all PLC latches/FFs to be asynchronously set/reset.
CCLK	O	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in.
	I	In the slave or readback after configuration, CCLK is input synchronous with the data on DIN or D[7:0]. CCLK is an output for daisy-chain operation when the lead device is in master, peripheral, or system bus modes.
DONE	I	As an input, a low level on DONE delays FPGA start-up after configuration.[1]
	O	As an active-high, open-drain output, a high level on this signal indicates that configuration is complete. DONE has an optional pull-up resistor.
PRGRM	I	$\overline{\text{PRGRM}}$ is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up.
RD_CFG	I	This pin must be held high during device initialization until the $\overline{\text{INIT}}$ pin goes high. This pin always has an active pull-up. During configuration, $\overline{\text{RD\_CFG}}$ is an active-low input that activates the TS_ALL function and 3-states all of the I/O. After configuration, $\overline{\text{RD\_CFG}}$ can be selected (via a bit stream option) to activate the TS_ALL function as described above, or, if readback is enabled via a bit stream option, a high-to-low transition on $\overline{\text{RD\_CFG}}$ will initiate readback of the configuration data, including PFU output states, starting with frame address 0.
RD_DATA/TDO	O	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary-scan, TDO is test data out.
$\overline{\text{CFG\_IRQ}}$/MPI_IRQ	O	During JTAG, slave, master, and asynchronous peripheral configuration assertion on this $\overline{\text{CFG\_IRQ}}$ (active-low) indicates an error or errors for block RAM or FPSC initialization. MPI active-low interrupt request output, when the MPI is used.
LVDS_R	—	Reference resistor connection for controlled impedance termination of Series 4 FPGA LVDS inputs.
Special-Purpose Pins		
M[3:0]	I	During powerup and initialization, M0—M3 are used to select the configuration mode with their values latched on the rising edge of $\overline{\text{INIT}}$. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O.[1]
PLL_CK[0:7][TC]	I	Semi-dedicated PLL clock pins. During configuration they are 3-stated with a pull up.
	I/O	These pins are user-programmable I/O pins if not used by PLLs after configuration.
P[TBLR]CLK[1:0][TC]	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.
	I/O	After configuration these pins are user programmable I/O, if not used for clock inputs.

Table 40. Pin Descriptions (Continued)

Symbol	I/O	Description
TDI, TCK, TMS	I	If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O if boundary scan is not used.[1]
RDY/$\overline{\text{BUSY}}$/RCLK	O	During configuration in asynchronous peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
	I/O	After configuration this pin is a user-programmable I/O pin.[1]
HDC	O	High During Configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
LDC	O	$\overline{\text{Low During Configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.[1]
INIT	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration. After configuration, this pin is a user-programmable I/O pin.[1]
$\overline{\text{CS0}}$, CS1	I	$\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, if MPI is not used, these pins are user-programmable I/O pins.[1]
$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$	I	$\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D[7:3] into a status output. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the MPI data transfer strobe. As a status indication, a high indicates ready, and a low indicates busy.
$\overline{\text{WR}}$/MPI_RW	I	$\overline{\text{WR}}$ is used in asynchronous peripheral mode. A low on $\overline{\text{WR}}$ transfers data on D[7:0] to the FPGA. In MPI mode, a high on MPI_RW allows a read from the data bus, while a low causes a write transfer to the FPGA.
	I/O	After configuration, if the MPI is not used, $\overline{\text{WR}}$/MPI_RW is a user-programmable I/O pin.[1]
PPC_A[14:31]	I	During MPI mode the PPC_A[14:31] are used as the address bus driven by the PowerPC bus master utilizing the least-significant bits of the PowerPC 32-bit address.
MPI_BURST	I	$\overline{\text{MPI\_BURST}}$ is driven low to indicate a burst transfer is in progress in MPI mode. Driven high indicates that the current transfer is not a burst.
MPI_BDIP	I	$\overline{\text{MPI\_BDIP}}$ is driven by the PowerPC processor in MPI mode. Assertion of this pin indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.
MPI_TSZ[0:1]	I	MPI_TSZ[0:1] signals are driven by the bus master in MPI mode to indicate the data transfer size for the transaction. Set 01 for byte, 10 for half-word, and 00 for word.
A[21:0]	O	During master parallel mode A[21:0] address the configuration EPROMs up to 4M bytes.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]
MPI_ACK	O	In MPI mode this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.[1]

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
G9	-	-	VSS	VSS	-	-
L3	7 (CL)	5	IO	PL21D	A10/PPC_A24	L10C
L4	7 (CL)	5	IO	PL21C	A9/PPC_A23	L10T
L5	7 (CL)	5	IO	PL22D	A8/PPC_A22	-
F10	-	-	VDD15	VDD15	-	-
G10	-	-	VSS	VSS	-	-
M3	7 (CL)	6	IO	PL24D	PLCK1C	L11C
M4	7 (CL)	6	IO	PL24C	PLCK1T	L11T
N4	7 (CL)	6	IO	PL25C	A7/PPC_A21	-
M2	7 (CL)	6	IO	PL26D	A6/PPC_A20	L12C
M1	7 (CL)	6	IO	PL26C	A5/PPC_A19	L12T
N3	7 (CL)	7	IO	PL27D	WR_N/MPI_RW	-
F11	-	-	VDD15	VDD15	-	-
N5	7 (CL)	8	IO	PL28D	A4/PPC_A18	-
M5	7 (CL)	-	VDDIO7	VDDIO7	-	-
N2	7 (CL)	8	IO	PL29D	A3/PPC_A17	L13C
N1	7 (CL)	8	IO	PL29C	A2/PPC_A16	L13T
G11	-	-	VSS	VSS	-	-
P2	7 (CL)	8	IO	PL30D	A1/PPC_A15	L14C
P1	7 (CL)	8	IO	PL30C	A0/PPC_A14	L14T
F12	-	-	VDD15	VDD15	-	-
P3	7 (CL)	8	IO	PL31D	DP0	L15C
P4	7 (CL)	8	IO	PL31C	DP1	L15T
R4	6 (BL)	1	IO	PL32D	D8	L16C
R3	6 (BL)	1	IO	PL32C	VREF_6_01	L16T
R2	6 (BL)	1	IO	PL33D	D9	L17C
R1	6 (BL)	1	IO	PL33C	D10	L17T
G12	-	-	VSS	VSS	-	-
T3	6 (BL)	2	IO	PL34D	-	-
P5	6 (BL)	-	VDDIO6	VDDIO6	-	-
T2	6 (BL)	2	IO	PL34B	-	L18C
T1	6 (BL)	2	IO	PL34A	-	L18T
U1	6 (BL)	3	IO	PL35B	D11	L19C
U2	6 (BL)	3	IO	PL35A	D12	L19T
R5	6 (BL)	-	VDDIO6	VDDIO6	-	-
V1	6 (BL)	3	IO	PL36B	VREF_6_03	L20C
V2	6 (BL)	3	IO	PL36A	D13	L20T
G13	-	-	VSS	VSS	-	-
W2	6 (BL)	4	IO	PL37B	-	L21C
W1	6 (BL)	4	IO	PL37A	VREF_6_04	L21T
Y1	6 (BL)	4	IO	PL39D	PLL_CK7C/HPPLL	L22C
Y2	6 (BL)	4	IO	PL39C	PLL_CK7T/HPPLL	L22T
U3	-	-	I	PTEMP	PTEMP	-
F13	-	-	VDD15	VDD15	-	-

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
V9	5 (BC)	1	IO	PB17A	-	-
W9	5 (BC)	1	IO	PB17C	-	L35T
Y9	5 (BC)	1	IO	PB17D	-	L35C
U9	5 (BC)	1	IO	PB18A	-	-
AA9	5 (BC)	1	IO	PB18C	VREF_5_01	L36T
AB9	5 (BC)	1	IO	PB18D	-	L36C
G16	-	-	VDD15	VDD15	-	-
H13	-	-	VSS	VSS	-	-
AB10	5 (BC)	2	IO	PB19A	-	L37T
AA10	5 (BC)	2	IO	PB19B	-	L37C
W10	5 (BC)	2	IO	PB19C	PBCK0T	L38T
Y10	5 (BC)	2	IO	PB19D	PBCK0C	L38C
V10	5 (BC)	2	IO	PB20A	-	-
U13	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB11	5 (BC)	2	IO	PB20C	VREF_5_02	L39T
AA11	5 (BC)	2	IO	PB20D	-	L39C
U10	5 (BC)	2	IO	PB21A	-	-
H6	-	-	VDD15	VDD15	-	-
Y11	5 (BC)	3	IO	PB21C	-	L40T
W11	5 (BC)	3	IO	PB21D	VREF_5_03	L40C
U11	5 (BC)	3	IO	PB22A	-	-
J7	-	-	VSS	VSS	-	-
AB12	5 (BC)	3	IO	PB22C	-	L41T
AA12	5 (BC)	3	IO	PB22D	-	L41C
U12	5 (BC)	3	IO	PB23A	-	-
Y12	5 (BC)	3	IO	PB23C	PBCK1T	L42T
W12	5 (BC)	3	IO	PB23D	PBCK1C	L42C
V11	5 (BC)	3	IO	PB24A	-	-
J8	-	-	VSS	VSS	-	-
AB13	5 (BC)	4	IO	PB24C	-	L43T
AA13	5 (BC)	4	IO	PB24D	-	L43C
V12	5 (BC)	4	IO	PB25A	-	-
U14	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB14	5 (BC)	4	IO	PB25C	-	L44T
AA14	5 (BC)	4	IO	PB25D	VREF_5_04	L44C
J9	-	-	VSS	VSS	-	-
Y13	5 (BC)	5	IO	PB26C	-	L45T
W13	5 (BC)	5	IO	PB26D	VREF_5_05	L45C
U15	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB15	5 (BC)	5	IO	PB27C	-	L46T
AA15	5 (BC)	5	IO	PB27D	-	L46C
AB16	5 (BC)	6	IO	PB28C	-	L47T
AA16	5 (BC)	6	IO	PB28D	VREF_5_06	L47C
H14	-	-	VDD15	VDD15	-	-

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
Y14	5 (BC)	6	IO	PB29C	-	L48T
W14	5 (BC)	6	IO	PB29D	-	L48C
J10	-	-	VSS	VSS	-	-
AB17	5 (BC)	7	IO	PB30C	-	L49T
AA17	5 (BC)	7	IO	PB30D	-	L49C
U16	5 (BC)	-	VDDIO5	VDDIO5	-	-
Y15	5 (BC)	7	IO	PB31C	VREF_5_07	L50T
W15	5 (BC)	7	IO	PB31D	-	L50C
V13	5 (BC)	-	VDDIO5	VDDIO5	-	-
AB18	5 (BC)	8	IO	PB33C	-	L51T
AA18	5 (BC)	8	IO	PB33D	VREF_5_08	L51C
J11	-	-	VSS	VSS	-	-
V14	5 (BC)	8	IO	PB34D	-	-
V16	5 (BC)	9	IO	PB35B	-	-
Y16	5 (BC)	9	IO	PB36C	-	L52T
W16	5 (BC)	9	IO	PB36D	-	L52C
V15	-	-	VDD33	VDD33	-	-
J12	-	-	VSS	VSS	-	-
H15	-	-	VDD15	VDD15	-	-
J13	-	-	VSS	VSS	-	-
J6	-	-	VDD15	VDD15	-	-
J14	-	-	VSS	VSS	-	-
Y17	-	-	VDD33	VDD33	-	-
K8	-	-	VSS	VSS	-	-
J15	-	-	VDD15	VDD15	-	-
K7	-	-	VDD15	VDD15	-	-
Y18	-	-	VDD33	VDD33	-	-
K9	-	-	VSS	VSS	-	-
W21	-	-	VSS	VSS	-	-
W22	-	-	VDDGB_B	VDDGB_B	-	-
F18	-	-	VDD_ANA	VDD_ANA	-	-
V21	-	-	O	REXT_B	-	-
V22	-	-	O	REXTN_B	-	-
U21	-	-	I	REFCLKN_B	-	HSN_1
U22	-	-	I	REFCLKP_B	-	HSP_1
E20	-	-	VSS	VSS	-	-
G17	-	-	VDD_ANA	VDD_ANA	-	-
G18	-	-	VDD_ANA	VDD_ANA	-	-
J16	-	-	VDD_ANA	VDD_ANA	-	-
J17	-	-	VDD_ANA	VDD_ANA	-	-
T20	-	-	VDDIB	VDDIB_BC	-	-
J18	-	-	VDD_ANA	VDD_ANA	-	-
T21	-	-	I	HDINN_BC	-	HSN_2
F19	-	-	VSS	VSS	-	-

Table 44. ORT42G5 484-pin PBGAM (fpBGA) Pinout (Continued)

484-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	484-PBGAM
N19	-	-	VDD_ANA	VDD_ANA	-	-
M19	-	-	VSS	VSS	-	-
P16	-	-	VDD_ANA	VDD_ANA	-	-
H21	-	-	I	HDINP_AC	-	HSP_9
R16	-	-	VSS	VSS	-	-
H22	-	-	I	HDINN_AC	-	HSN_9
P17	-	-	VDD_ANA	VDD_ANA	-	-
G20	-	-	VDDIB	VDDIB_AC	-	-
P18	-	-	VDD_ANA	VDD_ANA	-	-
P19	-	-	VDD_ANA	VDD_ANA	-	-
T17	-	-	VDD_ANA	VDD_ANA	-	-
T18	-	-	VDD_ANA	VDD_ANA	-	-
R17	-	-	VSS	VSS	-	-
G21	-	-	I	REFCLKP_A	-	HSP_10
G22	-	-	I	REFCLKN_A	-	HSN_10
F21	-	-	O	REXTN_A	-	-
F22	-	-	O	REXT_A	-	-
U18	-	-	VDD_ANA	VDD_ANA	-	-
E21	-	-	VDDGB_A	VDDGB_A	-	-
E22	-	-	VSS	VSS	-	-
D21	-	-	O	PSYS_RSSIG_ALL	-	-
D22	-	-	I	PSYS_DOBISTN	-	-
D20	-	-	VDD33	VDD33	-	-
K15	-	-	VDD15	VDD15	-	-
K10	-	-	VSS	VSS	-	-
L7	-	-	VDD15	VDD15	-	-
D19	-	-	I	PBIST_TEST_ENN	-	-
D18	-	-	I	PLOOP_TEST_ENN	-	-
L15	-	-	VDD15	VDD15	-	-
E17	-	-	I	PASB_PDN	-	-
K11	-	-	VSS	VSS	-	-
D17	-	-	VDD33	VDD33	-	-
M7	-	-	VDD15	VDD15	-	-
C21	-	-	I	PASB_RESETN	-	-
C22	-	-	I	PASB_TRISTN	-	-
K12	-	-	VSS	VSS	-	-
E16	-	-	I	PASB_TESTCLK	-	-
M15	-	-	VDD15	VDD15	-	-
C17	-	-	VDD33	VDD33	-	-
D16	1 (TC)	7	IO	PT36D	-	-
C16	1 (TC)	7	IO	PT36B	-	-
F14	1 (TC)	7	IO	PT35D	-	-
F15	1 (TC)	7	IO	PT35B	-	-
E14	1 (TC)	7	IO	PT34D	VREF_1_07	-

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AM4	6 (BL)	5	IO	PB2A	DP2	L13T_D0
AL5	6 (BL)	5	IO	PB2B	—	L13C_D0
AN7	6 (BL)	—	VDDIO6	VDDIO6	—	—
AP3	6 (BL)	5	IO	PB2C	PLL_CK6T/PPLL	L14T_A0
AP4	6 (BL)	5	IO	PB2D	PLL_CK6C/PPLL	L14C_A0
AN4	6 (BL)	5	IO	PB3B	—	—
U16	—	—	VSS	VSS	—	—
AK6	6 (BL)	5	IO	PB3C	—	L15T_A0
AK7	6 (BL)	5	IO	PB3D	—	L15C_A0
AL6	6 (BL)	5	IO	PB4A	VREF_6_05	L16T_A0
AM6	6 (BL)	5	IO	PB4B	DP3	L16C_A0
AP1	6 (BL)	—	VDDIO6	VDDIO6	—	—
AN5	6 (BL)	6	IO	PB4C	—	L17T_A0
AP5	6 (BL)	6	IO	PB4D	—	L17C_A0
AK8	6 (BL)	6	IO	PB5B	—	—
U17	—	—	VSS	VSS	—	—
AP6	6 (BL)	6	IO	PB5C	VREF_6_06	L18T_D0
AP7	6 (BL)	6	IO	PB5D	D14	L18C_D0
AM7	6 (BL)	6	IO	PB6A	—	L19T_D0
AN6	6 (BL)	6	IO	PB6B	—	L19C_D0
AP2	6 (BL)	—	VDDIO6	VDDIO6	—	—
AL8	6 (BL)	7	IO	PB6C	D15	L20T_A0
AL9	6 (BL)	7	IO	PB6D	D16	L20C_A0
AK9	6 (BL)	7	IO	PB7B	—	—
U18	—	—	VSS	VSS	—	—
AN8	6 (BL)	7	IO	PB7C	D17	L21T_A0
AM8	6 (BL)	7	IO	PB7D	D18	L21C_A0
AN9	6 (BL)	7	IO	PB8A	—	L22T_D0
AP8	6 (BL)	7	IO	PB8B	—	L22C_D0
AK10	6 (BL)	7	IO	PB8C	VREF_6_07	L23T_A0
AL10	6 (BL)	7	IO	PB8D	D19	L23C_A0
AP9	6 (BL)	8	IO	PB9B	—	—
U19	—	—	VSS	VSS	—	—
AM10	6 (BL)	8	IO	PB9C	D20	L24T_A0
AM11	6 (BL)	8	IO	PB9D	D21	L24C_A0
AK11	6 (BL)	8	IO	PB10B	—	—
AN10	6 (BL)	8	IO	PB10C	VREF_6_08	L25T_A0
AP10	6 (BL)	8	IO	PB10D	D22	L25C_A0
AN11	6 (BL)	9	IO	PB11A	—	L26T_A0
AP11	6 (BL)	9	IO	PB11B	—	L26C_A0
V16	—	—	VSS	VSS	—	—
AL12	6 (BL)	9	IO	PB11C	D23	L27T_A0
AK12	6 (BL)	9	IO	PB11D	D24	L27C_A0
AN12	6 (BL)	9	IO	PB12A	—	L28T_A0

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
AM28	5 (BC)	7	IO	PB31D	—	L26C_A0
AN30	5 (BC)	7	IO	PB32B	—	—
R14	—	—	VSS	VSS	—	—
AK25	5 (BC)	7	IO	PB32C	—	L27T_D0
AL26	5 (BC)	7	IO	PB32D	—	L27C_D0
AN17	5 (BC)	—	VDDIO5	VDDIO5	—	—
AL27	5 (BC)	8	IO	PB33C	—	L28T_A0
AL28	5 (BC)	8	IO	PB33D	VREF_5_08	L28C_A0
AN31	5 (BC)	8	IO	PB34B	—	—
R15	—	—	VSS	VSS	—	—
AK26	5 (BC)	8	IO	PB34D	—	—
AM30	5 (BC)	9	IO	PB35B	—	—
AL29	5 (BC)	9	IO	PB35D	VREF_5_09	—
AK27	5 (BC)	9	IO	PB36B	—	—
R20	—	—	VSS	VSS	—	—
AL30	5 (BC)	9	IO	PB36C	—	L29T_D0
AK29	5 (BC)	9	IO	PB36D	—	L29C_D0
AK28	—	—	VDD33	VDD33	—	—
AA16	—	—	VDD15	VDD15	—	—
AP32	—	—	IO	PSCHAR_LDIO9	—	—
AP33	—	—	IO	PSCHAR_LDIO8	—	—
AN32	—	—	IO	PSCHAR_LDIO7	—	—
AM31	—	—	IO	PSCHAR_LDIO6	—	—
AA17	—	—	VDD15	VDD15	—	—
AM32	—	—	VDD33	VDD33	—	—
AL31	—	—	IO	PSCHAR_LDIO5	—	—
AM33	—	—	IO	PSCHAR_LDIO4	—	—
AA18	—	—	VDD15	VDD15	—	—
AK30	—	—	IO	PSCHAR_LDIO3	—	—
AL32	—	—	IO	PSCHAR_LDIO2	—	—
AA19	—	—	VDD15	VDD15	—	—
AB16	—	—	VDD15	VDD15	—	—
AK31	—	—	VDD33	VDD33	—	—
AJ30	—	—	IO	PSCHAR_LDIO1	—	—
AK33	—	—	IO	PSCHAR_LDIO0	—	—
AK34	—	—	IO	PSCHAR_CKIO1	—	—
AJ31	—	—	IO	PSCHAR_CKIO0	—	—
AJ33	—	—	IO	PSCHAR_XCK	—	—
AJ34	—	—	IO	PSCHAR_WDSYNC	—	—
AH30	—	—	IO	PSCHAR_CV	—	—
AH31	—	—	IO	PSCHAR_BYTSYNC	—	—
AH32	—	—	O	ATMOUT_B (no connect)	—	—
AH33	—	—	VSS	VSS	—	—
AH34	—	—	VDDGB_B	VDDGB_B	—	—

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
P32	—	—	VDD_ANA	VDD_ANA	—	—
J34	—	—	I	HDINP_AA	—	—
J33	—	—	I	HDINN_AA	—	—
R32	—	—	VDD_ANA	VDD_ANA	—	—
L30	—	—	VDDIB	VDDIB_AA	—	—
K31	—	—	—	REFCLKP_A	—	—
K30	—	—	—	REFCLKN_A	—	—
J31	—	—	O	REXTN_A	—	—
J30	—	—	O	REXT_A	—	—
Y32	—	—	VDD_ANA	VDD_ANA	—	—
G34	—	—	VDDGB_A	VDDGB_A	—	—
G33	—	—	VSS	VSS	—	—
G32	—	—	O	ATMOUT_A (no connect)	—	—
G31	—	—	I	PRESERVE01 (no connect)	—	—
F33	—	—	I	PRESERVE02 (no connect)	—	—
G30	—	—	I	PRESERVE03 (no connect)	—	—
F31	—	—	O	PSYS_RSSIG_ALL	—	—
F30	—	—	I	PSYS_DOBISTN	—	—
E31	—	—	VDD33	VDD33	—	—
AB17	—	—	VDD15	VDD15	—	—
AB18	—	—	VDD15	VDD15	—	—
D32	—	—	I	PBIST_TEST_ENN	—	—
E30	—	—	I	PLOOP_TEST_ENN	—	—
AB19	—	—	VDD15	VDD15	—	—
D31	—	—	I	PASB_PDN	—	—
C32	—	—	I	PMP_TESTCLK	—	—
C31	—	—	VDD33	VDD33	—	—
AJ32	—	—	VDD15	VDD15	—	—
B32	—	—	I	PASB_RESETN	—	—
A33	—	—	I	PASB_TRISTN	—	—
B31	—	—	I	PMP_TESTCLK_ENN	—	—
A32	—	—	I	PASB_TESTCLK	—	—
AK32	—	—	VDD15	VDD15	—	—
AB21	—	—	VSS	VSS	—	—
A31	—	—	VDD33	VDD33	—	—
B30	1 (TC)	7	IO	PT36D	—	—
AB22	—	—	VSS	VSS	—	—
C30	1 (TC)	7	IO	PT36B	—	—
D30	1 (TC)	7	IO	PT35D	—	—
B13	1 (TC)	—	VDDIO1	VDDIO1	—	—
E29	1 (TC)	7	IO	PT35B	—	—
E28	1 (TC)	7	IO	PT34D	VREF_1_07	—
AN33	—	—	VSS	Vss	—	—
D29	1 (TC)	8	IO	PT34B	—	—

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
B24	1 (TC)	3	IO	PT23B	—	—
D20	1 (TC)	3	IO	PT22D	—	L15C_A0
D19	1 (TC)	3	IO	PT22C	—	L15T_A0
N14	—	—	Vss	Vss	—	—
E19	1 (TC)	3	IO	PT22B	—	L16C_A0
E18	1 (TC)	3	IO	PT22A	—	L16T_A0
C21	1 (TC)	4	IO	PT21D	—	L17C_A0
C20	1 (TC)	4	IO	PT21C	—	L17T_A0
A25	1 (TC)	4	IO	PT21B	—	L18C_A0
A24	1 (TC)	4	IO	PT21A	—	L18T_A0
B23	1 (TC)	4	IO	PT20D	—	L19C_A0
A23	1 (TC)	4	IO	PT20C	—	L19T_A0
N15	—	—	Vss	Vss	—	—
E17	1 (TC)	4	IO	PT20B	—	L20C_A0
E16	1 (TC)	4	IO	PT20A	—	L20T_A0
B22	1 (TC)	4	IO	PT19D	—	L21C_A0
B21	1 (TC)	4	IO	PT19C	VREF_1_04	L21T_A0
C18	1 (TC)	4	IO	PT19B	—	L22C_A0
C19	1 (TC)	4	IO	PT19A	—	L22T_A0
N20	—	—	Vss	Vss	—	—
A22	1 (TC)	5	IO	PT18D	PTCK1C	L23C_A0
A21	1 (TC)	5	IO	PT18C	PTCK1T	L23T_A0
N21	—	—	Vss	Vss	—	—
D17	1 (TC)	5	IO	PT18B	—	L24C_A0
D18	1 (TC)	5	IO	PT18A	—	L24T_A0
B20	1 (TC)	5	IO	PT17D	PTCK0C	L25C_A0
B19	1 (TC)	5	IO	PT17C	PTCK0T	L25T_A0
A20	1 (TC)	5	IO	PT17B	—	L26C_A0
A19	1 (TC)	5	IO	PT17A	—	L26T_A0
A18	1 (TC)	5	IO	PT16D	VREF_1_05	L27C_A0
B18	1 (TC)	5	IO	PT16C	—	L27T_A0
Y21	—	—	Vss	Vss	—	—
C17	1 (TC)	5	IO	PT16B	—	L28C_D0
D16	1 (TC)	5	IO	PT16A	—	L28T_D0
A17	1 (TC)	6	IO	PT15D	—	L29C_D0
B16	1 (TC)	6	IO	PT15C	—	L29T_D0
E15	1 (TC)	6	IO	PT15B	—	L30C_A0
E14	1 (TC)	6	IO	PT15A	—	L30T_A0
A16	1 (TC)	6	IO	PT14D	—	L31C_A0
A15	1 (TC)	6	IO	PT14C	VREF_1_06	L31T_A0
Y22	—	—	Vss	Vss	—	—
D14	1 (TC)	6	IO	PT14B	—	—
C16	0 (TL)	1	IO	PT13D	MPI_RTRY_N	L1C_A0
C15	0 (TL)	1	IO	PT13C	MPI_ACK_N	L1T_A0

Table 45. ORT82G5 680-Pin PBGAM (fpBGA) Pinout (Continued)

680-PBGAM	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	680-PBGAM
D7	0 (TL)	—	VDDIO0	VDDIO0	—	—
C14	0 (TL)	1	IO	PT13B	—	L2C_A0
B14	0 (TL)	1	IO	PT13A	VREF_0_01	L2T_A0
A14	0 (TL)	1	IO	PT12D	M0	L3C_A0
A13	0 (TL)	1	IO	PT12C	M1	L3T_A0
AA20	—	—	Vss	Vss	—	—
E12	0 (TL)	2	IO	PT12B	MPI_CLK	L4C_A0
E13	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L4T_A0
C13	0 (TL)	2	IO	PT11D	M2	L5C_A0
C12	0 (TL)	2	IO	PT11C	M3	L5T_A0
B12	0 (TL)	2	IO	PT11B	VREF_0_02	L6C_A0
A12	0 (TL)	2	IO	PT11A	MPI_TEA_N	L6T_A0
D12	0 (TL)	3	IO	PT10D	—	L7C_D0
C11	0 (TL)	3	IO	PT10C	—	L7T_D0
B11	0 (TL)	3	IO	PT10B	—	—
A11	0 (TL)	3	IO	PT9D	VREF_0_03	L8C_A0
A10	0 (TL)	3	IO	PT9C	—	L8T_A0
AA21	—	—	Vss	Vss	—	—
B10	0 (TL)	3	IO	PT9B	—	—
E11	0 (TL)	3	IO	PT8D	D0	L9C_D0
D10	0 (TL)	3	IO	PT8C	TMS	L9T_D0
C10	0 (TL)	3	IO	PT8B	—	—
A9	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L10C_A0
B9	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L10T_A0
AA22	—	—	Vss	Vss	—	—
E10	0 (TL)	4	IO	PT7B	—	—
A8	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L11C_A0
B8	0 (TL)	4	IO	PT6C	D3	L11T_A0
D9	0 (TL)	4	IO	PT6B	VREF_0_04	L12C_D0
C8	0 (TL)	4	IO	PT6A	—	L12T_D0
E9	0 (TL)	5	IO	PT5D	D1	L13C_D0
D8	0 (TL)	5	IO	PT5C	D2	L13T_D0
AB13	—	—	Vss	Vss	—	—
A7	0 (TL)	5	IO	PT5B	—	L14C_A0
A6	0 (TL)	5	IO	PT5A	VREF_0_05	L14T_A0
C7	0 (TL)	5	IO	PT4D	TDI	L15C_D0
B6	0 (TL)	5	IO	PT4C	TCK	L15T_D0
E8	0 (TL)	5	IO	PT4B	—	L16C_A0
E7	0 (TL)	5	IO	PT4A	—	L16T_A0
A5	0 (TL)	6	IO	PT3D	—	L17C_A0
B5	0 (TL)	6	IO	PT3C	VREF_0_06	L17T_A0
AB14	—	—	Vss	Vss	—	—
C6	0 (TL)	6	IO	PT3B	—	L18C_A0
D6	0 (TL)	6	IO	PT3A	—	L18T_A0