Infineon Technologies - CY8C3445AXI-104 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3445axi-104

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C34 family these blocks can include four 16-bit timer, counter, and PWM blocks; I²C slave, master, and multi-master; Full-Speed USB; and Full CAN 2.0b.

For more details on the peripherals see the "Example Peripherals" section on page 43 of this data sheet. For information on UDBs, DSI, and other digital blocks, see the "Digital Subsystem" section on page 43 of this data sheet.

PSoC's analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 1-percent error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Voltage references
- Analog-to-digital converter (ADC)
- Digital-to-analog converters (DACs)

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. The heart of the analog subsystem is a fast, accurate, configurable delta-sigma ADC with these features:

- Less than 100 µV offset
- A gain error of 0.2 percent
- INL less than ±1 LSB
- DNL less than ±1 LSB
- SINAD better than 66 dB

This converter addresses a wide variety of precision analog applications, including some of the most demanding sensors.

Two high-speed voltage or current DACs support 8-bit output signals at update rate of 8 Msps in current DAC (IDAC) and 1 Msps in voltage DAC (VDAC). They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths.

In addition to the ADC and DACs, the analog subsystem provides multiple:

- Uncommitted opamps
- Configurable switched capacitor/continuous time (SC/CT) blocks. These support:
  - Transimpedance amplifiers
  - Programmable gain amplifiers
  - Mixers
  - Other similar analog components

See the "Analog Subsystem" section on page 56 of this data sheet for more details.

PSoC's 8051 CPU subsystem is built around a single cycle pipelined 8051 8-bit processor running at up to 50 MHz. The CPU subsystem includes a programmable nested vector interrupt controller, DMA controller, and RAM. PSoC's nested vector interrupt controller provides low latency by allowing the CPU to vector directly to the first address of the interrupt service routine, bypassing the jump instruction required by other architectures. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor. The processor speed itself is configurable, allowing you to tune active power consumption for specific applications.

PSoC's nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 64 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling bootloaders. You can enable an error correcting code (ECC) for high reliability applications. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Up to 2 KB of byte-writeable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after power-on reset (POR).

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the VDDIO pins. Every GPIO has analog I/O, LCD drive[3], CapSense[4], flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow VOH to be set independently of VDDIO when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I²C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with Full-Speed USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All of the features of the PSoC I/Os are covered in detail in the "I/O System and Routing" section on page 36 of this data sheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The Internal Main Oscillator (IMO) is the clock base for the system, and has 2-percent accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 24 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs.

Notes
3. This feature on select devices only. See Ordering Information on page 121 for details.
4. GPIOs with opamp outputs are not recommended for use with CapSense.

4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight Multi-layer AHB Bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8, 16, 24, and 32-bit addressing and data

Table 4-6. PHUB Spokes and Peripherals

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, CAN, I2C, Timers, Counters, and PWMs
5	Reserved
6	UDBs group 1
7	UDBs group 2

4.4.2 DMA Features

- Twenty-four DMA channels
- Each channel has one or more Transaction Descriptors (TDs) to configure channel behavior. Up to 128 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel
- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64 KB
- TDs may be nested and/or chained for complex transactions

4.4.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100 percent of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in Table 4-7 after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

Table 4-7. Priority Levels

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

4.4.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

5.6 External Memory Interface

CY8C34 provides an External Memory Interface (EMIF) for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles.

Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C34 supports only one type of external memory device at a time.

External memory can be accessed via the 8051 xdata space; up to 24 address bits can be used. See "xdata Space" section on page 26. The memory can be 8 or 16 bits wide.

Figure 5-1. EMIF Block Diagram

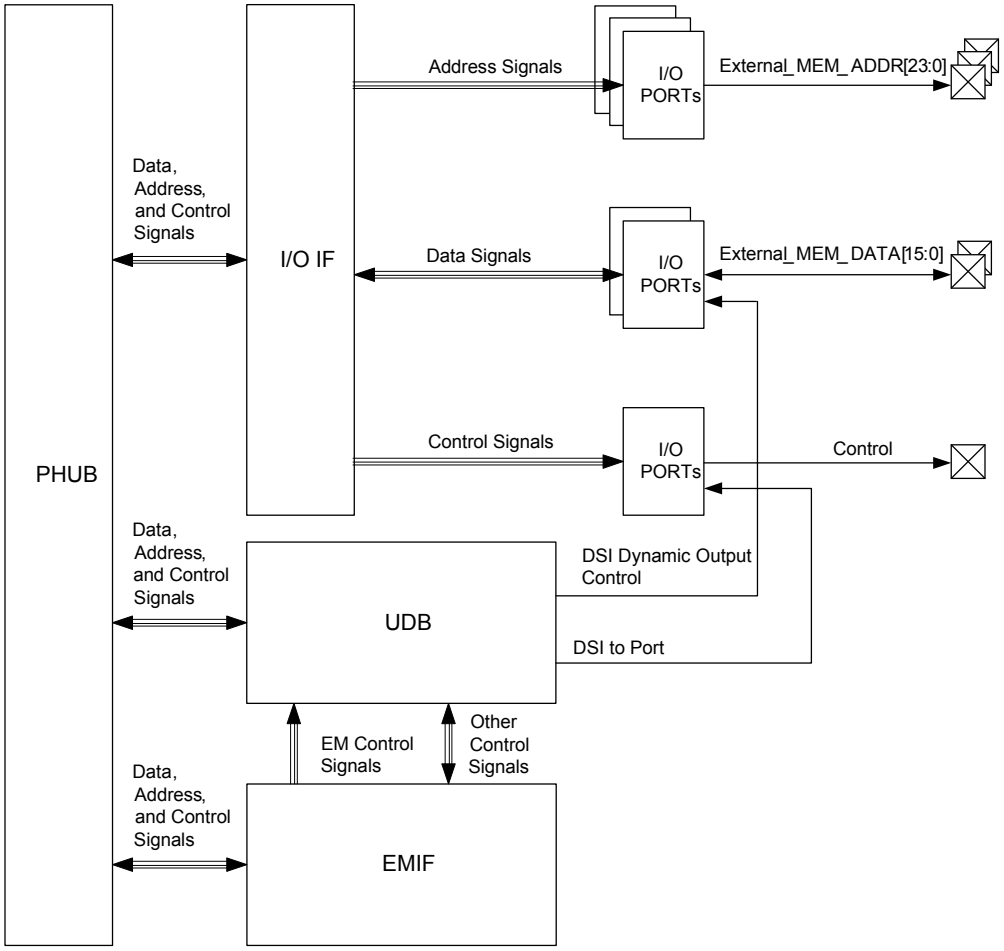
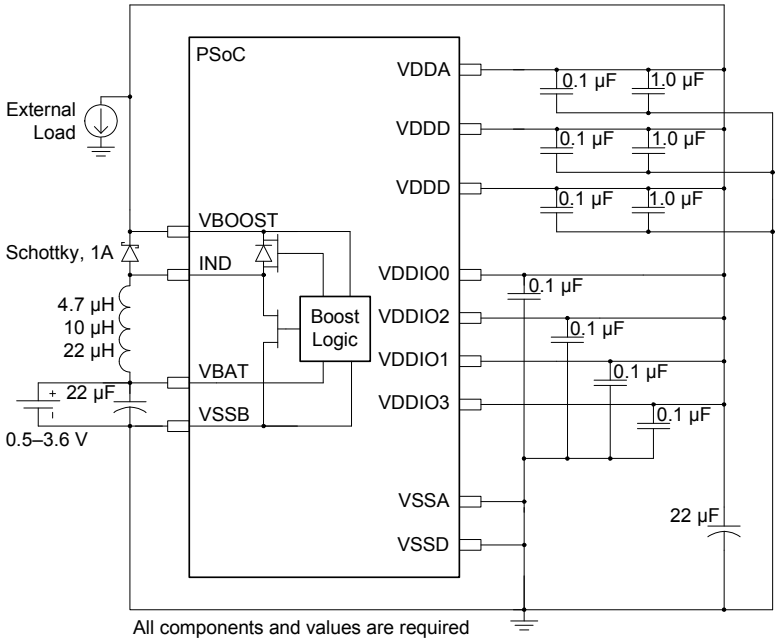
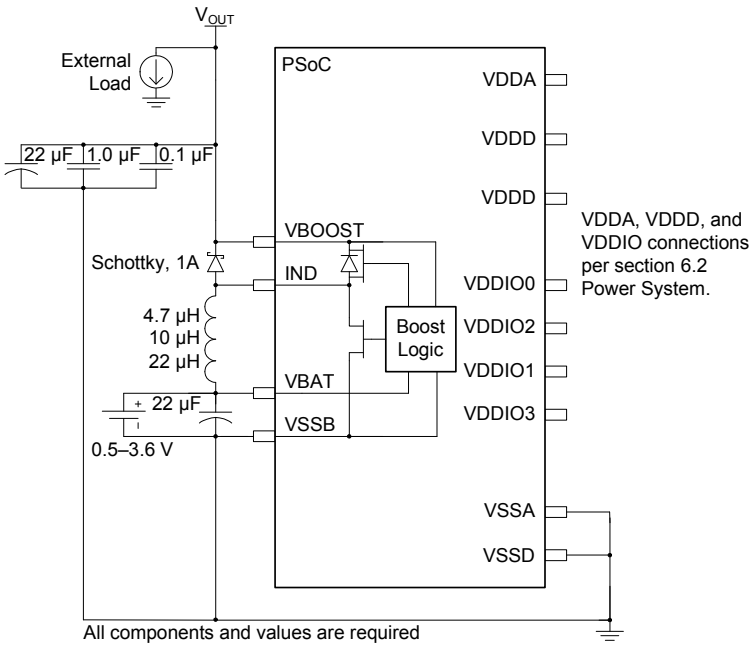


Figure 6-6. Application of Boost Converter powering PSoC device



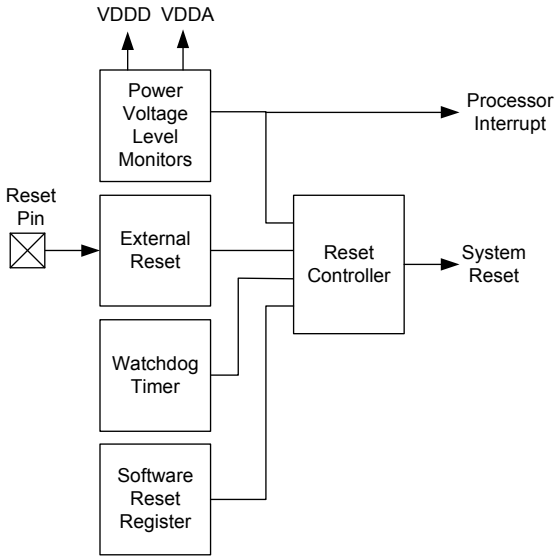
The boost converter may also generate a supply that is not used directly by the PSoC device. An example of this use case is boosting a 1.8 V supply to 4.0 V to drive a white LED. If the boost converter is not supplying the PSoC devices V_{DDA}, V_{DDD}, and V_{DDIO} it must comply with the same design rules as supplying the PSoC device, but with a change to the bulk capacitor requirements. A parallel arrangement 22 µF, 1.0 µF, and 0.1 µF capacitors are all required on the Vout supply and must be placed within 1 cm of the VBOOST pin to ensure regulator stability.

Figure 6-7. Application of Boost Converter not powering PSoC device



The switching frequency is set to 400 kHz using an oscillator integrated into the boost converter. The boost converter can be operated in two different modes: active and standby. Active mode is the normal mode of operation where the boost regulator actively generates a regulated output voltage. In standby mode, most boost functions are disabled, thus reducing power consumption of the boost circuit. Only minimal power is provided, typically < 5 µA to power the PSoC device in Sleep mode. The

Figure 6-8. Resets



The term **device reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to detect and report certain exception conditions. This register is cleared after a power-on reset. For details see the Technical Reference Manual.

6.3.1 Reset Sources

6.3.1.1 Power Voltage Level Monitors

- IPOR – Initial Power-on Reset

  At initial power on, IPOR monitors the power voltages V_{DDD}, V_{DDA}, V_{CCD} and V_{CCA}. The trip level is not precise. It is set to approximately 1 volt, which is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 150 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

  After boot, the IPOR circuit is disabled and voltage supervision is handed off to the precise low-voltage reset (PRES) circuit.

- PRES – Precise Low Voltage Reset

  This circuit monitors the outputs of the analog and digital internal regulators after power up. The regulator outputs are compared to a precise reference voltage. The response to a PRES trip is identical to an IPOR reset.

  In normal operating mode, the program cannot disable the digital PRES circuit. The analog regulator can be disabled, which also disables the analog portion of the PRES. The PRES circuit is disabled automatically during sleep and hibernate modes, with one exception: During sleep mode the regulators are periodically activated (buzzed) to provide supervisory services and to reduce wakeup time. At these times the PRES circuit is also buzzed to allow periodic voltage monitoring.

- ALVI, DLVI, AHVI – Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

  Interrupt circuits are available to detect when VDDA and VDDD go outside a voltage range. For AHVI, VDDA is compared to a fixed trip level. For ALVI and DLVI, VDDA and VDDD are compared to trip levels that are programmable, as listed in Table 6-5. ALVI and DLVI can also be configured to generate a device reset instead of an interrupt.

Table 6-5. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings
DLVI	VDDD	1.71 V to 5.5 V	1.70 V to 5.45 V in 250 mV increments
ALVI	VDDA	1.71 V to 5.5 V	1.70 V to 5.45 V in 250 mV increments
AHVI	VDDA	1.71 V to 5.5 V	5.75 V

The monitors are disabled until after IPOR. During sleep mode these circuits are periodically activated (buzzed). If an interrupt occurs during buzzing then the system first enters its wake up sequence. The interrupt is then recognized and may be serviced.

The buzz frequency is adjustable, and should be set to be less than the minimum time that any voltage is expected to be out of range. For details on how to adjust the buzz frequency, see the TRM.

6.3.1.2 Other Reset Sources

- XRES – External Reset

  PSoC 3 has either a single GPIO pin that is configured as an external reset or a dedicated XRES pin. Either the dedicated XRES pin or the GPIO pin, if configured, holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset.

  After XRES has been deasserted, at least 10 µs must elapse before it can be reasserted.

  The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

- SRES – Software Reset

  A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

  Another register bit exists to disable this function.

- WRES – Watchdog Timer Reset

  The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

  Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power-on reset event.

Figure 6-10. SIO Input/Output Block Diagram

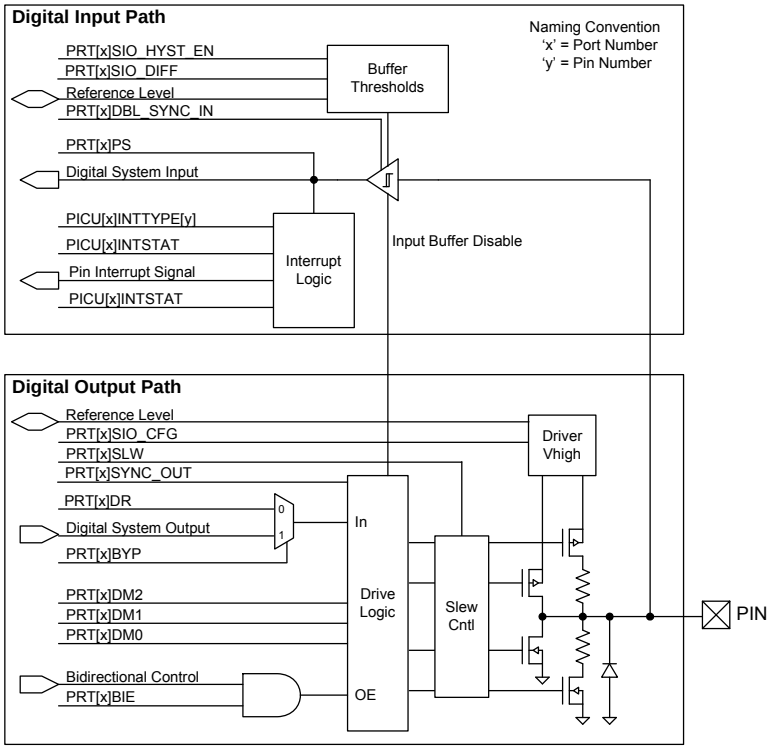
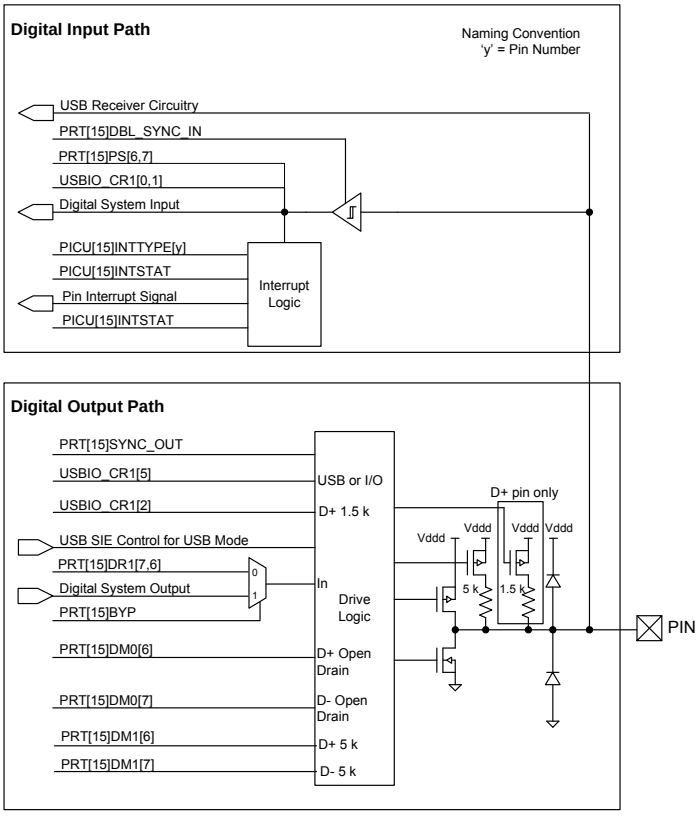


Figure 6-11. USBIO Block Diagram



6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to “1” and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt.

While level sensitive interrupts are not directly supported; Universal Digital Blocks (UDB) provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip’s analog (VDDA) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine VDDIO capability for a given port and pin.

The SIO port pins support an additional regulated high output capability, as described in Adjustable Output Level.

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders[15]. See the “CapSense” section on page 64 for more information.

6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the “LCD Direct Drive” section on page 63 for details.

6.4.11 Adjustable Output Level

This section applies only to SIO pins. SIO port pins support the ability to provide a regulated high output level for interface to external signals that are lower in voltage than the SIO’s respective VDDIO. SIO pins are individually configurable to output either the standard VDDIO level or the regulated output, which is based on an internally generated reference. Typically a voltage DAC (VDAC) is used to generate the reference (see Figure 6-13). The “DAC” section on page 64 has more details on VDAC use and reference routing to the SIO pins. Resistive pull-up and pull-down drive modes are not available with SIO in regulated output mode.

6.4.12 Adjustable Input Level

This section applies only to SIO pins. SIO pins by default support the standard CMOS and LVTTL input levels but also support a differential mode with programmable levels. SIO pins are grouped into pairs. Each pair shares a reference generator block which, is used to set the digital input buffer reference level for interface to external signals that differ in voltage from VDDIO. The reference sets the pins voltage threshold for a high logic level (see Figure 6-13). Available input thresholds are:

- 0.5 × VDDIO
- 0.4 × VDDIO
- 0.5 × VREF
- VREF

Typically a voltage DAC (VDAC) generates the V_{REF} reference. “DAC” section on page 64 has more details on VDAC use and reference routing to the SIO pins.

Note
15. GPIOs with opamp outputs are not recommended for use with CapSense

- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register

Independent of the ALU operation, these functions are available:

- Shift left
- Shift right
- Nibble swap
- Bitwise OR mask

7.2.2.3 Conditionals

Each datapath has two compares, with bit masking options. Compare operands include the two accumulators and the two data registers in a variety of configurations. Other conditions include zero detect, all ones detect, and overflow. These conditions are the primary datapath outputs, a selection of which can be driven out to the UDB routing matrix. Conditional computation can use the built in chaining to neighboring UDBs to operate on wider data widths without the need to use routing resources.

7.2.2.4 Variable MSB

The most significant bit of an arithmetic and shift function can be programmatically specified. This supports variable width CRC and PRS functions, and in conjunction with ALU output masking, can implement arbitrary width timers, counters and shift blocks.

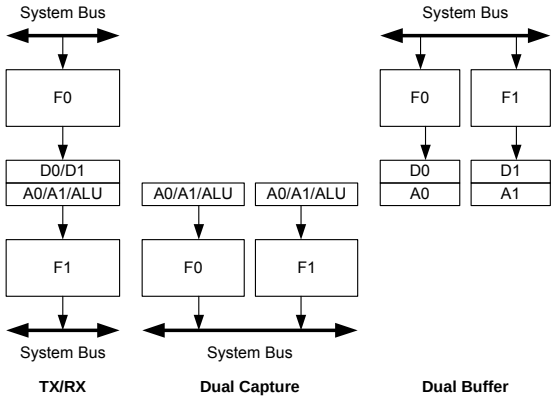
7.2.2.5 Built in CRC/PRS

The datapath has built in support for single cycle Cyclic Redundancy Check (CRC) computation and Pseudo Random Sequence (PRS) generation of arbitrary width and arbitrary polynomial. CRC/PRS functions longer than 8 bits may be implemented in conjunction with PLD logic, or built in chaining may be use to extend the function into neighboring UDBs.

7.2.2.6 Input/Output FIFOs

Each datapath contains two four-byte deep FIFOs, which can be independently configured as an input buffer (system bus writes to the FIFO, datapath internal reads the FIFO), or an output buffer (datapath internal writes to the FIFO, the system bus reads from the FIFO). The FIFOs generate status that are selectable as datapath outputs and can therefore be driven to the routing, to interact with sequencers, interrupts, or DMA.

Figure 7-5. Example FIFO Configurations



7.2.2.7 Chaining

The datapath can be configured to chain conditions and signals such as carries and shift data with neighboring datapaths to create higher precision arithmetic, shift, CRC/PRS functions.

7.2.2.8 Time Multiplexing

In applications that are over sampled, or do not need high clock rates, the single ALU block in the datapath can be efficiently shared with two sets of registers and condition generators. Carry and shift out data from the ALU are registered and can be selected as inputs in subsequent cycles. This provides support for 16-bit functions in one (8-bit) datapath.

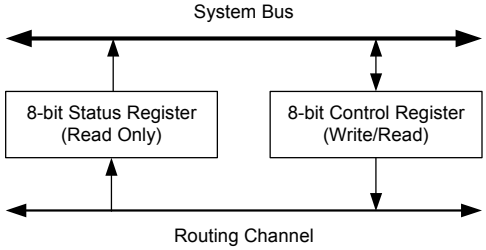
7.2.2.9 Datapath I/O

There are six inputs and six outputs that connect the datapath to the routing matrix. Inputs from the routing provide the configuration for the datapath operation to perform in each cycle, and the serial data inputs. Inputs can be routed from other UDB blocks, other device peripherals, device I/O pins, and so on. The outputs to the routing can be selected from the generated conditions, and the serial data outputs. Outputs can be routed to other UDB blocks, device peripherals, interrupt and DMA controller, I/O pins, and so on.

7.2.3 Status and Control Module

The primary purpose of this circuitry is to coordinate CPU firmware interaction with internal UDB operation.

Figure 7-6. Status and Control Registers

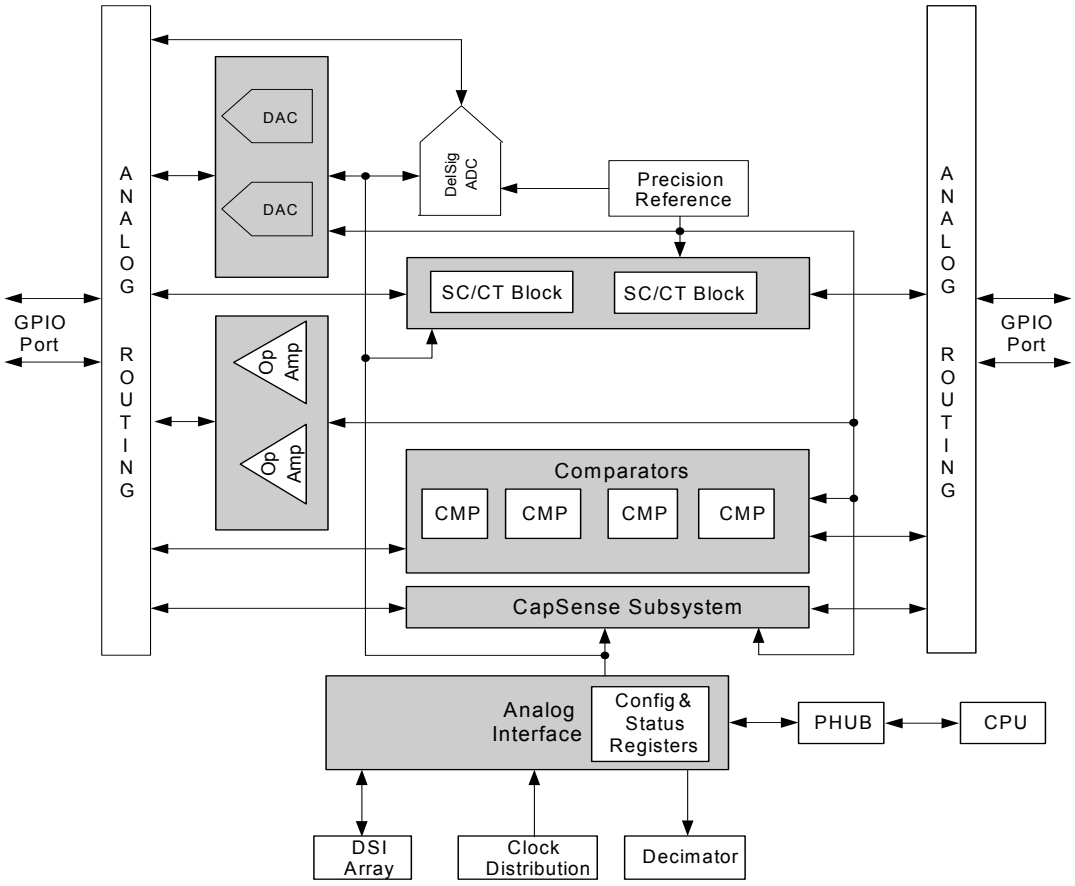


8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses.
- High resolution Delta-Sigma ADC.
- Two 8-bit DACs that provide either voltage or current output.
- Four comparators with optional connection to configurable LUT outputs.
- Two configurable switched capacitor/continuous time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer.
- Two opamps for internal use and connection to GPIO that can be used as high current output buffers.
- CapSense subsystem to enable capacitive touch sensing.
- Precision reference for generating an accurate analog voltage for internal analog blocks.

Figure 8-1. Analog Subsystem Block Diagram



The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions (PGA, transimpedance amplifier, voltage DAC, current DAC, and so on). The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

8.1 Analog Routing

The CY8C34 family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks.

For information on how to make pin selections for optimal analog routing, refer to the application note, AN58304 - PSoC® 3 and PSoC® 5 - Pin Selection for Analog Designs.

8.1.1 Features

- Flexible, configurable analog routing architecture
- 16 Analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus
- 8 Analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the CY8C34 family. The analog routing architecture is divided into four quadrants as shown in Figure 8-2. Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in CY8C34, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in Figure 8-2.

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ[25]	Max	Units
	Sleep Mode[28]						
	CPU = OFF RTC = ON (= ECO32K ON, in low-power mode) Sleep timer = ON (= ILO ON at 1 kHz)[29] WDT = OFF I2C Wake = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V - 5.5 V	T = –40 °C	–	1.1	2.3	µA
			T = 25 °C	–	1.1	2.2	
			T = 85 °C	–	15	30	
		$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V	T = –40 °C	–	1	2.2	
			T = 25 °C	–	1	2.1	
			T = 85 °C	–	12	28	
		$V_{DD} = V_{DDIO}$ = 1.71 V – 1.95 V[30]	T = 25 °C	–	2.2	4.2	
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I2C Wake = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V[31]	T = 25 °C	–	2.2	2.7	
	I2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V[31]	T = 25 °C	–	2.2	2.8	
	Hibernate Mode[28]						
	Hibernate mode current All regulators and oscillators off SRAM retention GPIO interrupts are active Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V - 5.5 V	T = –40 °C	–	0.2	1.5	µA
			T = 25 °C	–	0.5	1.5	
			T = 85 °C	–	4.1	5.3	
		$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V	T = –40 °C	–	0.2	1.5	
			T = 25 °C	–	0.2	1.5	
			T = 85 °C	–	3.2	4.2	
		$V_{DD} = V_{DDIO}$ = 1.71 V – 1.95 V[30]	T = –40 °C	–	0.2	1.5	
			T = 25 °C	–	0.3	1.5	
			T = 85 °C	–	3.3	4.3	
I_{DDAR}	Analog current consumption while device is reset[32]	$V_{DDA} \leq 3.6$ V		–	0.3	0.6	mA
		$V_{DDA} > 3.6$ V		–	1.4	3.3	mA
I_{DDDR}	Digital current consumption while device is reset[32]	$V_{DDD} \leq 3.6$ V		–	1.1	3.1	mA
		$V_{DDD} > 3.6$ V		–	0.7	3.1	mA

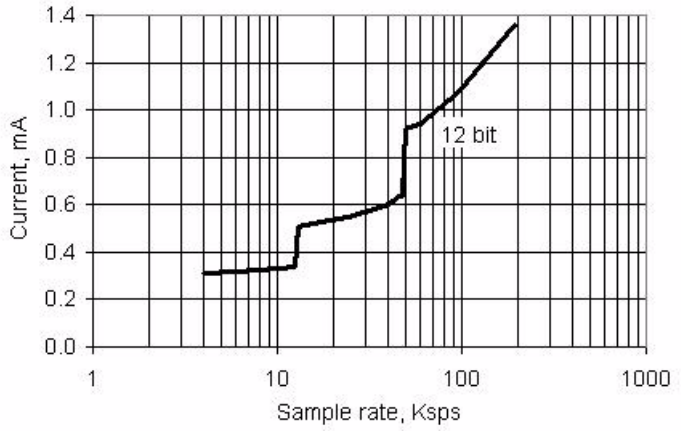
Table 11-22. Delta-sigma ADC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time		–	–	4	Samples
THD	Total harmonic distortion[51]	Buffer gain = 1, 12-bit, Range = ±1.024 V	–	–	0.0032	%
12-Bit Resolution Mode						
SR12	Sample rate, continuous, high power[51]	Range = ±1.024 V, unbuffered	4	–	192	ksps
BW12	Input bandwidth at max sample rate[51]	Range = ±1.024 V, unbuffered	–	44	–	kHz
SINAD12int	Signal to noise ratio, 12-bit, internal reference[51]	Range = ±1.024 V, unbuffered	66	–	–	dB
8-Bit Resolution Mode						
SR8	Sample rate, continuous, high power[51]	Range = ±1.024 V, unbuffered	8	–	384	ksps
BW8	Input bandwidth at max sample rate[51]	Range = ±1.024 V, unbuffered	–	88	–	kHz
SINAD8int	Signal to noise ratio, 8-bit, internal reference[51]	Range = ±1.024 V, unbuffered	43	–	–	dB

Table 11-23. Delta-sigma ADC Sample Rates, Range = ±1.024 V

Resolution, Bits	Continuous		Multi-Sample	
	Min	Max	Min	Max
8	8000	384000	1911	91701
9	6400	307200	1543	74024
10	5566	267130	1348	64673
11	4741	227555	1154	55351
12	4000	192000	978	46900

Figure 11-33. Delta-sigma ADC IDD vs sps, Range = ±1.024 V, Continuous Sample Mode, Input Buffer Bypassed



Note
51. Based on device characterization (Not production tested).

11.5.3 Voltage Reference

Table 11-24. Voltage Reference Specifications

See also ADC external reference specifications in *Section 11.5.2*.

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{REF}	Precision reference voltage	Initial trimming, 25 °C	1.014 (–1%)	1.024	1.034 (+1%)	V

11.5.4 Analog Globals

Table 11-25. Analog Globals Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rppag	Resistance pin-to-pin through P2[4], AGL0, DSM INP, AGL1, P2[5][52]	V_{DDA} = 3 V	–	1472	2200	Ω
Rppmuxbus	Resistance pin-to-pin through P2[3], amuxbusL, P2[4][52]	V_{DDA} = 3 V	–	706	1100	Ω

11.5.5 Comparator

Table 11-26. Comparator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage in fast mode	Factory trim, V_{DDA} > 2.7 V, $V_{IN} \geq 0.5$ V	–		10	mV
	Input offset voltage in slow mode	Factory trim, Vin ≥ 0.5 V	–		9	mV
	Input offset voltage in fast mode[53]	Custom trim	–	–	4	mV
	Input offset voltage in slow mode[53]	Custom trim	–	–	4	mV
	Input offset voltage in ultra low-power mode	$V_{DDA} \leq 4.6$ V	–	±12	–	mV
V_{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V_{ICM}	Input common mode voltage	High current / fast mode	V_{SSA}	–	V_{DDA}	V
		Low current / slow mode	V_{SSA}	–	V_{DDA}	V
		Ultra low power mode $V_{DDA} \leq 4.6$ V	V_{SSA}	–	V_{DDA} – 1.15	
CMRR	Common mode rejection ratio		–	50	–	dB
I_{CMP}	High current mode/fast mode[54]		–	–	400	µA
	Low current mode/slow mode[54]		–	–	100	µA
	Ultra low-power mode[54]	$V_{DDA} \leq 4.6$ V	–	6	–	µA

Table 11-27. Comparator AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESP}	Response time, high current mode[54]	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode[54]	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low-power mode[54]	50 mV overdrive, measured pin-to-pin, $V_{DDA} \leq 4.6$ V	–	55	–	µs

Notes
52. The resistance of the analog global and analog mux bus is high if $V_{DDA} \leq 2.7$ V, and the chip is in either sleep or hibernate mode. Use of analog global and analog mux bus under these conditions is not recommended.
53. The recommended procedure for using a custom trim value for the on-chip comparators can be found in the TRM.
54. Based on device characterization (Not production tested).

11.5.6 Current Digital-to-analog Converter (IDAC)

All specifications are based on use of the low-resistance IDAC output pins (see Pin Descriptions on page 11 for details). See the IDAC component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-28. IDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	8	bits
I_{OUT}	Output current at code = 255	Range = 2.04 mA, code = 255, $V_{DDA} \geq 2.7$ V, Rload = 600 Ω	–	2.04	–	mA
		Range = 2.04 mA, high speed mode, code = 255, $V_{DDA} \leq 2.7$ V, Rload = 300 Ω	–	2.04	–	mA
		Range = 255 µA, code = 255, Rload = 600 Ω	–	255	–	µA
		Range = 31.875 µA, code = 255, Rload = 600 Ω	–	31.875	–	µA
	Monotonicity		–	–	Yes	
Ezs	Zero scale error		–	0	±1	LSB
Eg	Gain error	Range = 2.04 mA, 25 °C	–	–	±2.5	%
		Range = 255 µA, 25 ° C	–	–	±2.5	%
		Range = 31.875 µA, 25 ° C	–	–	±3.5	%
TC_Eg	Temperature coefficient of gain error	Range = 2.04 mA	–	–	0.04	% / °C
		Range = 255 µA	–	–	0.04	% / °C
		Range = 31.875 µA	–	–	0.05	% / °C
INL	Integral nonlinearity	Sink mode, range = 255 µA, Codes 8 – 255, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.9	±1	LSB
		Source mode, range = 255 µA, Codes 8 – 255, Rload = 2.4 kΩ, Cload = 15 pF	–	±1.2	±1.6	LSB
DNL	Differential nonlinearity	Sink mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
		Source mode, range = 255 µA, Rload = 2.4 kΩ, Cload = 15 pF	–	±0.3	±1	LSB
Vcompliance	Dropout voltage, source or sink mode	Voltage headroom at max current, R_{LOAD} to V_{DDA} or R_{LOAD} to V_{SSA}, V_{DIFF} from V_{DDA}	1	–	–	V

Table 11-28. IDAC DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Operating current, code = 0	Low speed mode, source mode, range = 31.875 µA	–	44	100	µA
		Low speed mode, source mode, range = 255 µA,	–	33	100	µA
		Low speed mode, source mode, range = 2.04 mA	–	33	100	µA
		Low speed mode, sink mode, range = 31.875 µA	–	36	100	µA
		Low speed mode, sink mode, range = 255 µA	–	33	100	µA
		Low speed mode, sink mode, range = 2.04 mA	–	33	100	µA
		High speed mode, source mode, range = 31.875 µA	–	310	500	µA
		High speed mode, source mode, range = 255 µA	–	305	500	µA
		High speed mode, source mode, range = 2.04 mA	–	305	500	µA
		High speed mode, sink mode, range = 31.875 µA	–	310	500	µA
		High speed mode, sink mode, range = 255 µA	–	300	500	µA
		High speed mode, sink mode, range = 2.04 mA	–	300	500	µA

Figure 11-34. IDAC INL vs Input Code, Range = 255 µA, Source Mode

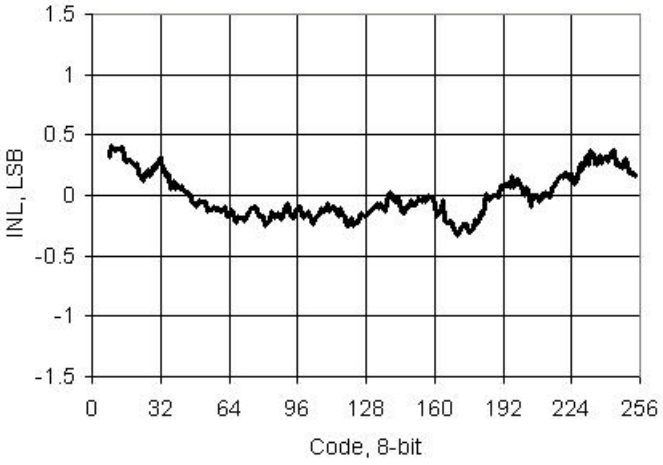


Figure 11-35. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

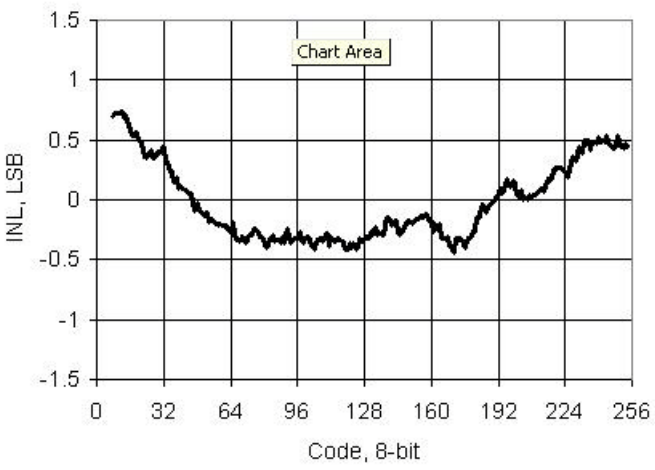


Table 11-29. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, High speed mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, High speed mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-44. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V

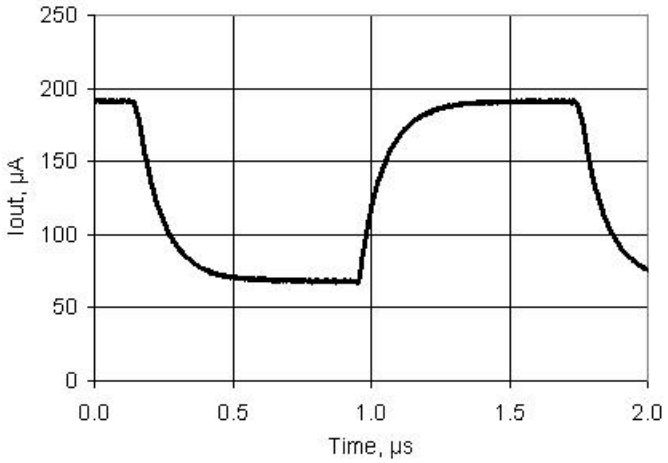


Figure 11-45. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V

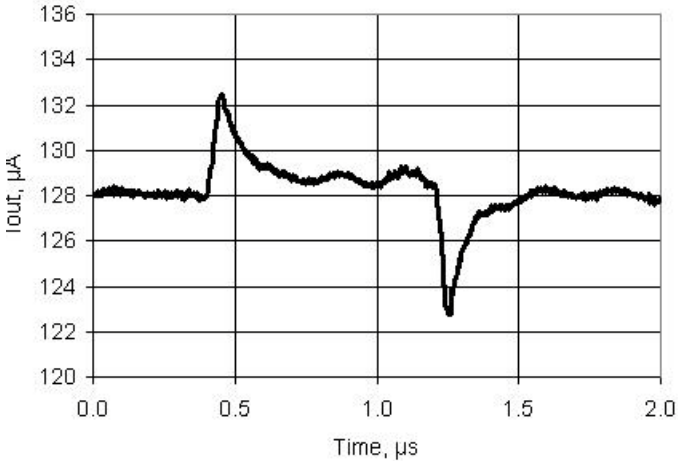


Figure 11-46. IDAC PSRR vs Frequency

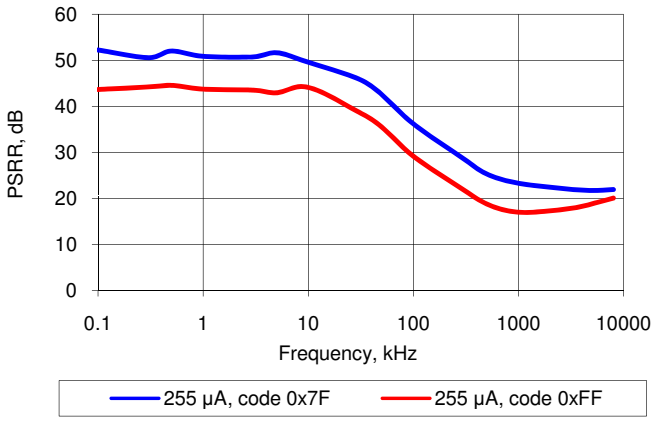
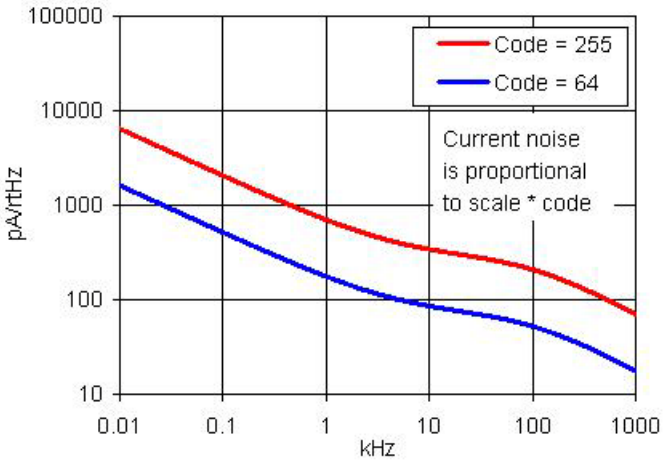


Figure 11-47. IDAC Current Noise, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V



11.7.2 EEPROM

Table 11-55. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		1.71	–	5.5	V

Table 11-56. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	10	20	ms
	EEPROM data retention time, retention period measured from last erase cycle	Average ambient temp, $T_A \le 25$ °C, 1M erase/program cycles	20	–	–	years
		Average ambient temp, $T_A \le 55$ °C, 100 K erase/program cycles	20	–	–	
		Average ambient temp. $T_A \le 85$ °C, 10 K erase/program cycles	10	–	–	

11.7.3 Nonvolatile Latches (NVL))

Table 11-57. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-58. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25 °C	1K	–	–	program/ erase cycles
		Programmed at 0 °C to 70 °C	100	–	–	program/ erase cycles
	NVL data retention time	Average ambient temp. $T_A \le 55$ °C	20	–	–	years
		Average ambient temp. $T_A \le 85$ °C	10	–	–	years

11.7.4 SRAM

Table 11-59. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{SRAM}	SRAM retention voltage		1.2	–	–	V

Table 11-60. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{SRAM}	SRAM operating frequency		DC	–	50.01	MHz

13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25.00	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA} (48-pin SSOP)		–	49	–	°C/Watt
T_{JA}	Package θ_{JA} (48-pin QFN)		–	14	–	°C/Watt
T_{JA}	Package θ_{JA} (68-pin QFN)		–	15	–	°C/Watt
T_{JA}	Package θ_{JA} (100-pin TQFP)		–	34	–	°C/Watt
T_{JC}	Package θ_{JC} (48-pin SSOP)		–	24	–	°C/Watt
T_{JC}	Package θ_{JC} (48-pin QFN)		–	15	–	°C/Watt
T_{JC}	Package θ_{JC} (68-pin QFN)		–	13	–	°C/Watt
T_{JC}	Package θ_{JC} (100-pin TQFP)		–	10	–	°C/Watt

Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
48-pin SSOP	MSL 3
48-pin QFN	MSL 3
68-pin QFN	MSL 3
100-pin TQFP	MSL 3

14. Acronyms

Table 14-1. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier

17. Revision History

Description Title: PSoC® 3: CY8C34 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-53304				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	2714270	06/03/09	VVSK	New data sheet
*A	2758970	09/02/09	MKEA	Updated Part Numbering Conventions Added Section 11.7.5 (EMIF Figures and Tables) Updated GPIO and SIO AC specifications Updated XRES Pin Description and Xdata Address Map specifications Updated DFB and Comparator specifications Updated PHUB features section and RTC in sleep mode Updated IDAC and VDAC DC and Analog Global specifications Updated USBIO AC and Delta Sigma ADC specifications Updated PPOR and Voltage Monitors DC specifications Updated Drive Mode diagram Added 48-QFN Information Updated other electrical specifications
*B	2824546	12/09/09	MKEA	Updated I2C section to reflect 1 Mbps. Updated Table 11-6 and 11- 7 (Boost AC and DC specs); also added Shottky Diode specs. Changed current for sleep/hibernate mode to include SIO; Added footnote to analog global specs. Updated Figures 1-1, 6-2, 7-14, and 8-1. Updated Table 6-2 and Table 6-3 (Hibernate and Sleep rows) and Power Modes section. Updated GPIO and SIO AC specifications. Updated Gain error in IDAC and VDAC specifications. Updated description of V_{DDA} spec in Table 11-1 and removed GPIO Clamp Current parameter. Updated number of UDBs on page 1. Moved FILO from ILO DC to AC table. Added PCB Layout and PCB Schematic diagrams. Updated Fgpioout spec (Table 11-9). Added duty cycle frequency in PLL AC spec table. Added note for Sleep and Hibernate modes and Active Mode specs in Table 11-2. Linked URL in Section 10.3 to PSoC Creator site. Updated Ja and Jc values in Table 13-1. Updated Single Sample Mode and Fast FIR Mode sections. Updated Input Resistance specification in Del-Sig ADC table. Added Tio_init parameter. Updated PGA and UGB AC Specs. Removed SPC ADC. Updated Boost Converter section. Added section 'SIO as Comparator'; updated Hysteresis spec (differential mode) in Table 11-10. Updated V_{BAT} condition and deleted Vstart parameter in Table 11-6. Added 'Bytes' column for Tables 4-1 to 4-5.
*C	2873322	02/04/10	MKEA	Changed maximum value of PPOR_TR to '1'. Updated Vbias specification. Updated PCB Schematic. Updated Figure 8-1 and Figure 6-3. Updated Interrupt Vector table, Updated Sales links. Updated JTAG and SWD specifications. Removed Jp-p and Jperiod from ECO AC Spec table. Added note on sleep timer in Table 11-2. Updated ILO AC and DC specifications. Added Resolution parameter in VDAC and IDAC tables. Updated I_{OUT} typical and maximum values. Changed Temperature Sensor range to –40 °C to +85 °C. Removed Latchup specification from Table 11-1.