

Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3445axi-108t">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3445axi-108t</a>

## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP](#). Following is an abbreviated list for PSoC 3:

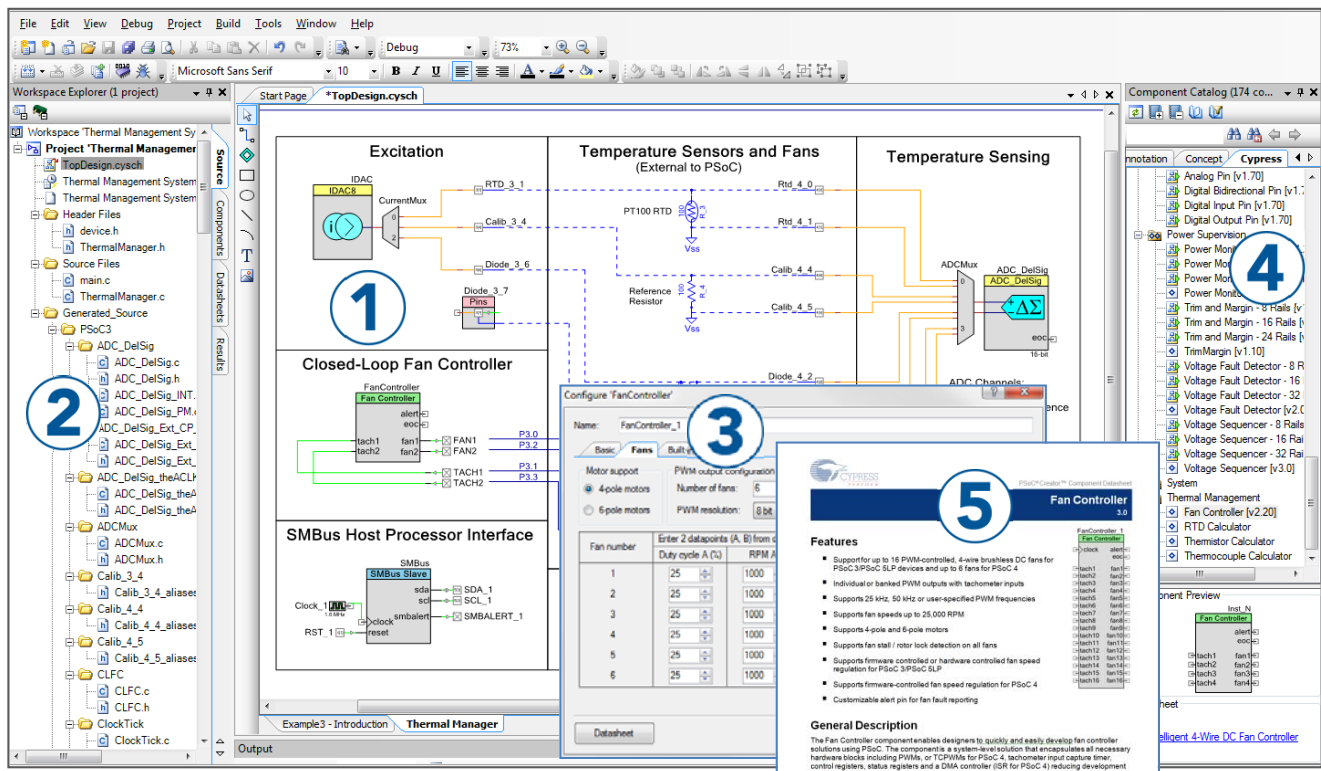
- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)  
In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes and [code examples](#) covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 3 are:
  - [AN54181: Getting Started With PSoC 3](#)
  - [AN61290: Hardware Design Considerations](#)
  - [AN57821: Mixed Signal Circuit Board Layout](#)
  - [AN58304: Pin Selection for Analog Designs](#)
  - [AN81623: Digital Design Best Practices](#)
  - [AN73854: Introduction To Bootloaders](#)
- Development Kits:
  - [CY8CKIT-030](#) is designed for analog performance, for developing high-precision analog, low-power, and low-voltage applications.
  - [CY8CKIT-001](#) provides a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.
  - The [MiniProg3](#) device provides an interface for flash programming and debug.
- Technical Reference Manuals (TRM)
  - [Architecture TRM](#)
  - [Registers TRM](#)
  - [Programming Specification](#)

## PSoC Creator

[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

**Figure 1. Multiple-Sensor Example Project in PSoC Creator**



In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C34 family these blocks can include four 16-bit timer, counter, and PWM blocks; I<sup>2</sup>C slave, master, and multi-master; Full-Speed USB; and Full CAN 2.0b.

For more details on the peripherals see the “[Example Peripherals](#)” section on page 43 of this data sheet. For information on UDBs, DSI, and other digital blocks, see the “[Digital Subsystem](#)” section on page 43 of this data sheet.

PSoC’s analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 1-percent error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Voltage references
- Analog-to-digital converter (ADC)
- Digital-to-analog converters (DACs)

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. The heart of the analog subsystem is a fast, accurate, configurable delta-sigma ADC with these features:

- Less than 100  $\mu$ V offset
- A gain error of 0.2 percent
- INL less than  $\pm 1$  LSB
- DNL less than  $\pm 1$  LSB
- SINAD better than 66 dB

This converter addresses a wide variety of precision analog applications, including some of the most demanding sensors.

Two high-speed voltage or current DACs support 8-bit output signals at update rate of 8 Msps in current DAC (IDAC) and 1 Msps in voltage DAC (VDAC). They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths.

In addition to the ADC and DACs, the analog subsystem provides multiple:

- Uncommitted opamps
- Configurable switched capacitor/continuous time (SC/CT) blocks. These support:
  - Transimpedance amplifiers
  - Programmable gain amplifiers
  - Mixers

- Other similar analog components

See the “[Analog Subsystem](#)” section on page 56 of this data sheet for more details.

PSoC’s 8051 CPU subsystem is built around a single cycle pipelined 8051 8-bit processor running at up to 50 MHz. The CPU subsystem includes a programmable nested vector interrupt controller, DMA controller, and RAM. PSoC’s nested vector interrupt controller provides low latency by allowing the CPU to vector directly to the first address of the interrupt service routine, bypassing the jump instruction required by other architectures. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor. The processor speed itself is configurable, allowing you to tune active power consumption for specific applications.

PSoC’s nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 64 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling bootloaders. You can enable an error correcting code (ECC) for high reliability applications. A powerful and flexible protection model secures the user’s sensitive information, allowing selective memory block locking for read and write protection. Up to 2 KB of byte-writeable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after power-on reset (POR).

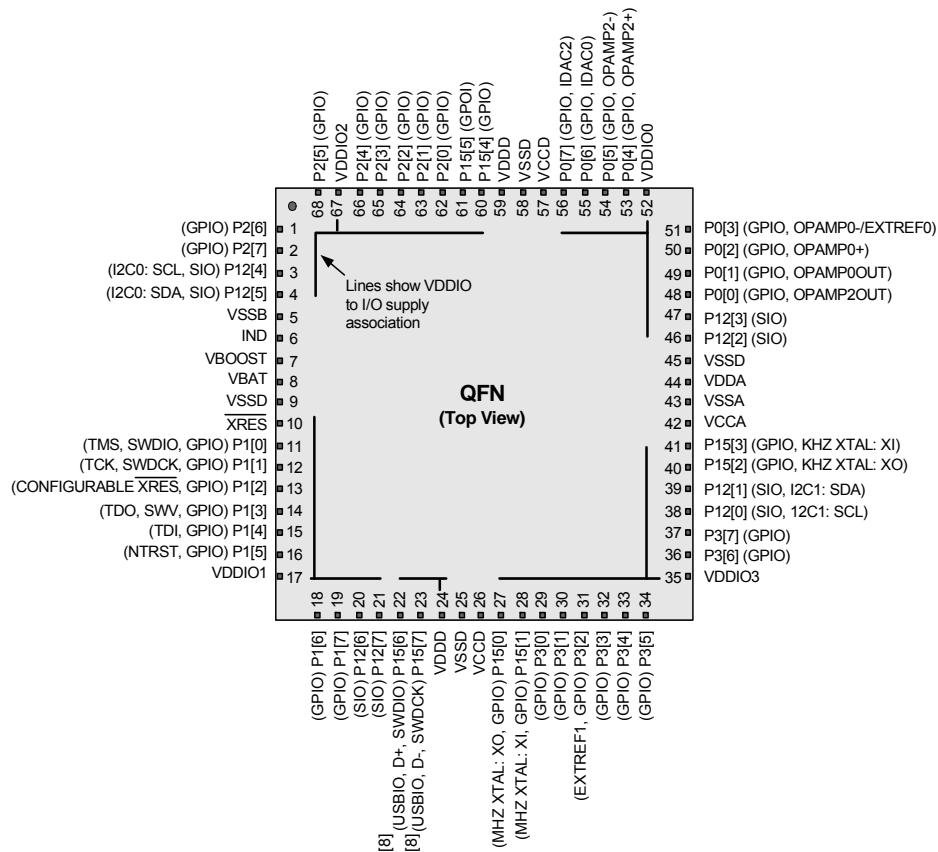
The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the VDDIO pins. Every GPIO has analog I/O, LCD drive<sup>[3]</sup>, CapSense<sup>[4]</sup>, flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow VOH to be set independently of VDDIO when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I<sup>2</sup>C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with Full-Speed USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All of the features of the PSoC I/Os are covered in detail in the “[I/O System and Routing](#)” section on page 36 of this data sheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The Internal Main Oscillator (IMO) is the clock base for the system, and has 2-percent accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 24 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs.

### Notes

3. This feature on select devices only. See [Ordering Information](#) on page 121 for details.
4. GPIOs with opamp outputs are not recommended for use with CapSense.

Figure 2-5. 68-Pin QFN Part Pinout<sup>[9]</sup>



## Notes

8. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
9. The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see [AN72845](#), Design Guidelines for QFN Devices.

## 4.3 Instruction Set

The 8051 instruction set is highly optimized for 8-bit handling and Boolean operations. The types of instructions supported include:

- Arithmetic instructions
- Logical instructions
- Data transfer instructions
- Boolean instructions
- Program branching instructions

### 4.3.1 Instruction Set Summary

#### 4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. [Table 4-1](#) lists the different arithmetic instructions.

**Table 4-1. Arithmetic Instructions**

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A,Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A,Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3



boost typically draws 250  $\mu\text{A}$  in active mode and 25  $\mu\text{A}$  in standby mode. The boost operating modes must be used in conjunction with chip power modes to minimize total power consumption. Table 6-4 lists the boost power modes available in different chip power modes.

**Table 6-4. Chip and Boost Power Modes Compatibility**

Chip Power Modes	Boost Power Modes
Chip-active or alternate active mode	Boost must be operated in its active mode.
Chip-sleep mode	Boost can be operated in either active or standby mode. In boost standby mode, the chip must wake up periodically for boost active-mode refresh.
Chip-hibernate mode	Boost can be operated in its active mode. However, it is recommended not to use the boost in chip hibernate mode due to the higher current consumption in boost active mode.

### 6.2.2.1 Boost Firmware Requirements

To ensure boost inrush current is within specification at startup, the **Enable Fast IMO During Startup** value must be unchecked in the PSoC Creator IDE. The **Enable Fast IMO During Startup** option is found in PSoC Creator in the design wide resources (cydwr) file **System** tab. Un-checking this option configures the device to run at 12 MHz vs 48 MHz during startup while configuring the device. The slower clock speed results in reduced current draw through the boost circuit.

### 6.2.2.2 Boost Design Process

Correct operation of the boost converter requires specific component values determined for each design's unique operating conditions. The  $C_{\text{BAT}}$  capacitor, Inductor, Schottky diode, and  $C_{\text{BOOST}}$  capacitor components are required with the values specified in the electrical specifications, Table 11-7 on page 77. The only variable component value is the inductor  $L_{\text{BOOST}}$  which is primarily sized for correct operation of the boost across operating conditions and secondarily for efficiency. Additional operating region constraints exist for  $V_{\text{OUT}}$ ,  $V_{\text{BAT}}$ ,  $I_{\text{OUT}}$ , and  $T_A$ .

The following steps must be followed to determine boost converter operating parameters and  $L_{\text{BOOST}}$  value.

1. Choose desired  $V_{\text{BAT}}$ ,  $V_{\text{OUT}}$ ,  $T_A$ , and  $I_{\text{OUT}}$  operating condition ranges for the application.
2. Determine if  $V_{\text{BAT}}$  and  $V_{\text{OUT}}$  ranges fit the boost operating range based on the  **$T_A$  range over  $V_{\text{BAT}}$  and  $V_{\text{OUT}}$**  chart, Figure 11-8 on page 77. If the operating ranges are not met,

modify the operating conditions or use an external boost regulator.

3. Determine if the desired ambient temperature ( $T_A$ ) range fits the ambient temperature operating range based on the  **$T_A$  range over  $V_{\text{BAT}}$  and  $V_{\text{OUT}}$**  chart, Figure 11-8 on page 77. If the temperature range is not met, modify the operating conditions and return to step 2, or use an external boost regulator.
4. Determine if the desired output current ( $I_{\text{OUT}}$ ) range fits the output current operating range based on the  **$I_{\text{OUT}}$  range over  $V_{\text{BAT}}$  and  $V_{\text{OUT}}$**  chart, Figure 11-9 on page 77. If the output current range is not met, modify the operating conditions and return to step 2, or use an external boost regulator.
5. Find the allowed inductor values based on the  **$L_{\text{BOOST}}$  values over  $V_{\text{BAT}}$  and  $V_{\text{OUT}}$**  chart, Figure 11-10 on page 77.
6. Based on the allowed inductor values, inductor dimensions, inductor cost, boost efficiency, and  $V_{\text{RIPPLE}}$  choose the optimum inductor value for the system. Boost efficiency and  $V_{\text{RIPPLE}}$  typical values are provided in the **Efficiency vs  $V_{\text{BAT}}$**  and  **$V_{\text{RIPPLE}}$  vs  $V_{\text{BAT}}$**  charts, Figure 11-11 on page 78 through Figure 11-14 on page 78. In general, if high efficiency and low  $V_{\text{RIPPLE}}$  are most important, then the highest allowed inductor value should be used. If low inductor cost or small inductor size are most important, then one of the smaller allowed inductor values should be used. If the allowed inductor(s) efficiency,  $V_{\text{RIPPLE}}$ , cost or dimensions are not acceptable for the application than an external boost regulator should be used.

## 6.3 Reset

CY8C34 has multiple internal and external reset sources available. The reset sources are:

- **Power source monitoring** – The analog and digital power voltages,  $V_{\text{DDA}}$ ,  $V_{\text{DDD}}$ ,  $V_{\text{CCA}}$ , and  $V_{\text{CCD}}$  are monitored in several different modes during power up, active mode, and sleep mode (buzzing). If any of the voltages goes outside predetermined ranges then a reset is generated. The monitors are programmable to generate an interrupt to the processor under certain conditions before reaching the reset thresholds.
- **External** – The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to  $V_{\text{DDIO1}}$ .  $V_{\text{DDD}}$ ,  $V_{\text{DDA}}$ , and  $V_{\text{DDIO1}}$  must all have voltage applied before the part comes out of reset.
- **Watchdog timer** – A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset.
- **Software** – The device can be reset under program control.

- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register

Independent of the ALU operation, these functions are available:

- Shift left
- Shift right
- Nibble swap
- Bitwise OR mask

### 7.2.2.3 Conditionals

Each datapath has two compares, with bit masking options. Compare operands include the two accumulators and the two data registers in a variety of configurations. Other conditions include zero detect, all ones detect, and overflow. These conditions are the primary datapath outputs, a selection of which can be driven out to the UDB routing matrix. Conditional computation can use the built in chaining to neighboring UDBs to operate on wider data widths without the need to use routing resources.

### 7.2.2.4 Variable MSB

The most significant bit of an arithmetic and shift function can be programmatically specified. This supports variable width CRC and PRS functions, and in conjunction with ALU output masking, can implement arbitrary width timers, counters and shift blocks.

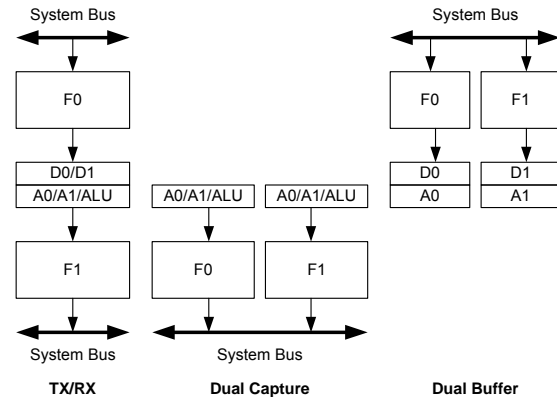
### 7.2.2.5 Built in CRC/PRS

The datapath has built in support for single cycle Cyclic Redundancy Check (CRC) computation and Pseudo Random Sequence (PRS) generation of arbitrary width and arbitrary polynomial. CRC/PRS functions longer than 8 bits may be implemented in conjunction with PLD logic, or built in chaining may be used to extend the function into neighboring UDBs.

### 7.2.2.6 Input/Output FIFOs

Each datapath contains two four-byte deep FIFOs, which can be independently configured as an input buffer (system bus writes to the FIFO, datapath internal reads the FIFO), or an output buffer (datapath internal writes to the FIFO, the system bus reads from the FIFO). The FIFOs generate status that are selectable as datapath outputs and can therefore be driven to the routing, to interact with sequencers, interrupts, or DMA.

**Figure 7-5. Example FIFO Configurations**



### 7.2.2.7 Chaining

The datapath can be configured to chain conditions and signals such as carries and shift data with neighboring datapaths to create higher precision arithmetic, shift, CRC/PRS functions.

### 7.2.2.8 Time Multiplexing

In applications that are over sampled, or do not need high clock rates, the single ALU block in the datapath can be efficiently shared with two sets of registers and condition generators. Carry and shift out data from the ALU are registered and can be selected as inputs in subsequent cycles. This provides support for 16-bit functions in one (8-bit) datapath.

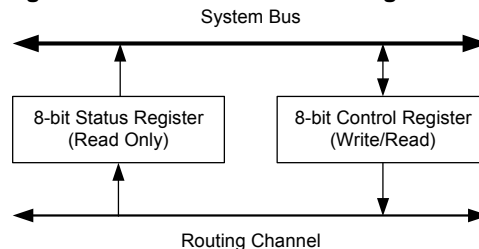
### 7.2.2.9 Datapath I/O

There are six inputs and six outputs that connect the datapath to the routing matrix. Inputs from the routing provide the configuration for the datapath operation to perform in each cycle, and the serial data inputs. Inputs can be routed from other UDB blocks, other device peripherals, device I/O pins, and so on. The outputs to the routing can be selected from the generated conditions, and the serial data outputs. Outputs can be routed to other UDB blocks, device peripherals, interrupt and DMA controller, I/O pins, and so on.

### 7.2.3 Status and Control Module

The primary purpose of this circuitry is to coordinate CPU firmware interaction with internal UDB operation.

**Figure 7-6. Status and Control Registers**



The bits of the control register, which may be written to by the system bus, are used to drive into the routing matrix, and thus provide firmware with the opportunity to control the state of UDB processing. The status register is read-only and it allows internal UDB state to be read out onto the system bus directly from internal routing. This allows firmware to monitor the state of UDB processing. Each bit of these registers has programmable connections to the routing matrix and routing connections are made depending on the requirements of the application.

## 7.2.3.1 Usage Examples

As an example of control input, a bit in the control register can be allocated as a function enable bit. There are multiple ways to enable a function. In one method the control bit output would be routed to the clock control block in one or more UDBs and serve as a clock enable for the selected UDB blocks. A status example is a case where a PLD or datapath block generated a condition, such as a “compare true” condition that is captured and latched by the status register and then read (and cleared) by CPU firmware.

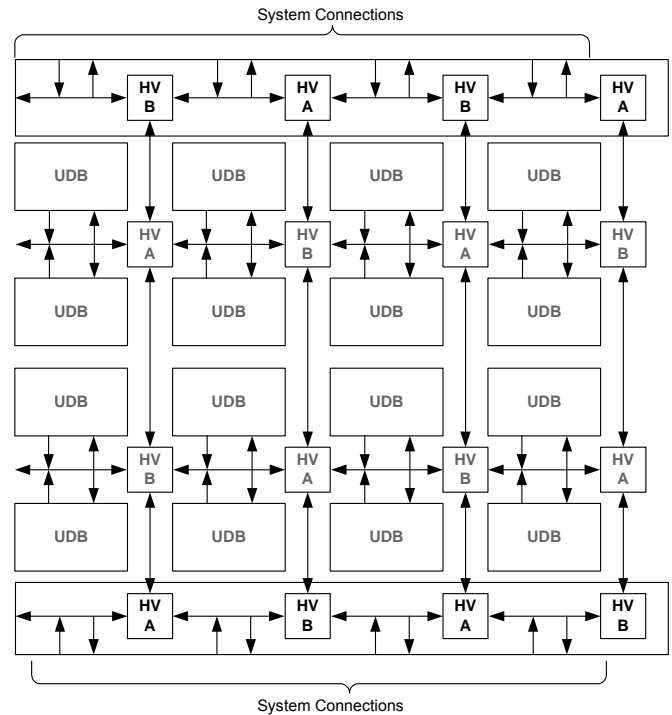
## 7.2.3.2 Clock Generation

Each subcomponent block of a UDB including the two PLDs, the datapath, and Status and Control, has a clock selection and control block. This promotes a fine granularity with respect to allocating clocking resources to UDB component blocks and allows unused UDB resources to be used by other functions for maximum system efficiency.

## 7.3 UDB Array Description

Figure 7-7 shows an example of a 16 UDB array. In addition to the array core, there are a DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

**Figure 7-7. Digital System Interface Structure**



### 7.3.1 UDB Array Programmable Resources

Figure 7-8 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit Timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.



## 8.3.2 LUT

The CY8C34 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

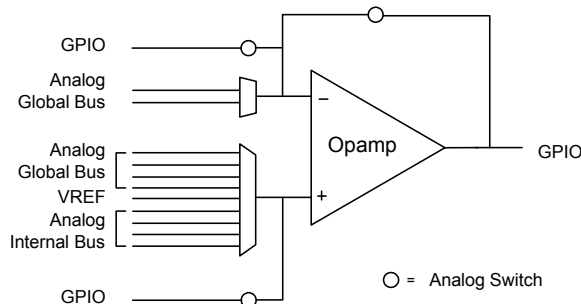
**Table 8-2. LUT Function vs. Program Word and Inputs**

Control Word	Output (A and B are LUT inputs)
0000b	FALSE ('0')
0001b	A AND B
0010b	A AND (NOT B)
0011b	A
0100b	(NOT A) AND B
0101b	B
0110b	A XOR B
0111b	A OR B
1000b	A NOR B
1001b	A XNOR B
1010b	NOT B
1011b	A OR (NOT B)
1100b	NOT A
1101b	(NOT A) OR B
1110b	A NAND B
1111b	TRUE ('1')

## 8.4 Opamps

The CY8C34 family of devices contains two general purpose opamps in a device.

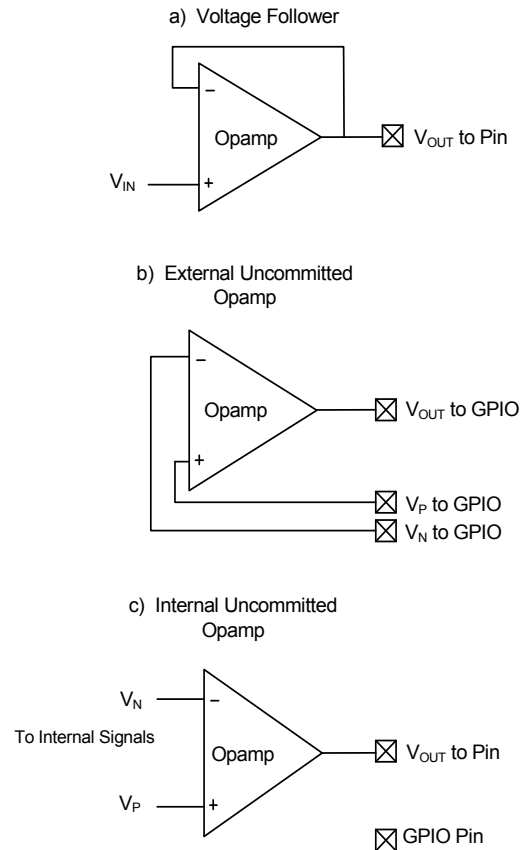
**Figure 8-6. Opamp**



The opamp is uncommitted and can be configured as a gain stage or voltage follower, or output buffer on external or internal signals.

See Figure 8-7. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

**Figure 8-7. Opamp Configurations**



The opamp has three speed modes, slow, medium, and fast. The slow mode consumes the least amount of quiescent power and the fast mode consumes the most power. The inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 25 mA) the output voltage may only get within 500 mV of the rails.

## 8.5 Programmable SC/CT Blocks

The CY8C34 family of devices contains two switched capacitor/continuous time (SC/CT) blocks in a device. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the  $V_{REF}$  TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

## 8.6 LCD Direct Drive

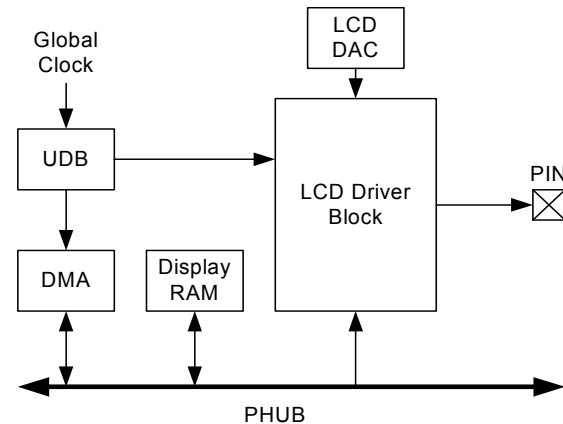
The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C34 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane × 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

**Figure 8-10. LCD System**



### 8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

### 8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers via DMA.

### 8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

### 8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

## 8.7 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a delta-sigma modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

## 8.8 Temp Sensor

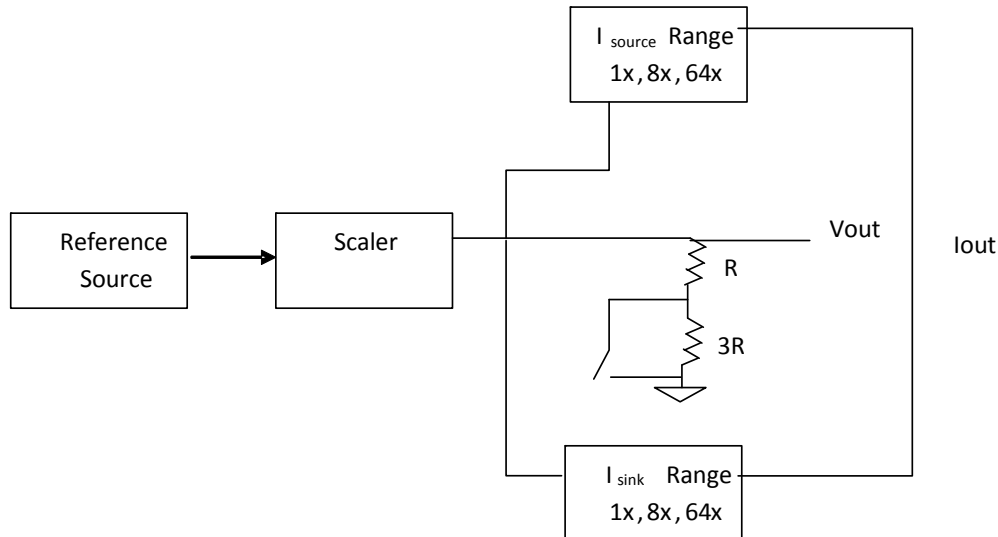
Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

## 8.9 DAC

The CY8C34 parts contain two Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features:

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct  $\pm 25$  percent of gain error
- Source and sink option for current output
- High and low speed / power modes
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-11. DAC Block Diagram



### 8.9.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875  $\mu$ A, 0 to 255  $\mu$ A, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

### 8.9.2 Voltage DAC

For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

## 8.10 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk - Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

## 11.3 Power Regulators

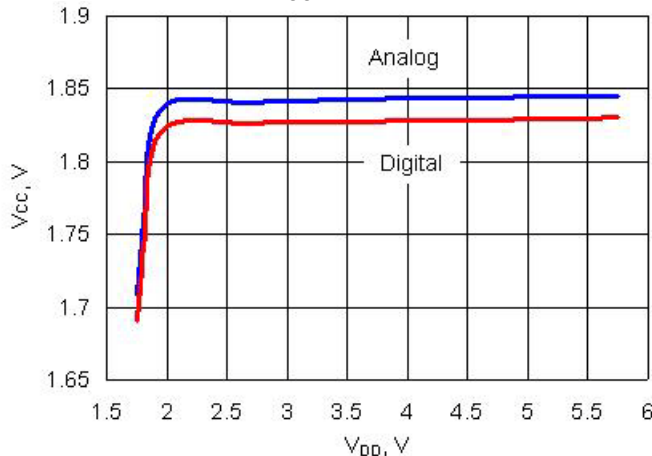
Specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$  and  $T_J \leq 100\text{ }^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

### 11.3.1 Digital Core Regulator

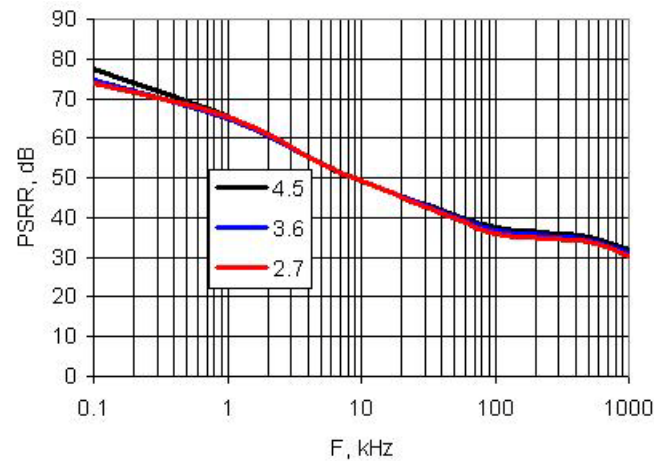
**Table 11-4. Digital Core Regulator DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$V_{DDD}$	Input voltage		1.8	–	5.5	V
$V_{CCD}$	Output voltage		–	1.80	–	V
	Regulator output capacitor	$\pm 10\%$ , X5R ceramic or better. The two $V_{CCD}$ pins must be shorted together, with as short a trace as possible, see <a href="#">Power System</a> on page 30	0.9	1	1.1	$\mu\text{F}$

**Figure 11-5. Regulators  $V_{CC}$  vs  $V_{DD}$**



**Figure 11-6. Digital Regulator PSRR vs Frequency and  $V_{DD}$**

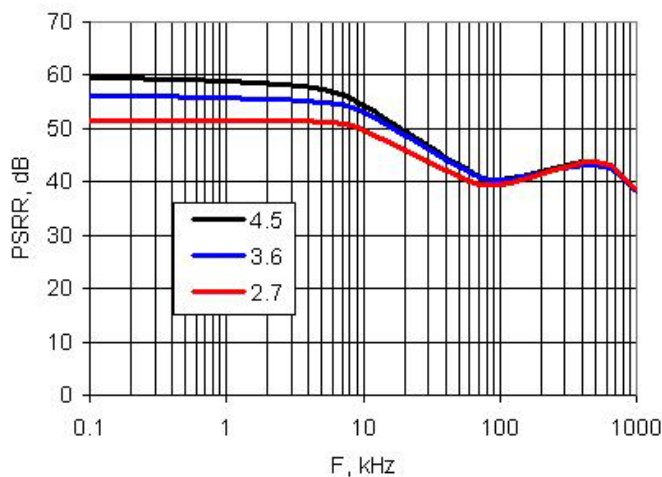


### 11.3.2 Analog Core Regulator

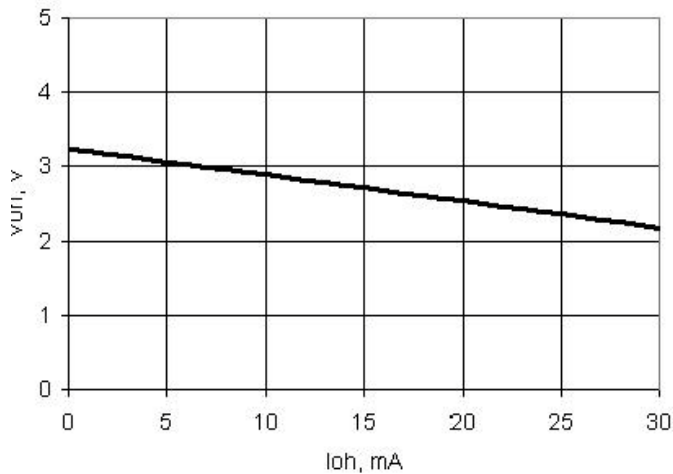
**Table 11-5. Analog Core Regulator DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$V_{DDA}$	Input voltage		1.8	–	5.5	V
$V_{CCA}$	Output voltage		–	1.80	–	V
	Regulator output capacitor	$\pm 10\%$ , X5R ceramic or better	0.9	1	1.1	$\mu\text{F}$

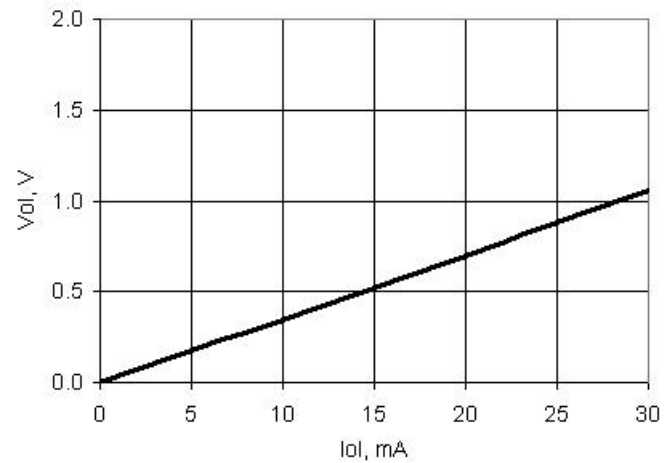
**Figure 11-7. Analog Regulator PSRR vs Frequency and  $V_{DD}$**



**Figure 11-22. USBIO Output High Voltage and Current, GPIO Mode**



**Figure 11-23. USBIO Output Low Voltage and Current, GPIO Mode**



**Table 11-15. USBIO AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
Td <sub>rate</sub>	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tj <sub>r1</sub>	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tj <sub>r2</sub>	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Td <sub>j1</sub>	Driver differential jitter to next transition		–3.5	–	3.5	ns
Td <sub>j2</sub>	Driver differential jitter to pair transition		–4	–	4	ns
Tf <sub>deop</sub>	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tf <sub>eo<sub>pt</sub></sub>	Source SE0 interval of EOP		160	–	175	ns
Tf <sub>eo<sub>pr</sub></sub>	Receiver SE0 interval of EOP		82	–	–	ns
Tf <sub>st</sub>	Width of SE0 interval during differential transition		–	–	14	ns
F <sub>gpio_out</sub>	GPIO mode output operating frequency	3 V ≤ V <sub>DD</sub> ≤ 5.5 V	–	–	20	MHz
		V <sub>DD</sub> = 1.71 V	–	–	6	MHz
Tr <sub>gpio</sub>	Rise time, GPIO mode, 10%/90% V <sub>DD</sub>	V <sub>DD</sub> > 3 V, 25 pF load	–	–	12	ns
		V <sub>DD</sub> = 1.71 V, 25 pF load	–	–	40	ns
Tf <sub>gpio</sub>	Fall time, GPIO mode, 90%/10% V <sub>DD</sub>	V <sub>DD</sub> > 3 V, 25 pF load	–	–	12	ns
		V <sub>DD</sub> = 1.71 V, 25 pF load	–	–	40	ns



#### 11.4.4 XRES

**Table 11-17. XRES DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
V <sub>IH</sub>	Input voltage high threshold		$0.7 \times V_{DDIO}$	–	–	V
V <sub>IL</sub>	Input voltage low threshold		–	–	$0.3 \times V_{DDIO}$	V
R <sub>pullup</sub>	Pull-up resistor		3.5	5.6	8.5	kΩ
C <sub>IN</sub>	Input capacitance <sup>[46]</sup>		–	3	–	pF
V <sub>H</sub>	Input voltage hysteresis (Schmitt-Trigger) <sup>[46]</sup>		–	100	–	mV
I <sub>diode</sub>	Current through protection diode to V <sub>DDIO</sub> and V <sub>SSIO</sub>		–	–	100	μA

**Table 11-18. XRES AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
T <sub>RESET</sub>	Reset pulse width		1	–	–	μs

**Note**

46. Based on device characterization (Not production tested).

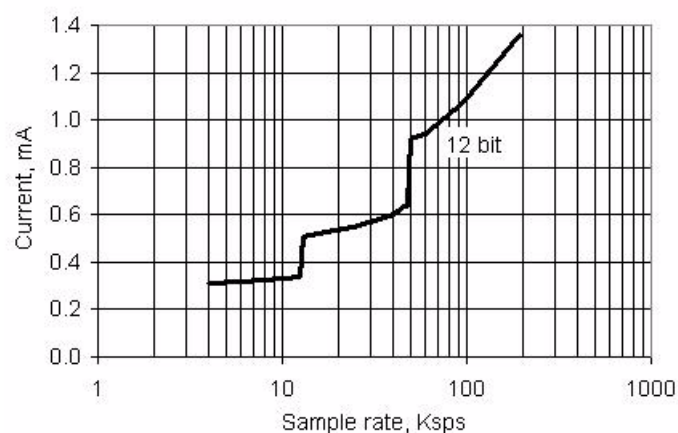
**Table 11-22. Delta-sigma ADC AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time		–	–	4	Samples
THD	Total harmonic distortion <sup>[51]</sup>	Buffer gain = 1, 12-bit, Range = $\pm 1.024$ V	–	–	0.0032	%
<b>12-Bit Resolution Mode</b>						
SR12	Sample rate, continuous, high power <sup>[51]</sup>	Range = $\pm 1.024$ V, unbuffered	4	–	192	ksps
BW12	Input bandwidth at max sample rate <sup>[51]</sup>	Range = $\pm 1.024$ V, unbuffered	–	44	–	kHz
SINAD12int	Signal to noise ratio, 12-bit, internal reference <sup>[51]</sup>	Range = $\pm 1.024$ V, unbuffered	66	–	–	dB
<b>8-Bit Resolution Mode</b>						
SR8	Sample rate, continuous, high power <sup>[51]</sup>	Range = $\pm 1.024$ V, unbuffered	8	–	384	ksps
BW8	Input bandwidth at max sample rate <sup>[51]</sup>	Range = $\pm 1.024$ V, unbuffered	–	88	–	kHz
SINAD8int	Signal to noise ratio, 8-bit, internal reference <sup>[51]</sup>	Range = $\pm 1.024$ V, unbuffered	43	–	–	dB

**Table 11-23. Delta-sigma ADC Sample Rates, Range =  $\pm 1.024$  V**

Resolution, Bits	Continuous		Multi-Sample	
	Min	Max	Min	Max
8	8000	384000	1911	91701
9	6400	307200	1543	74024
10	5566	267130	1348	64673
11	4741	227555	1154	55351
12	4000	192000	978	46900

**Figure 11-33. Delta-sigma ADC IDD vs sps, Range =  $\pm 1.024$  V, Continuous Sample Mode, Input Buffer Bypassed**



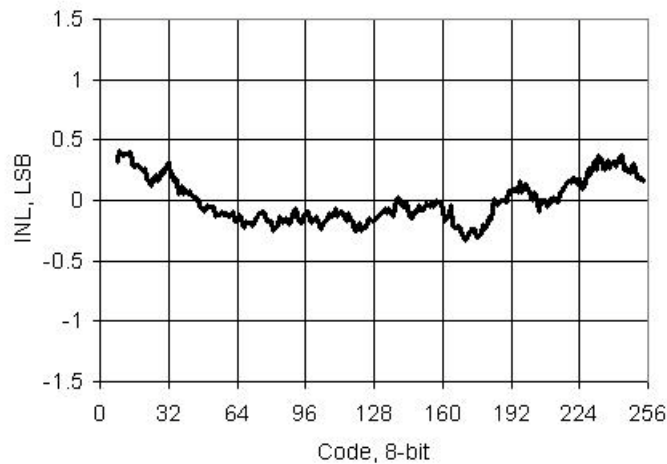
**Note**

51. Based on device characterization (Not production tested).

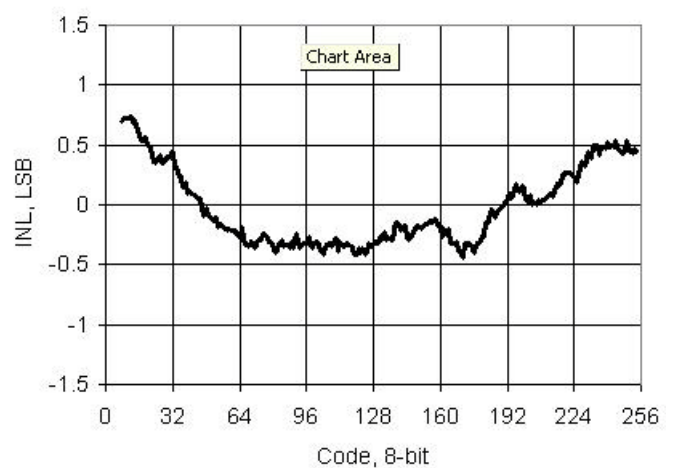
**Table 11-28. IDAC DC Specifications** (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
$I_{DD}$	Operating current, code = 0	Low speed mode, source mode, range = 31.875 $\mu$ A	–	44	100	$\mu$ A
		Low speed mode, source mode, range = 255 $\mu$ A,	–	33	100	$\mu$ A
		Low speed mode, source mode, range = 2.04 mA	–	33	100	$\mu$ A
		Low speed mode, sink mode, range = 31.875 $\mu$ A	–	36	100	$\mu$ A
		Low speed mode, sink mode, range = 255 $\mu$ A	–	33	100	$\mu$ A
		Low speed mode, sink mode, range = 2.04 mA	–	33	100	$\mu$ A
		High speed mode, source mode, range = 31.875 $\mu$ A	–	310	500	$\mu$ A
		High speed mode, source mode, range = 255 $\mu$ A	–	305	500	$\mu$ A
		High speed mode, source mode, range = 2.04 mA	–	305	500	$\mu$ A
		High speed mode, sink mode, range = 31.875 $\mu$ A	–	310	500	$\mu$ A
		High speed mode, sink mode, range = 255 $\mu$ A	–	300	500	$\mu$ A
		High speed mode, sink mode, range = 2.04 mA	–	300	500	$\mu$ A

**Figure 11-34. IDAC INL vs Input Code, Range = 255  $\mu$ A, Source Mode**



**Figure 11-35. IDAC INL vs Input Code, Range = 255  $\mu$ A, Sink Mode**



#### 11.9.5 External Clock Reference

**Table 11-81. External Clock Reference AC Specifications<sup>[76]</sup>**

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at $V_{DDIO}/2$	30	50	70	%
	Input edge rate	$V_{IL}$ to $V_{IH}$	0.5	–	–	V/ns

#### 11.9.6 Phase-Locked Loop

**Table 11-82. PLL DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$I_{DD}$	PLL operating current	In = 3 MHz, Out = 24 MHz	–	200	–	μA

**Table 11-83. PLL AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
F <sub>PLLIN</sub>	PLL input frequency <sup>[77]</sup>		1	–	48	MHz
	PLL intermediate frequency <sup>[78]</sup>	Output of prescaler	1	–	3	MHz
F <sub>PLLOUT</sub>	PLL output frequency <sup>[77]</sup>		24	–	50	MHz
	Lock time at startup		–	–	250	μs
J <sub>period-rms</sub>	Jitter (rms) <sup>[76]</sup>		–	–	250	ps

#### Notes

76. Based on device characterization (Not production tested).

77. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.

78. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

**Table 14-1. Acronyms Used in this Document** *(continued)*

Acronym	Description
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise low-voltage reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion

**Table 14-1. Acronyms Used in this Document** *(continued)*

Acronym	Description
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

## 15. Reference Documents

[PSoC® 3, PSoC® 5 Architecture TRM](#)

[PSoC® 3 Registers TRM](#)



## 17. Revision History

Description Title: PSoC® 3: CY8C34 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-53304				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	2714270	06/03/09	VVSK	New data sheet
*A	2758970	09/02/09	MKEA	Updated Part Numbering Conventions Added Section 11.7.5 (EMIF Figures and Tables) Updated GPIO and SIO AC specifications Updated XRES Pin Description and Xdata Address Map specifications Updated DFB and Comparator specifications Updated PHUB features section and RTC in sleep mode Updated IDAC and VDAC DC and Analog Global specifications Updated USBIO AC and Delta Sigma ADC specifications Updated PPOR and Voltage Monitors DC specifications Updated Drive Mode diagram Added 48-QFN Information Updated other electrical specifications
*B	2824546	12/09/09	MKEA	Updated I2C section to reflect 1 Mbps. Updated Table 11-6 and 11-7 (Boost AC and DC specs); also added Schottky Diode specs. Changed current for sleep/hibernate mode to include SIO; Added footnote to analog global specs. Updated Figures 1-1, 6-2, 7-14, and 8-1. Updated Table 6-2 and Table 6-3 (Hibernate and Sleep rows) and Power Modes section. Updated GPIO and SIO AC specifications. Updated Gain error in IDAC and VDAC specifications. Updated description of $V_{DDA}$ spec in Table 11-1 and removed GPIO Clamp Current parameter. Updated number of UDBs on page 1. Moved FILO from ILO DC to AC table. Added PCB Layout and PCB Schematic diagrams. Updated Fgpioout spec (Table 11-9). Added duty cycle frequency in PLL AC spec table. Added note for Sleep and Hibernate modes and Active Mode specs in Table 11-2. Linked URL in Section 10.3 to PSoC Creator site. Updated Ja and Jc values in Table 13-1. Updated Single Sample Mode and Fast FIR Mode sections. Updated Input Resistance specification in Del-Sig ADC table. Added Tio_init parameter. Updated PGA and UGB AC Specs. Removed SPC ADC. Updated Boost Converter section. Added section 'SIO as Comparator'; updated Hysteresis spec (differential mode) in Table 11-10. Updated $V_{BAT}$ condition and deleted Vstart parameter in Table 11-6. Added 'Bytes' column for Tables 4-1 to 4-5.
*C	2873322	02/04/10	MKEA	Changed maximum value of PPOR_TR to '1'. Updated Vbias specification. Updated PCB Schematic. Updated Figure 8-1 and Figure 6-3. Updated Interrupt Vector table, Updated Sales links. Updated JTAG and SWD specifications. Removed Jp-p and Jperiod from ECO AC Spec table. Added note on sleep timer in Table 11-2. Updated ILO AC and DC specifications. Added Resolution parameter in VDAC and IDAC tables. Updated $I_{OUT}$ typical and maximum values. Changed Temperature Sensor range to -40 °C to +85 °C. Removed Latchup specification from Table 11-1.

**Description Title: PSoC® 3: CY8C34 Family Datasheet Programmable System-on-Chip (PSoC®) (continued)**  
**Document Number: 001-53304**

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*J	3179219	02/22/2011	MKEA	Updated conditions for flash data retention time. Updated 100-pin TQFP package spec. Updated EEPROM AC specifications.
*K	3200146	03/28/2011	MKEA	Removed Preliminary status from the data sheet. Updated JTAG ID Deleted Cin_G1, ADC input capacitance from Delta-Sigma ADC DC spec table Updated JTAG Interface AC Specifications and SWD Interface Specifications tables Updated USBIO DC specs Added 0.01 to max speed Updated Features on page 1 Added Section 5.5, Nonvolatile Latches Updated Flash AC specs Added CAN DC specs Updated delta-sigma graphs, noise histogram figures and RMS Noise spec tables Add reference to application note AN58304 in section 8.1 Updated 100-pin TQFP package spec Added oscillator, I/O, VDAC, regulator graphs Updated JTAG/SWD timing diagrams Updated GPIO and SIO AC specs Updated POR with Brown Out AC spec table Updated IDAC graphs Added DMA timing diagram, interrupt timing and interrupt vector, I2C timing diagrams Updated opamp graphs and PGA graphs Added full chip performance graphs Changed MHzECO range. Added "Solder Reflow Peak Temperature" table.
*L	3259185	05/17/2011	MKEA	Added JTAG and SWD interface connection diagrams Updated T <sub>JA</sub> and T <sub>JC</sub> values in Table 13-1 Changed typ and max values for the TCVo <sub>s</sub> parameter in Opamp DC specifications table. Updated Clocking subsystem diagram. Changed VSSD to VSSB in the PSoC Power System diagram Updated Ordering information.

**Description Title: PSoC® 3: CY8C34 Family Datasheet Programmable System-on-Chip (PSoC®) (continued)**  
**Document Number: 001-53304**

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*P	3732521	09/03/2012	MKEA	<p>Replaced I<sub>DDDR</sub> and I<sub>DDAR</sub> specs in <a href="#">Table 11-2, “DC Specifications,”</a> on page 71 that were dropped out in *N revision.</p> <p>Updated <a href="#">Table 11-32, “Mixer DC Specifications,”</a> on page 102, V<sub>OS</sub> Max value from 10 to 15.</p> <p>Updated <a href="#">Table 11-21, “12-bit Delta-sigma ADC DC Specifications,”</a> on page 91, I<sub>DD 12</sub> Max value from 1.4 to 1.95 mA</p> <p>Replaced PSoC® 3 Programming AN62391 with TRM in footnote #59 and <a href="#">Section Table 9., “Programming, Debug Interfaces, Resources,”</a> on page 65</p> <p>Removed Figure 11-8 (Efficiency vs Vout)</p> <p>Removed 62-MHz sub-row in <a href="#">Table 11-2, “DC Specifications,”</a> on page 71</p> <p>Updated <a href="#">Table 11-19, “Opamp DC Specifications,”</a> on page 88, I<sub>DD</sub> Quiescent current row values from 200 and 270 to 250 and 400 respectively.</p> <p>Updated conditions for Storage Temperature in <a href="#">Table 11-1, “Absolute Maximum Ratings DC Specifications[18],”</a> on page 70</p> <p>Updated conditions and min values for NVL data retention time in <a href="#">Table 11-58, “NVL AC Specifications,”</a> on page 109.</p> <p>Updated <a href="#">Table 11-75, “ILO DC Specifications,”</a> on page 118.</p> <p>Removed following pruned parts from “<a href="#">Ordering Information</a>” section on page 121.</p> <p>CY8C3444AXI-116</p> <p>CY8C3445LTI-089</p> <p>CY8C3446AXI-105</p> <p>CY8C3446LTI-083</p> <p>CY8C3446PVI-091</p> <p>CY8C3446PVI-102</p> <p>Updated PSoC 3 boost circuit value throughout the document.</p> <p>Updated package diagram 51-85061 to *F revision.</p>
*Q	3922905	03/06/2013	MKEA	<p>Updated I<sub>DD XX</sub> parameters under <a href="#">Table 11-21, “12-bit Delta-sigma ADC DC Specifications,”</a> on page 91.</p> <p>Updated <a href="#">I<sup>2</sup>C</a> section and updated GPIO and SIO DC specification tables.</p>
*R	4064707	07/18/2013	MKEA	<p>Added USB test ID in <a href="#">Features</a>.</p> <p>Updated schematic in <a href="#">Section 2</a>.</p> <p>Added paragraph for device reset warning in <a href="#">Section 5.4</a>.</p> <p>Added NVL bit for DEBUG_EN in <a href="#">Section 5.5</a>.</p> <p>Updated UDB PLD array diagram in <a href="#">Section 7.2.1</a>.</p> <p>Changed Tstartup specs in <a href="#">Section 11.2.1</a>.</p> <p>Changed GPIO rise and fall time specs in <a href="#">Section 11.4</a>.</p> <p>Added Opamp IIB spec in <a href="#">Section 11.5.1</a>.</p> <p>Added IMO spec condition: pre-assembly in <a href="#">Section 11.9.1</a>.</p> <p>Added Appendix for CSP package (preliminary)</p>
*S	4118845	09/10/2013	MKEA	<p>Removed T<sub>STG</sub> spec and added note clarifying the maximum storage temperature range in <a href="#">Table 11-1</a>.</p> <p>Updated Vos spec conditions and TCVo<sub>s</sub> in <a href="#">Table 11-21</a>.</p> <p>Updated 100-TQFP package diagram.</p>
*T	4188568	11/14/2013	MKEA	<p>Updated delta-sigma Vos spec conditions.</p> <p>Added SIO Comparator specifications.</p>
*U	4385782	05/21/2014	MKEA	<p>Updated <a href="#">General Description</a> and <a href="#">Features</a>.</p> <p>Added <a href="#">More Information</a> and <a href="#">PSoC Creator</a> sections.</p> <p>Updated 100-pin TQFP package diagram.</p>