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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3445pvi-094t

4.3 Instruction Set

The 8051 instruction set is highly optimized for 8-bit handling and Boolean operations. The types of instructions supported include:

- Arithmetic instructions
- Logical instructions
- Data transfer instructions
- Boolean instructions
- Program branching instructions

4.3.1 Instruction Set Summary

4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. Table 4-1 lists the different arithmetic instructions.

Table 4-1. Arithmetic Instructions

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A,Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A,Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3

The CY8C34 family provides the standard set of registers found on industry standard 8051 devices. In addition, the CY8C34 devices add SFRs to provide direct access to the I/O ports on the device. The following sections describe the SFRs added to the CY8C34 family.

5.7.4 XData Space Access SFRs

The 8051 core features dual DPTR registers for faster data transfer operations. The data pointer select SFR, DPS, selects which data pointer register, DPTR0 or DPTR1, is used for the following instructions:

- MOVX @DPTR, A
- MOVX A, @DPTR
- MOVC A, @A+DPTR
- JMP @A+DPTR
- INC DPTR
- MOV DPTR, #data16

The extended data pointer SFRs, DPX0, DPX1, MXAX, and P2AX, hold the most significant parts of memory addresses during access to the xdata space. These SFRs are used only with the MOVX instructions.

During a MOVX instruction using the DPTR0/DPTR1 register, the most significant byte of the address is always equal to the contents of DPX0/DPX1. During a MOVX instruction using the R0 or R1 register, the most significant byte of the address is always equal to the contents of MXAX, and the next most significant byte is always equal to the contents of P2AX.

5.7.5 I/O Port SFRs

The I/O ports provide digital input sensing, output drive, pin interrupts, connectivity for analog inputs and outputs, LCD, and access to peripherals through the DSI. Full information on I/O ports is found in I/O System and Routing on page 36.

I/O ports are linked to the CPU through the PHUB and are also available in the SFRs. Using the SFRs allows faster access to a limited set of I/O port registers, while using the PHUB allows boot configuration and access to all I/O port registers.

Each SFR supported I/O port provides three SFRs:

- SFRPRTxDR sets the output data state of the port (where x is port number and includes ports 0-6, 12 and 15)
- The SFRPRTxSEL selects whether the PHUB PRTxDR register or the SFRPRTxDR controls each pin's output buffer within the port. If a SFRPRTxSEL[y] bit is high, the corresponding SFRPRTxDR[y] bit sets the output state for that pin. If a SFRPRTxSEL[y] bit is low, the corresponding PRTxDR[y] bit sets the output state of the pin (where y varies from 0 to 7).
- The SFRPRTxPS is a read only register that contains pin state values of the port pins.

5.7.5.1 xdata Space

The 8051 xdata space is 24-bit, or 16 MB in size. The majority of this space is not "external"—it is used by on-chip components. See Table 5-5. External, that is, off-chip, memory can be accessed using the EMIF. See External Memory Interface on page 24.

Table 5-5. XDATA Data Address Map

Address Range	Purpose
0×00 0000 – 0×00 1FFF	SRAM
0×00 4000 – 0×00 42FF	Clocking, PLLs, and oscillators
0×00 4300 – 0×00 43FF	Power management
0×00 4400 – 0×00 44FF	Interrupt controller
0×00 4500 – 0×00 45FF	Ports interrupt control
0×00 4700 – 0×00 47FF	Flash programming interface
0×00 4800 - 0×00 48FF	Cache controller
0×00 4900 – 0×00 49FF	I^2C controller
0×00 4E00 – 0×00 4EFF	Decimator
0×00 4F00 – 0×00 4FFF	Fixed timer/counter/PWMs
0×00 5000 – 0×00 51FF	I/O ports control
0×00 5400 – 0×00 54FF	External Memory Interface (EMIF) control registers
0×00 5800 – 0×00 5FFF	Analog Subsystem interface
0×00 6000 – 0×00 60FF	USB controller
0×00 6400 – 0×00 6FFF	UDB Working Registers
0×00 7000 – 0×00 7FFF	PHUB configuration
0×00 8000 – 0×00 8FFF	EEPROM
0×00 A000 – 0×00 A400	CAN
0×01 0000 – 0×01 FFFF	Digital Interconnect configuration
0×05 0220 – 0×05 02F0	Debug controller
0×08 0000 – 0×08 1FFF	Flash ECC bytes
0×80 0000 – 0×FF FFFF	External Memory Interface

debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low-power mode. Firmware can reset the central timewheel. Systems that require accurate timing should use the RTC capability instead of the central timewheel.

The 100-kHz clock (CLK100K) can be used as a low power master clock. It can also generate time intervals using the fast timewheel.

The fast timewheel is a 5-bit counter, clocked by the 100-kHz clock. It features programmable settings and automatically resets when the terminal count is reached. An optional interrupt can be generated each time the terminal count is reached. This enables flexible, periodic interrupts of the CPU at a higher rate than is allowed using the central timewheel.

The 33 kHz clock (CLK33K) comes from a divide-by-3 operation on CLK100K. This output can be used as a reduced accuracy version of the 32.768-kHz ECO clock with no need for a crystal.

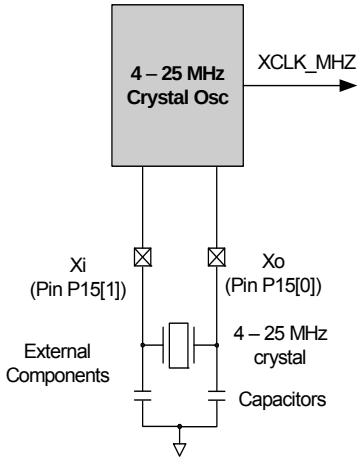
6.1.2 External Oscillators

Figure 6-1 shows that there are two external oscillators. They can be routed directly or divided. The direct routes may not have a 50% duty cycle. Divided clocks have a 50% duty cycle.

6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see Figure 6-2). It supports a wide variety of crystal types, in the range of 4 to 25 MHz. When used in conjunction with the PLL, it can generate other clocks up to the device's maximum frequency (see "Phase-Locked Loop" section on page 28). The GPIO pins connecting to the external crystal and capacitors are fixed. MHzECO accuracy depends on the crystal chosen.

Figure 6-2. MHzECO Block Diagram

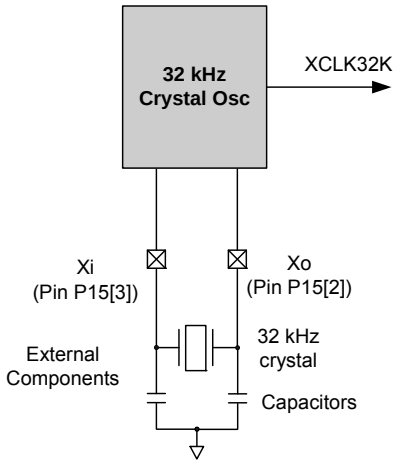


6.1.2.2 32.768-kHz ECO

The 32.768-kHz External Crystal Oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768-kHz watch crystal (see Figure 6-3). The 32kHzECO also connects directly to the sleep timer and provides the source for the RTC. The RTC uses a 1-second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance, CL1CL2 / (CL1 + CL2), including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators. See also pin capacitance specifications in the "GPIO" section on page 79.

6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and Universal Digital Blocks.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The master clock is used to select and supply the fastest clock in the system for general clock requirements and clock synchronization of the PSoC device.
- Bus Clock 16-bit divider uses the master clock to generate the bus clock used for data transfers. Bus clock is the source clock for the CPU clock divider.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks

The USBIO pins (P15[7] and P15[6]), when enabled for I/O mode, have limited drive mode control. The drive mode is set using the PRT15.DM0[7, 6] register. A resistive pull option is also available at the USBIO pins, which can be enabled using the PRT15.DM1[7, 6] register. When enabled for USB mode, the drive mode control has no impact on the configuration of the USB pins. Unlike the GPIO and SIO configurations, the port wide configuration registers do not configure the USB drive mode bits. Table 6-7 shows the drive mode configuration for the USBIO pins.

Table 6-7. USBIO Drive Modes (P15[7] and P15[6])

PRT15.DM1[7,6] Pull up enable	PRT15.DM0[7,6] Drive Mode enable	PRT15.DR[7,6] = 1	PRT15.DR[7,6] = 0	Description
0	0	High Z	Strong Low	Open Drain, Strong Low
0	1	Strong High	Strong Low	Strong Outputs
1	0	Res High (5k)	Strong Low	Resistive Pull Up, Strong Low
1	1	Strong High	Strong Low	Strong Outputs

- High impedance analog

  The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

  To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

- High impedance digital

  The input buffer is enabled for digital signal input. This is the standard high impedance (High Z) state recommended for digital inputs.

- Resistive pull-up or resistive pull-down

  Resistive pull-up or pull-down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

- Open drain, drives high and open drain, drives low

  Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I^2C bus signal lines.

- Strong drive

  Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

- Resistive pull-up and pull-down

  Similar to the resistive pull-up and resistive pull-down modes except the pin is always in series with a resistor. The high data state is pull-up while the low data state is pull-down. This mode is most often used when other signals that may cause shorts can drive the bus. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

6.4.3 Bidirectional Mode

High-speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRT×DM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRTxSLW registers.

11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 30	0.9	1	1.1	µF

Figure 11-5. Regulators V_{CC} vs V_{DD}

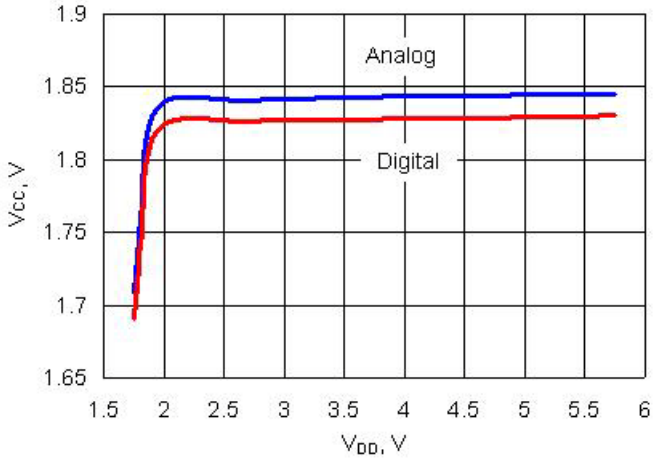
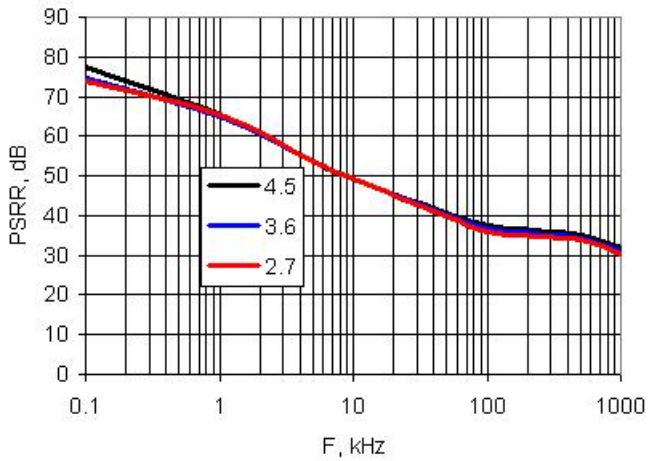


Figure 11-6. Digital Regulator PSRR vs Frequency and V_{DD}

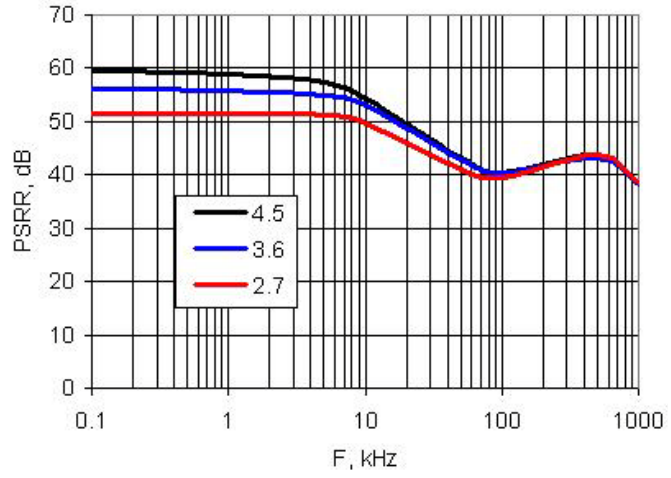


11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better	0.9	1	1.1	µF

Figure 11-7. Analog Regulator PSRR vs Frequency and V_{DD}



11.4 Inputs and Outputs

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

When the power supplies ramp up, there are low-impedance connections between each GPIO pin and its V_{DDIO} supply. This causes the pin voltages to track V_{DDIO} until both V_{DDIO} and V_{DDA} reach the IPOR voltage, which can be as high as 1.45 V. At that point, the low-impedance connections no longer exist and the pins change to their normal NVL settings.

11.4.1 GPIO

Table 11-9. GPIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold	CMOS Input, PRT[×]CTL = 0	0.7 × V_{DDIO}	–	–	V
V_{IL}	Input voltage low threshold	CMOS Input, PRT[×]CTL = 0	–	–	0.3 × V_{DDIO}	V
V_{IH}	Input voltage high threshold	LVTTL Input, PRT[×]CTL = 1,V_{DDIO} < 2.7 V	0.7 × V_{DDIO}	–	–	V
V_{IH}	Input voltage high threshold	LVTTL Input, PRT[×]CTL = 1, V_{DDIO} ≥ 2.7V	2.0	–	–	V
V_{IL}	Input voltage low threshold	LVTTL Input, PRT[×]CTL = 1,V_{DDIO} < 2.7 V	–	–	0.3 × V_{DDIO}	V
V_{IL}	Input voltage low threshold	LVTTL Input, PRT[×]CTL = 1, V_{DDIO} ≥ 2.7V	–	–	0.8	V
V_{OH}	Output voltage high	I_{OH} = 4 mA at 3.3 V_{DDIO}	V_{DDIO} – 0.6	–	–	V
		I_{OH} = 1 mA at 1.8 V_{DDIO}	V_{DDIO} – 0.5	–	–	V
V_{OL}	Output voltage low	I_{OL} = 8 mA at 3.3 V_{DDIO}	–	–	0.6	V
		I_{OL} = 4 mA at 1.8 V_{DDIO}	–	–	0.6	V
		I_{OL} = 3 mA at 3.3 V_{DDIO}	–	–	0.4	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull-down resistor		3.5	5.6	8.5	kΩ
I_{IL}	Input leakage current (absolute value)[39]	25 °C, V_{DDIO} = 3.0 V	–	–	2	nA
C_{IN}	Input capacitance[39]	GPIOs not shared with opamp outputs, MHz ECO or kHzECO	–	4	7	pF
		GPIOs shared with MHz ECO or kHzECO[40]	–	5	7	pF
		GPIOs shared with opamp outputs	–	–	18	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[39]		–	40	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	µA
Rglobal	Resistance pin to analog global bus	25 °C, V_{DDIO} = 3.0 V	–	320	–	Ω
Rmux	Resistance pin to analog mux bus	25 °C, V_{DDIO} = 3.0 V	–	220	–	Ω

Notes
39. Based on device characterization (Not production tested).
40. For information on designing with PSoC oscillators, refer to the application note, AN54439 - PSoC® 3 and PSoC 5 External Oscillator.

Table 11-13. SIO Comparator Specifications[45]

Parameter	Description	Conditions	Min	Typ	Max	Units
Vos	Offset voltage	V_{DDIO} = 2 V	–	–	68	mV
		V_{DDIO} = 2.7 V	–	–	72	
		V_{DDIO} = 5.5 V	–	–	82	
TCVos	Offset voltage drift with temp		–	–	250	µV/°C
CMRR	Common mode rejection ratio	V_{DDIO} = 2 V	30	–	–	dB
		V_{DDIO} = 2.7 V	35	–	–	
		V_{DDIO} = 5.5 V	40	–	–	
Tresp	Response time		–	–	30	ns

11.4.3 USBIO

For operation in GPIO mode, the standard range for V_{DDD} applies, see Device Level Specifications on page 71.

Table 11-14. USBIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high	15 kΩ ±5% to V_{SS}, internal pull-up enabled	2.8	–	3.6	V
Volusb	Static output low	15 kΩ ±5% to V_{SS}, internal pull-up enabled	–	–	0.3	V
Vihgpio	Input voltage high, GPIO mode	$V_{DDD} \geq 3$ V	2	–	–	V
Vilgpio	Input voltage low, GPIO mode	$V_{DDD} \geq 3$ V	–	–	0.8	V
Vohgpio	Output voltage high, GPIO mode	I_{OH} = 4 mA, $V_{DDD} \geq 3$ V	2.4	–	–	V
Volgpio	Output voltage low, GPIO mode	I_{OL} = 4 mA, $V_{DDD} \geq 3$ V	–	–	0.3	V
Vdi	Differential input sensitivity	|(D+) – (D–)|	–	–	0.2	V
Vcm	Differential input common mode range		0.8	–	2.5	V
Vse	Single ended receiver threshold		0.8	–	2	V
Rps2	PS/2 pull-up resistance	In PS/2 mode, with PS/2 pull-up enabled	3	–	7	kΩ
Rext	External USB series resistor	In series with each USB pin	21.78 (–1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance	Including Rext	28	–	44	Ω
C_{IN}	USB transceiver input capacitance		–	–	20	pF
I_{IL}[45]	Input leakage current (absolute value)	25 °C, V_{DDD} = 3.0 V	–	–	2	nA

Note
45. Based on device characterization (Not production tested).

11.5.2 Delta-sigma ADC

Unless otherwise specified, operating conditions are:

- Operation in continuous sample mode
- fclk = 6.144 MHz
- Reference = 1.024 V internal reference bypassed on P3.2 or P0.3
- Unless otherwise specified, all charts and graphs show typical values

Table 11-21. 12-bit Delta-sigma ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		8	–	12	bits
	Number of channels, single ended		–	–	No. of GPIO	–
	Number of channels, differential	Differential pair is formed using a pair of GPIOs.	–	–	No. of GPIO/2	–
	Monotonic	Yes	–	–	–	–
Ge	Gain error	Buffered, buffer gain = 1, Range = ±1.024 V, 25 °C	–	–	±0.2	%
Gd	Gain drift	Buffered, buffer gain = 1, Range = ±1.024 V	–	–	50	ppm/°C
Vos	Input offset voltage	Buffered, 12-bit mode	–	–	±0.1	mV
TCVos	Temperature coefficient, input offset voltage	Buffer gain = 1, 12-bit, Range = ±1.024 V	–	–	1	µV/°C
	Input voltage range, single ended[48]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential unbuffered[48]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential, buffered[48]		V_{SSA}	–	V_{DDA} – 1	V
INL12	Integral non linearity[48]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL12	Differential non linearity[48]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL8	Integral non linearity[48]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL8	Differential non linearity[48]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
Rin_Buff	ADC input resistance	Input buffer used	10	–	–	MΩ
Rin_ADC12	ADC input resistance	Input buffer bypassed, 12 bit, Range = ±1.024 V	–	148[49]	–	kΩ
Rin_ExtRef	ADC external reference input resistance		–	70[49, 50]	–	kΩ
Vextref	ADC external reference input voltage, see also internal reference in Voltage Reference on page 93	Pins P0[3], P3[2]	0.9	–	1.3	V
Current Consumption						
I_{DD_12}	I_{DDA} + I_{DDD} current consumption, 12 bit[48]	192 ksps, unbuffered	–	–	1.95	mA
I_{BUFF}	Buffer current consumption[48]		–	–	2.5	mA

Notes

48. Based on device characterization (Not production tested).
49. By using switched capacitors at the ADC input an effective input resistance is created. Holding the gain and number of bits constant, the resistance is proportional to the inverse of the clock frequency. This value is calculated, not measured. For more information see the Technical Reference Manual.
50. Recommend an external reference device with an output impedance <100 Ω, for example, the LM185/285/385 family. A 1-µF capacitor is recommended. For more information, see AN61290 - PSoC® 3 and PSoC 5LP Hardware Design Considerations.

Figure 11-40. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode

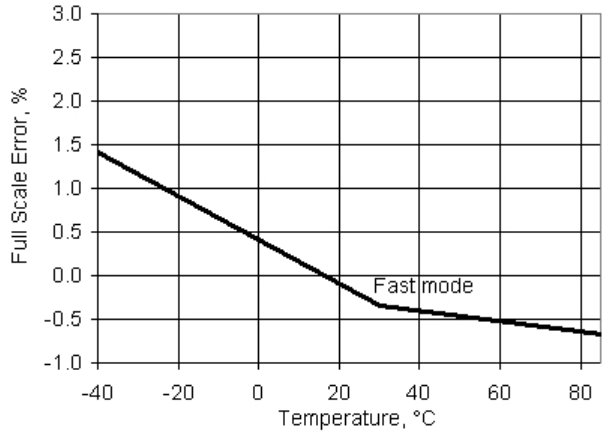


Figure 11-41. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode

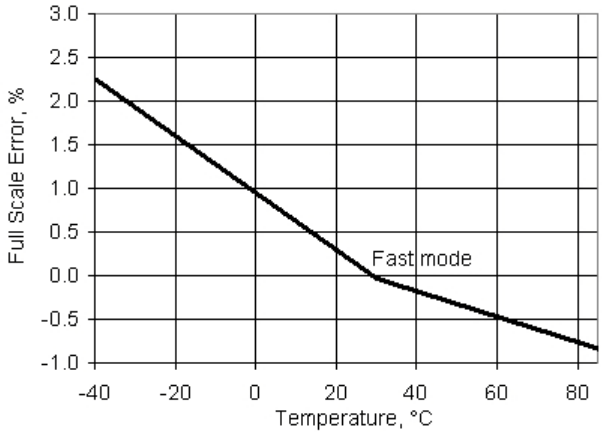


Figure 11-42. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

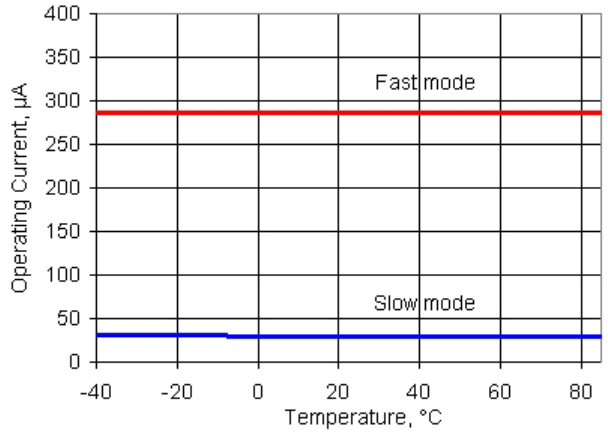


Figure 11-43. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

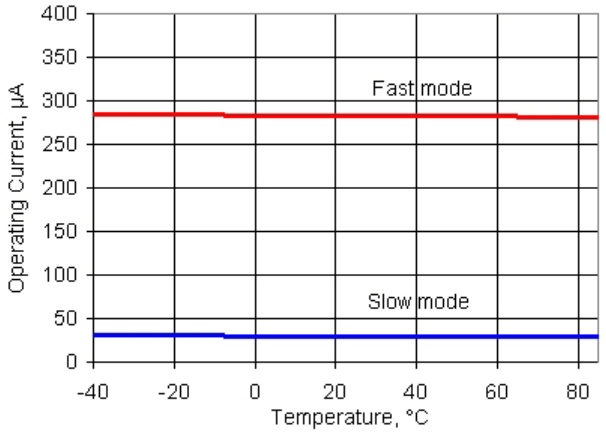


Figure 11-50. VDAC INL vs Temperature, 1 V Mode

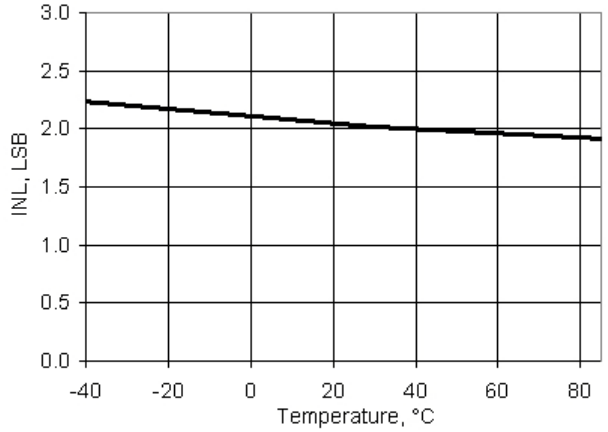


Figure 11-51. VDAC DNL vs Temperature, 1 V Mode

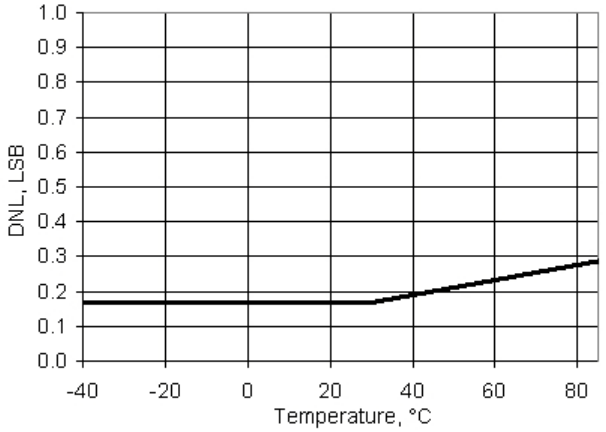


Figure 11-52. VDAC Full Scale Error vs Temperature, 1 V Mode

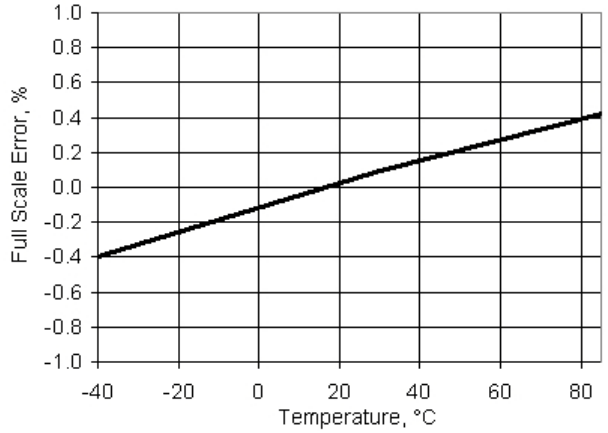


Figure 11-53. VDAC Full Scale Error vs Temperature, 4 V Mode

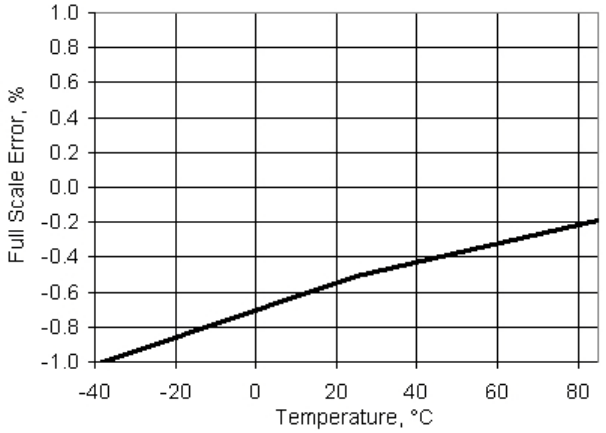


Figure 11-54. VDAC Operating Current vs Temperature, 1V Mode, Low speed mode

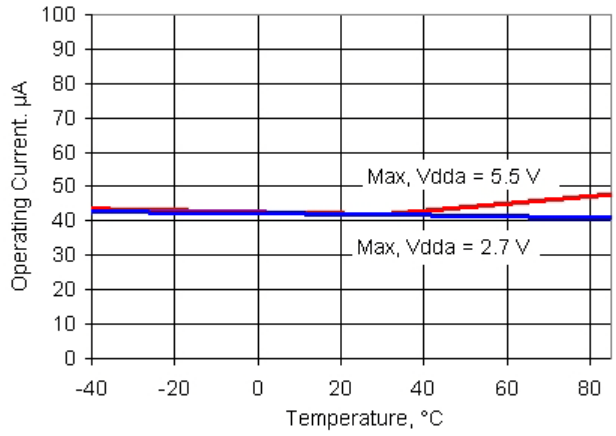
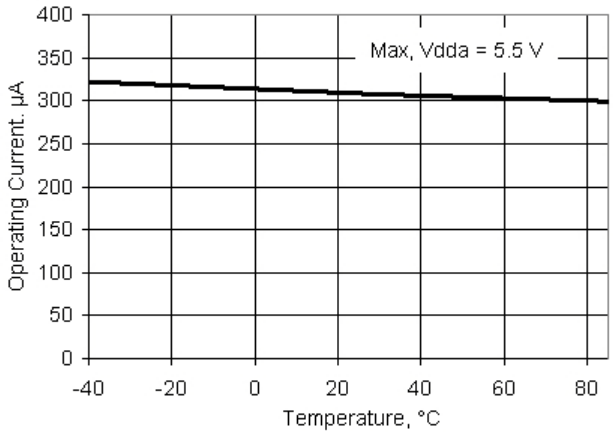


Figure 11-55. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode



11.6 Digital Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.6.1 Timer

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode. Timers can also be implemented in UDBs; for more information, see the Timer component data sheet in PSoC Creator.

Table 11-41. Timer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit timer, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	50 MHz		–	260	–	µA

Table 11-42. Timer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	50.01	MHz
	Capture pulse width (Internal)		21	–	–	ns
	Capture pulse width (external)		42	–	–	ns
	Timer resolution		21	–	–	ns
	Enable pulse width		21	–	–	ns
	Enable pulse width (external)		42	–	–	ns
	Reset pulse width		21	–	–	ns
	Reset pulse width (external)		42	–	–	ns

11.6.2 Counter

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component data sheet in PSoC Creator.

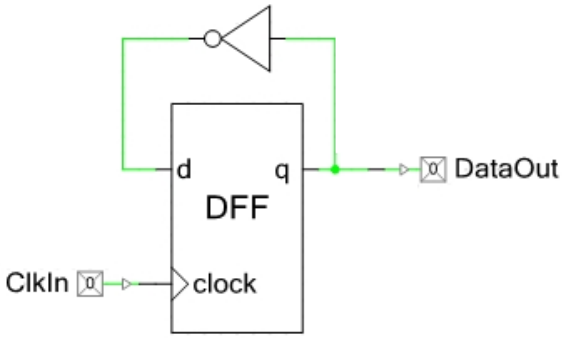
Table 11-43. Counter DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16–bit counter, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	50 MHz		–	260	–	µA

Table 11-44. Counter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	50.01	MHz
	Capture pulse		21	–	–	ns
	Resolution		21	–	–	ns
	Pulse width		21	–	–	ns
	Pulse width (external)		42			ns
	Enable pulse width		21	–	–	ns
	Enable pulse width (external)		42	–	–	ns
	Reset pulse width		21	–	–	ns
	Reset pulse width (external)		42	–	–	ns

Figure 11-63. Clock to Output Performance



11.7 Memory

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-53. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-54. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Row write time (erase + program)		–	15	20	ms
T_{ERASE}	Row erase time		–	10	13	ms
	Row program time		–	5	7	ms
T_{BULK}	Bulk erase time (16 KB to 64 KB)		–	–	35	ms
	Sector erase time (8 KB to 16 KB)		–	–	15	ms
T_{PROG}	Total device programming time	No overhead[59]	–	1.5	2	seconds
	Flash data retention time, retention period measured from last erase cycle	Average ambient temp. T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	years
		Average ambient temp. T_A ≤ 85 °C, 10 K erase/program cycles	10	–	–	years

Note
59. See PSoC® 3 Device Programming Specifications for a description of a low-overhead method of programming PSoC 3 flash.

11.7.2 EEPROM

Table 11-55. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		1.71	–	5.5	V

Table 11-56. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	10	20	ms
	EEPROM data retention time, retention period measured from last erase cycle	Average ambient temp, $T_A \le 25$ °C, 1M erase/program cycles	20	–	–	years
		Average ambient temp, $T_A \le 55$ °C, 100 K erase/program cycles	20	–	–	
		Average ambient temp. $T_A \le 85$ °C, 10 K erase/program cycles	10	–	–	

11.7.3 Nonvolatile Latches (NVL))

Table 11-57. NVL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-58. NVL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at 25 °C	1K	–	–	program/ erase cycles
		Programmed at 0 °C to 70 °C	100	–	–	program/ erase cycles
	NVL data retention time	Average ambient temp. $T_A \le 55$ °C	20	–	–	years
		Average ambient temp. $T_A \le 85$ °C	10	–	–	years

11.7.4 SRAM

Table 11-59. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{SRAM}	SRAM retention voltage		1.2	–	–	V

Table 11-60. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{SRAM}	SRAM operating frequency		DC	–	50.01	MHz

11.7.5 External Memory Interface

Figure 11-64. Asynchronous Write and Read Cycle Timing, No Wait States

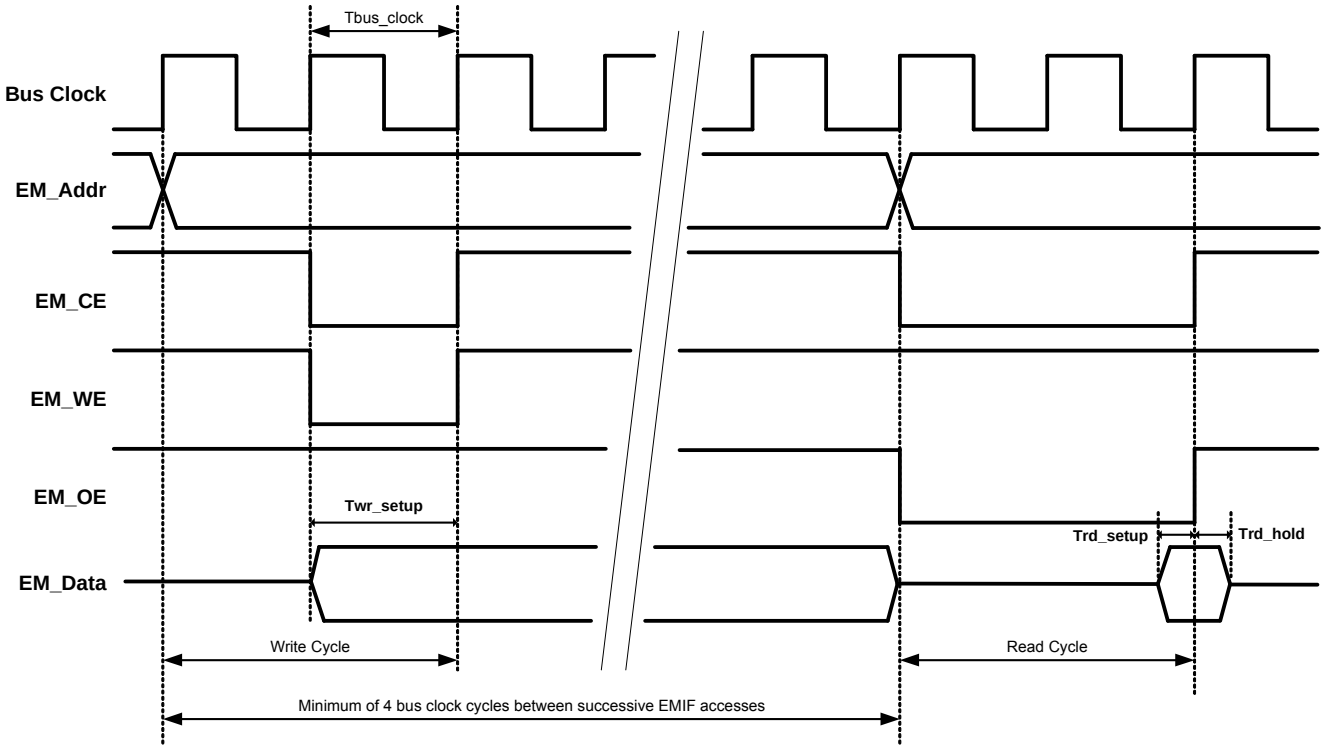


Table 11-61. Asynchronous Write and Read Timing Specifications[60]

Parameter	Description	Conditions	Min	Typ	Max	Units
Fbus_clock	Bus clock frequency[61]		–	–	33	MHz
Tbus_clock	Bus clock period[62]		30.3	–	–	ns
Twr_Setup	Time from EM_data valid to rising edge of EM_WE and EM_CE		Tbus_clock – 10	–	–	ns
Trd_setup	Time that EM_data must be valid before rising edge of EM_OE		5	–	–	ns
Trd_hold	Time that EM_data must be valid after rising edge of EM_OE		5	–	–	ns

Notes
60. Based on device characterization (Not production tested).
61. EMIF signal timings are limited by GPIO frequency limitations. See "GPIO" section on page 79.
62. EMIF output signals are generally synchronized to bus clock, so EMIF signal timings are dependent on bus clock frequency.

11.8.3 Interrupt Controller

Table 11-69. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Delay from interrupt signal input to ISR code execution from ISR code	Includes worse case completion of longest instruction DIV with 6 cycles	–	–	25	Tcy CPU

11.8.4 JTAG Interface

Figure 11-68. JTAG Interface Timing

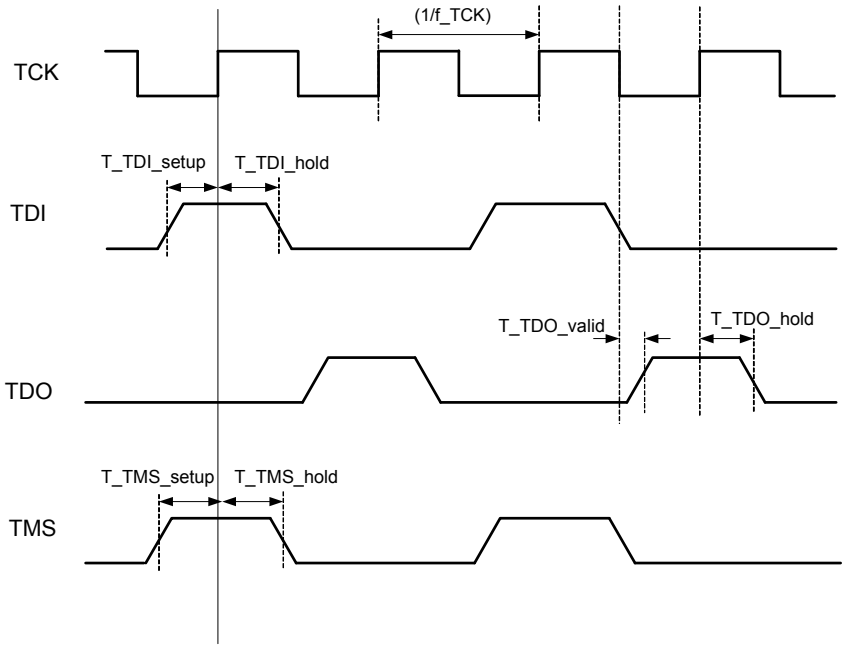


Table 11-70. JTAG Interface AC Specifications[69]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_TCK	TCK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	14[70]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[70]	MHz
T_TDI_setup	TDI setup before TCK high		(T/10) – 5	–	–	ns
T_TMS_setup	TMS setup before TCK high		T/4	–	–	
T_TDI_hold	TDI, TMS hold after TCK high	T = 1/f_TCK max	T/4	–	–	
T_TDO_valid	TCK low to TDO valid	T = 1/f_TCK max	–	–	2T/5	
T_TDO_hold	TDO hold after TCK high	T = 1/f_TCK max	T/4	–	–	

Notes
69. Based on device characterization (Not production tested).
70. f_TCK must also be no more than 1/3 CPU clock frequency.

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C34 device includes: a precision on-chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I^2C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C34 derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C34 Family with Single Cycle 8051

Part Number	MCU Core				Analog								Digital				I/O[81]				Package	JTAG ID[82]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks[79]	Opamps	DFB	CapSense	UDBs[80]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
16 KB Flash																						
CY8C3444LTI-110	50	16	2	0.5	✔	12-bit Del-Sig	2	4	2	2	–	✔	16	4	–	–	46	38	8	0	68-pin QFN	0×1E06E069
CY8C3444LTI-119	50	16	2	0.5	✔	12-bit Del-Sig	2	4	2	2	–	✔	16	4	–	–	29	25	4	0	48-pin QFN	0×1E077069
CY8C3444PVI-100	50	16	2	0.5	✔	12-bit Del-Sig	2	4	2	2	–	✔	16	4	–	–	29	25	4	0	48-pin SSOP	0×1E064069
32 KB Flash																						
CY8C3445AXI-104	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	–	–	70	62	8	0	100-pin TQFP	0×1E068069
CY8C3445LTI-079	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	–	–	46	38	8	0	68-pin QFN	0×1E04F069
CY8C3445LTI-078	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	–	–	29	25	4	0	48-pin QFN	0×1E04E069
CY8C3445PVI-094	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	–	–	29	25	4	0	48-pin SSOP	0×1E05E069
CY8C3445AXI-108	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	✔	–	72	62	8	2	100-pin TQFP	0×1E06C069
CY8C3445LTI-081	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	✔	–	48	38	8	2	68-pin QFN	0×1E051069
CY8C3445PVI-090	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	✔	–	31	25	4	2	48-pin SSOP	0×1E05A069
64 KB Flash																						
CY8C3446LTI-073	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	✔	–	31	25	4	2	48-pin QFN	0×1E049069
CY8C3446LTI-074	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	–	–	46	38	8	0	68-pin QFN	0×1E04A069
CY8C3446LTI-083	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	–	–	29	25	4	0	48-pin QFN	0x1E053069
CY8C3446AXI-099	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	✔	–	72	62	8	2	100-pin TQFP	0×1E063069
CY8C3446AXI-105	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	–	–	70	62	8	0	100-pin TQFP	0x1E069069
CY8C3446LTI-085	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	✔	–	48	38	8	2	68-pin QFN	0×1E055069
CY8C3446PVI-076	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	✔	–	31	25	4	2	48-pin SSOP	0×1E04C069
CY8C3446PVI-102	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	–	✔	29	25	4	0	48-pin SSOP	0x1E066069

Notes

79. Analog blocks support a wide variety of functionality including TIA, PGA, and mixers. See the Example Peripherals on page 43 for more information on how analog blocks can be used.
80. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the Example Peripherals on page 43 for more information on how UDBs can be used.
81. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the I/O System and Routing on page 36 for details on the functionality of each of these types of I/O.
82. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
µA	microamperes
µF	microfarads
µH	microhenrys
µs	microseconds
µV	microvolts
µW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts

Description Title: PSoC® 3: CY8C34 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-53304				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*J	3179219	02/22/2011	MKEA	Updated conditions for flash data retention time. Updated 100-pin TQFP package spec. Updated EEPROM AC specifications.
*K	3200146	03/28/2011	MKEA	Removed Preliminary status from the data sheet. Updated JTAG ID Deleted Cin_G1, ADC input capacitance from Delta-Sigma ADC DC spec table Updated JTAG Interface AC Specifications and SWD Interface Specifications tables Updated USBIO DC specs Added 0.01 to max speed Updated Features on page 1 Added Section 5.5, Nonvolatile Latches Updated Flash AC specs Added CAN DC specs Updated delta-sigma graphs, noise histogram figures and RMS Noise spec tables Add reference to application note AN58304 in section 8.1 Updated 100-pin TQFP package spec Added oscillator, I/O, VDAC, regulator graphs Updated JTAG/SWD timing diagrams Updated GPIO and SIO AC specs Updated POR with Brown Out AC spec table Updated IDAC graphs Added DMA timing diagram, interrupt timing and interrupt vector, I2C timing diagrams Updated opamp graphs and PGA graphs Added full chip performance graphs Changed MHzECO range. Added “Solder Reflow Peak Temperature” table.
*L	3259185	05/17/2011	MKEA	Added JTAG and SWD interface connection diagrams Updated T_{JA} and T_{JC} values in Table 13-1 Changed typ and max values for the TCVos parameter in Opamp DC specifications table. Updated Clocking subsystem diagram. Changed VSSD to VSSB in the PSoC Power System diagram Updated Ordering information.

Description Title: PSoC® 3: CY8C34 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-53304				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*V	4708125	03/31/2015	MKEA	Added INL4 and DNL4 specs in VDAC DC Specifications. Updated Figure 6-11. Added second note after Figure 6-4. Added a reference to Fig 6-1 in *Section 6.1.1* and *Section 6.1.2*. Updated *Section 6.2.2*. Added *Section 7.8.1*. Updated Boost specifications.
*W	4807497	06/23/2015	MKEA	Added reference to code examples in More Information. Updated typ value of TWRITE from 2 to 10 in EEPROM AC specs table. Changed “Device supply for USB operation" to "Device supply (VDDD) for USB operation" in USB DC Specifications. Clarified power supply sequencing and margin for VDDA and VDDD. Updated Serial Wire Debug Interface with limitations of debugging on Port 15. Updated Section 11.7.5. Updated Delta-sigma ADC DC Specifications
*X	4932879	09/24/2015	MKEA	Changed the Regulator Output Capacitor min and max from "-" to 0.9 and 1.1, respectively. Added reference to AN54439 in Section 11.9.3. Added MHz ECO DC specs table. Removed references to IPOR rearm issues in Section 6.3.1.1. Table 6-1: Changed DSI Fmax to 33 MHz. Figure 6-1: Changed External I/O or DSI to 0-33 MHz. Table 11-10: Changed Fgpioin Max to 33 MHz. Table 11-12: Changed Fsioin Max to 33 MHz.
*Y	5322536	06/27/2016	MKEA	Updated More Information. Corrected typos in External Electrical Connections. Added links to CAD Libraries in Section 2.

18. Sales, Solutions, and Legal Information

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