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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3446lti-073t

Contents

1. Architectural Overview	4	9. Programming, Debug Interfaces, Resources	65
2. Pinouts	6	9.1 JTAG Interface	66
3. Pin Descriptions	11	9.2 Serial Wire Debug Interface	67
4. CPU	12	9.3 Debug Features	68
4.1 8051 CPU	12	9.4 Trace Features	68
4.2 Addressing Modes	12	9.5 Single Wire Viewer Interface	68
4.3 Instruction Set	13	9.6 Programming Features	68
4.4 DMA and PHUB	17	9.7 Device Security	68
4.5 Interrupt Controller	18	10. Development Support	69
5. Memory	22	10.1 Documentation	69
5.1 Static RAM	22	10.2 Online	69
5.2 Flash Program Memory	22	10.3 Tools	69
5.3 Flash Security	22	11. Electrical Specifications	70
5.4 EEPROM	22	11.1 Absolute Maximum Ratings	70
5.5 Nonvolatile Latches (NVLs)	23	11.2 Device Level Specifications	71
5.6 External Memory Interface	24	11.3 Power Regulators	75
5.7 Memory Map	25	11.4 Inputs and Outputs	79
6. System Integration	27	11.5 Analog Peripherals	88
6.1 Clocking System	27	11.6 Digital Peripherals	105
6.2 Power System	30	11.7 Memory	108
6.3 Reset	34	11.8 PSoC System Resources	114
6.4 I/O System and Routing	36	11.9 Clocking	117
7. Digital Subsystem	43	12. Ordering Information	121
7.1 Example Peripherals	43	12.1 Part Numbering Conventions	122
7.2 Universal Digital Block	45	13. Packaging	123
7.3 UDB Array Description	48	14. Acronyms	126
7.4 DSI Routing Interface Description	49	15. Reference Documents	127
7.5 CAN	50	16. Document Conventions	128
7.6 USB	52	16.1 Units of Measure	128
7.7 Timers, Counters, and PWMs	53	17. Revision History	129
7.8 I ² C	54	18. Sales, Solutions, and Legal Information	137
8. Analog Subsystem	56	Worldwide Sales and Design Support.....	137
8.1 Analog Routing	57	Products	137
8.2 Delta-sigma ADC	59	PSoC® Solutions	137
8.3 Comparators	60	Cypress Developer Community.....	137
8.4 Opamps	61	Technical Support	137
8.5 Programmable SC/CT Blocks	61		
8.6 LCD Direct Drive	63		
8.7 CapSense	64		
8.8 Temp Sensor	64		
8.9 DAC	64		
8.10 Up/Down Mixer	64		
8.11 Sample and Hold	65		

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C34 family these blocks can include four 16-bit timer, counter, and PWM blocks; I²C slave, master, and multi-master; Full-Speed USB; and Full CAN 2.0b.

For more details on the peripherals see the “[Example Peripherals](#)” section on page 43 of this data sheet. For information on UDBs, DSI, and other digital blocks, see the “[Digital Subsystem](#)” section on page 43 of this data sheet.

PSoC’s analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 1-percent error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Voltage references
- Analog-to-digital converter (ADC)
- Digital-to-analog converters (DACs)

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. The heart of the analog subsystem is a fast, accurate, configurable delta-sigma ADC with these features:

- Less than 100 μ V offset
- A gain error of 0.2 percent
- INL less than ± 1 LSB
- DNL less than ± 1 LSB
- SINAD better than 66 dB

This converter addresses a wide variety of precision analog applications, including some of the most demanding sensors.

Two high-speed voltage or current DACs support 8-bit output signals at update rate of 8 Msps in current DAC (IDAC) and 1 Msps in voltage DAC (VDAC). They can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths.

In addition to the ADC and DACs, the analog subsystem provides multiple:

- Uncommitted opamps
- Configurable switched capacitor/continuous time (SC/CT) blocks. These support:
 - Transimpedance amplifiers
 - Programmable gain amplifiers
 - Mixers

- Other similar analog components

See the “[Analog Subsystem](#)” section on page 56 of this data sheet for more details.

PSoC’s 8051 CPU subsystem is built around a single cycle pipelined 8051 8-bit processor running at up to 50 MHz. The CPU subsystem includes a programmable nested vector interrupt controller, DMA controller, and RAM. PSoC’s nested vector interrupt controller provides low latency by allowing the CPU to vector directly to the first address of the interrupt service routine, bypassing the jump instruction required by other architectures. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor. The processor speed itself is configurable, allowing you to tune active power consumption for specific applications.

PSoC’s nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 64 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling bootloaders. You can enable an error correcting code (ECC) for high reliability applications. A powerful and flexible protection model secures the user’s sensitive information, allowing selective memory block locking for read and write protection. Up to 2 KB of byte-writeable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after power-on reset (POR).

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the VDDIO pins. Every GPIO has analog I/O, LCD drive^[3], CapSense^[4], flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow VOH to be set independently of VDDIO when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I²C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with Full-Speed USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All of the features of the PSoC I/Os are covered in detail in the “[I/O System and Routing](#)” section on page 36 of this data sheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The Internal Main Oscillator (IMO) is the clock base for the system, and has 2-percent accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 24 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs.

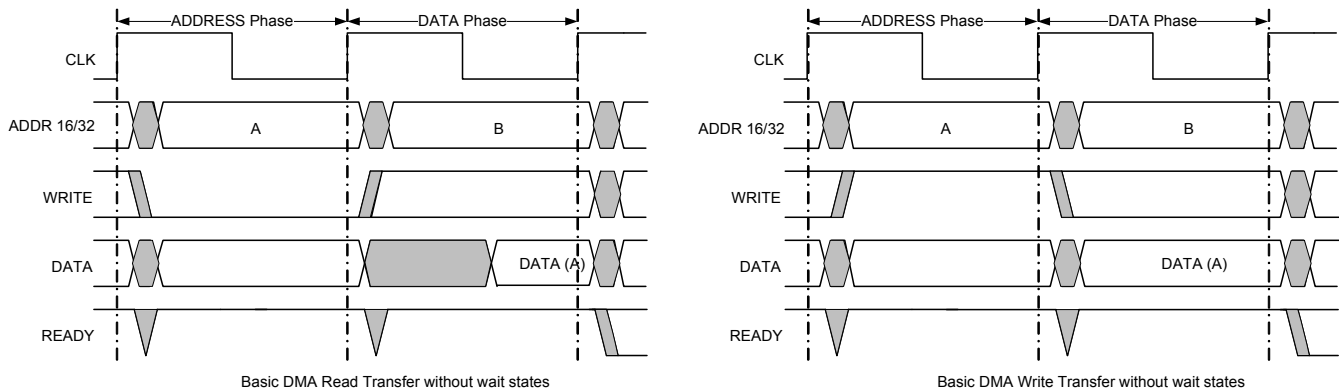
Notes

3. This feature on select devices only. See [Ordering Information](#) on page 121 for details.
4. GPIOs with opamp outputs are not recommended for use with CapSense.

4.4.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location). The basic timing diagrams of DMA read and write cycles are shown in [Figure 4-1](#). For more description on other transfer modes, refer to the Technical Reference Manual.

Figure 4-1. DMA Timing Diagram



4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU

can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts

- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

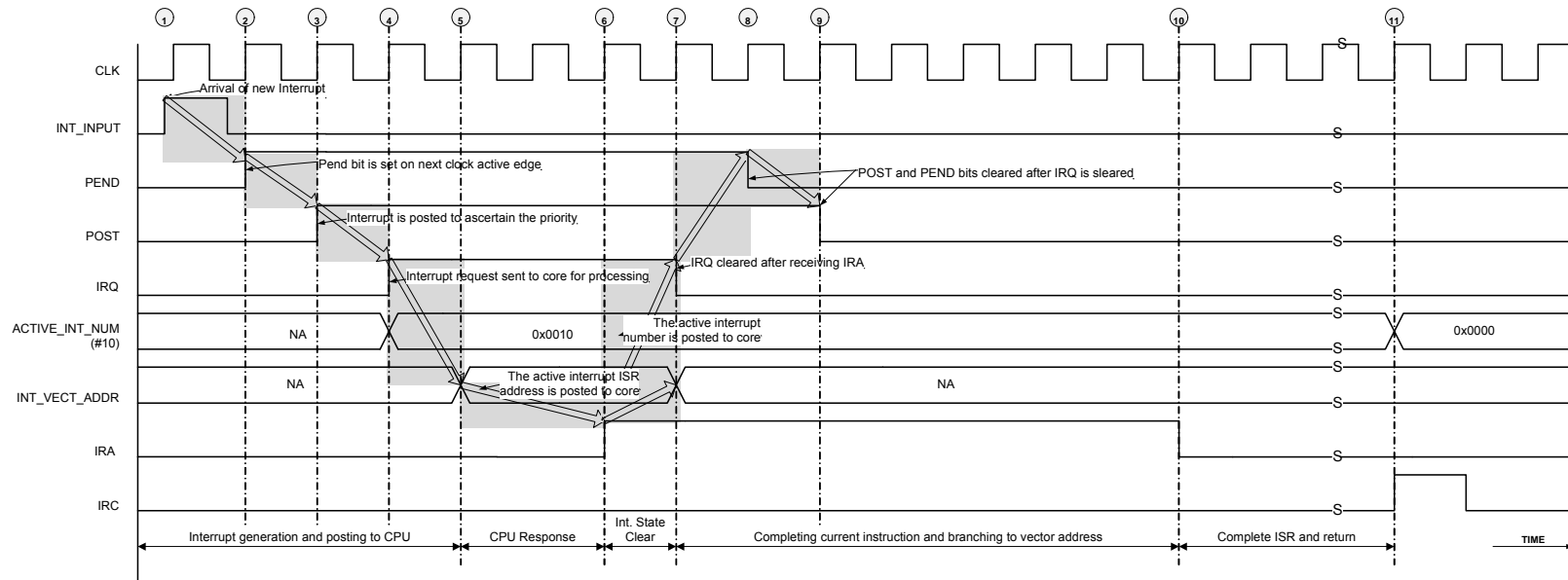
When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are

direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Figure 4-2 represents typical flow of events when an interrupt triggered. Figure 4-3 on page 20 shows the interrupt structure and priority polling.

Figure 4-2. Interrupt Processing Timing Diagram



Notes

- 1: Interrupt triggered asynchronous to the clock
- 2: The PEND bit is set on next active clock edge to indicate the interrupt arrival
- 3: POST bit is set following the PEND bit
- 4: Interrupt request and the interrupt number sent to CPU core after evaluation priority (Takes 3 clocks)
- 5: ISR address is posted to CPU core for branching

The CY8C34 family provides the standard set of registers found on industry standard 8051 devices. In addition, the CY8C34 devices add SFRs to provide direct access to the I/O ports on the device. The following sections describe the SFRs added to the CY8C34 family.

5.7.4 XData Space Access SFRs

The 8051 core features dual DPTR registers for faster data transfer operations. The data pointer select SFR, DPS, selects which data pointer register, DPTR0 or DPTR1, is used for the following instructions:

- MOVX @DPTR, A
- MOVX A, @DPTR
- MOVC A, @A+DPTR
- JMP @A+DPTR
- INC DPTR
- MOV DPTR, #data16

The extended data pointer SFRs, DPX0, DPX1, MXAX, and P2AX, hold the most significant parts of memory addresses during access to the xdata space. These SFRs are used only with the MOVX instructions.

During a MOVX instruction using the DPTR0/DPTR1 register, the most significant byte of the address is always equal to the contents of DPX0/DPX1. During a MOVX instruction using the R0 or R1 register, the most significant byte of the address is always equal to the contents of MXAX, and the next most significant byte is always equal to the contents of P2AX.

5.7.5 I/O Port SFRs

The I/O ports provide digital input sensing, output drive, pin interrupts, connectivity for analog inputs and outputs, LCD, and access to peripherals through the DSI. Full information on I/O ports is found in [I/O System and Routing](#) on page 36.

I/O ports are linked to the CPU through the PHUB and are also available in the SFRs. Using the SFRs allows faster access to a limited set of I/O port registers, while using the PHUB allows boot configuration and access to all I/O port registers.

Each SFR supported I/O port provides three SFRs:

- SFRPRTxDR sets the output data state of the port (where x is port number and includes ports 0-6, 12 and 15)
- The SFRPRTxSEL selects whether the PHUB PRTxDR register or the SFRPRTxDR controls each pin's output buffer within the port. If a SFRPRTxSEL[y] bit is high, the corresponding SFRPRTxDR[y] bit sets the output state for that pin. If a SFRPRTxSEL[y] bit is low, the corresponding PRTxDR[y] bit sets the output state of the pin (where y varies from 0 to 7).
- The SFRPRTxPS is a read only register that contains pin state values of the port pins.

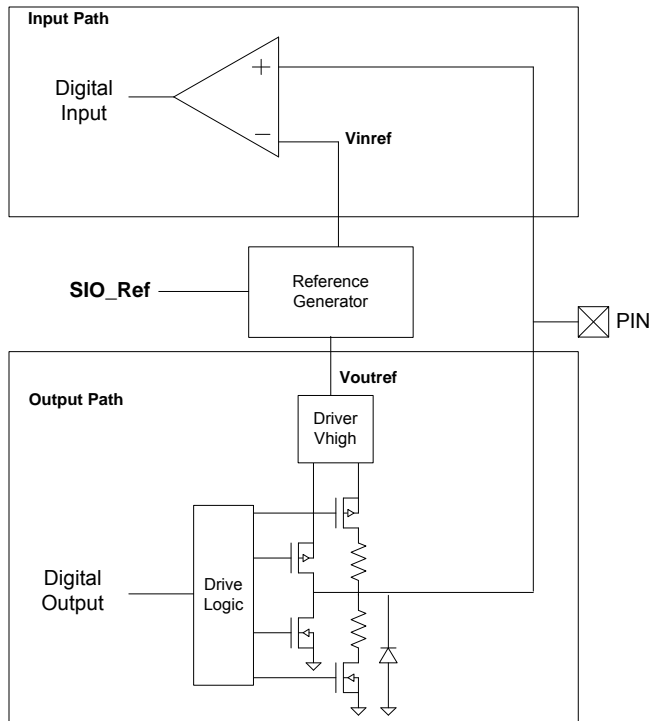
5.7.5.1 xdata Space

The 8051 xdata space is 24-bit, or 16 MB in size. The majority of this space is not “external”—it is used by on-chip components. See [Table 5-5](#). External, that is, off-chip, memory can be accessed using the EMIF. See [External Memory Interface](#) on page 24.

Table 5-5. XDATA Data Address Map

Address Range	Purpose
0x00 0000 – 0x00 1FFF	SRAM
0x00 4000 – 0x00 42FF	Clocking, PLLs, and oscillators
0x00 4300 – 0x00 43FF	Power management
0x00 4400 – 0x00 44FF	Interrupt controller
0x00 4500 – 0x00 45FF	Ports interrupt control
0x00 4700 – 0x00 47FF	Flash programming interface
0x00 4800 – 0x00 48FF	Cache controller
0x00 4900 – 0x00 49FF	I ² C controller
0x00 4E00 – 0x00 4EFF	Decimator
0x00 4F00 – 0x00 4FFF	Fixed timer/counter/PWMs
0x00 5000 – 0x00 51FF	I/O ports control
0x00 5400 – 0x00 54FF	External Memory Interface (EMIF) control registers
0x00 5800 – 0x00 5FFF	Analog Subsystem interface
0x00 6000 – 0x00 60FF	USB controller
0x00 6400 – 0x00 6FFF	UDB Working Registers
0x00 7000 – 0x00 7FFF	PHUB configuration
0x00 8000 – 0x00 8FFF	EEPROM
0x00 A000 – 0x00 A400	CAN
0x01 0000 – 0x01 FFFF	Digital Interconnect configuration
0x05 0220 – 0x05 02F0	Debug controller
0x08 0000 – 0x08 1FFF	Flash ECC bytes
0x80 0000 – 0xFF FFFF	External Memory Interface

Figure 6-13. SIO Reference for Input and Output



6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the [Adjustable Input Level](#) section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold.

The digital input path in [Figure 6-10](#) on page 38 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a SIO pin's protection diode.

Powering the device up or down while connected to an operational I2C bus may cause transient states on the SIO pins. The overall I2C bus design should take this into account.

6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating V_{DD} .

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit where $V_{DDIO} \leq V_{IN} \leq 5.5$ V.
- The GPIO pins must be limited to 100 μ A using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the V_{ddio} supply where $V_{ddio} \leq V_{IN} \leq V_{DDA}$.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the V_{ddio} supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I²C where different devices are running from different supply voltages. In the I²C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I²C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's V_{IH} and V_{IL} levels are determined by the associated V_{ddio} supply pin.

The SIO pin must be in one of the following modes: 0 (high impedance analog), 1 (high impedance digital), or 4 (open drain drives low). See [Figure 6-12](#) for details. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull-down or pull-up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low-Power Functionality

In all low-power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low-power modes.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in [Pinouts](#) on page 6. The special features are:

- Digital
 - 4 to 25 MHz crystal oscillator
 - 32.768-kHz crystal oscillator
 - Wake from sleep on I²C address match. Any pin can be used for I²C if wake from sleep is not required.
 - JTAG interface pins
 - SWD interface pins
 - SWV interface pins
 - External reset
- Analog
 - Opamp inputs and outputs
 - High current IDAC outputs
 - External reference inputs

8.2.3 Start of Conversion Input

The SoC signal is used to start an ADC conversion. A digital clock or UDB output can be used to drive this input. It can be used when the sampling period must be longer than the ADC conversion time or when the ADC must be synchronized to other hardware. This signal is optional and does not need to be connected if ADC is running in a continuous mode.

8.2.4 End of Conversion Output

The EoC signal goes high at the end of each ADC conversion. This signal may be used to trigger either an interrupt or DMA request.

8.3 Comparators

The CY8C34 family of devices contains four comparators in a device. Comparators have these features:

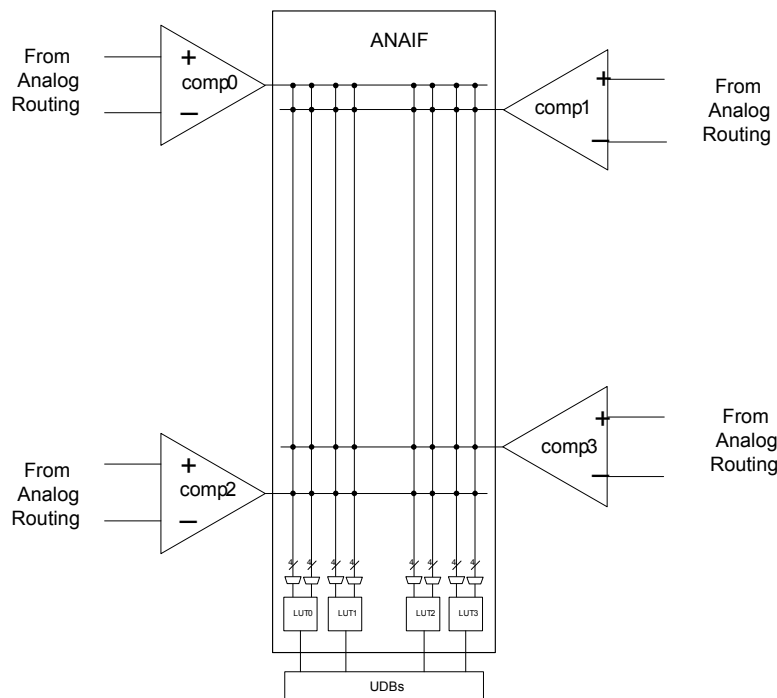
- Input offset factory trimmed to less than 5 mV
- Rail-to-rail common mode input range (V_{SSA} to V_{DDA})

- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low-power
- Comparator outputs can be routed to lookup tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB Digital System Interface.

Figure 8-5. Analog Comparator



11. Electrical Specifications

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component data sheets for full AC/DC specifications of individual functions. See the “[Example Peripherals](#)” section on page 43 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings DC Specifications^[18]

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Analog supply voltage relative to V_{SSA}		-0.5	–	6	V
V_{DDD}	Digital supply voltage relative to V_{SSD}		-0.5	–	6	V
V_{DDIO}	I/O supply voltage relative to V_{SSD}		-0.5	–	6	V
V_{CCA}	Direct analog core voltage input		-0.5	–	1.95	V
V_{CCD}	Direct digital core voltage input		-0.5	–	1.95	V
V_{SSA}	Analog ground voltage		$V_{SSD} - 0.5$	–	$V_{SSD} + 0.5$	V
$V_{GPIO}^{[19]}$	DC input voltage on GPIO	Includes signals sourced by V_{DDA} and routed internal to the pin	$V_{SSD} - 0.5$	–	$V_{DDIO} + 0.5$	V
V_{SIO}	DC input voltage on SIO	Output disabled	$V_{SSD} - 0.5$	–	7	V
		Output enabled	$V_{SSD} - 0.5$	–	6	V
V_{IND}	Voltage at boost converter input		0.5	–	5.5	V
V_{BAT}	Boost converter supply		$V_{SSD} - 0.5$	–	5.5	V
I_{VDDIO}	Current per V_{DDIO} supply pin		–	–	100	mA
I_{GPIO}	GPIO current		-30	–	41	mA
I_{SIO}	SIO current		-49	–	28	mA
I_{USBIO}	USBIO current		-56	–	59	mA
V_{EXTREF}	ADC external reference inputs	Pins P0[3], P3[2]	–	–	2	V
LU	Latch up current ^[20]		-140	–	140	mA
ESD_{HBM}	Electrostatic discharge voltage, Human body model	V_{SSA} tied to V_{SSD}	2200	–	–	V
		V_{SSA} not tied to V_{SSD}	750	–	–	V
ESD_{CDM}	Electrostatic discharge voltage, Charge device model		500	–	–	V

Notes

18. Usage above the absolute maximum conditions listed in [Table 11-1](#) may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

19. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin $\leq V_{DDIO} \leq V_{DDA}$.

20. Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test.

11.3 Power Regulators

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor	$\pm 10\%$, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 30	0.9	1	1.1	μF

Figure 11-5. Regulators V_{CC} vs V_{DD}

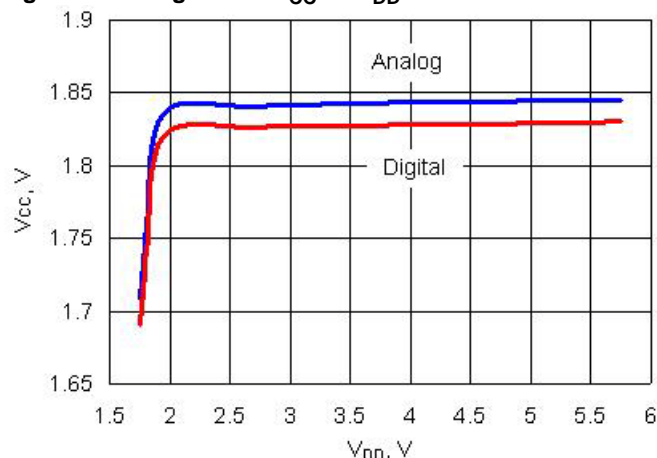
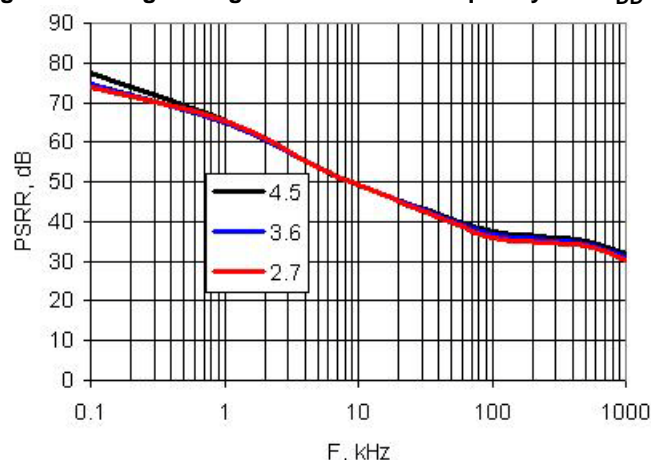


Figure 11-6. Digital Regulator PSRR vs Frequency and V_{DD}



11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor	$\pm 10\%$, X5R ceramic or better	0.9	1	1.1	μF

Figure 11-7. Analog Regulator PSRR vs Frequency and V_{DD}

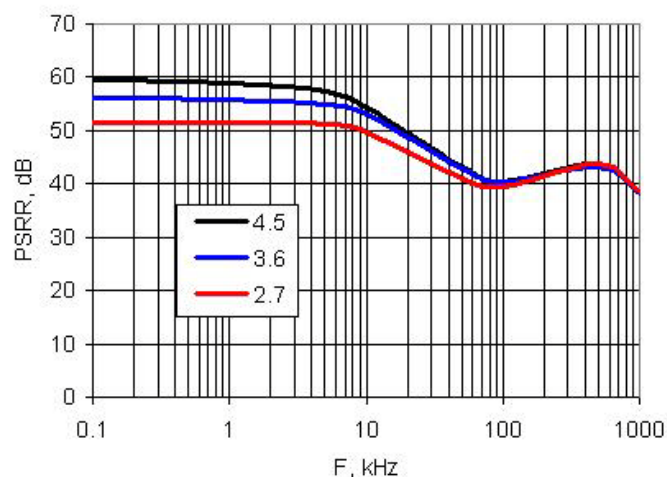


Figure 11-27. Opamp Voffset vs Vcommon and V_{DDA}, 25 °C

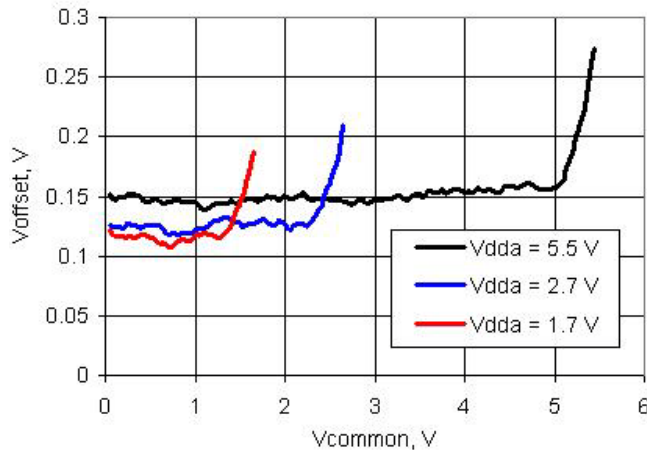


Figure 11-28. Opamp Output Voltage vs Load Current and Temperature, High Power Mode, 25 °C, V_{DDA} = 2.7 V

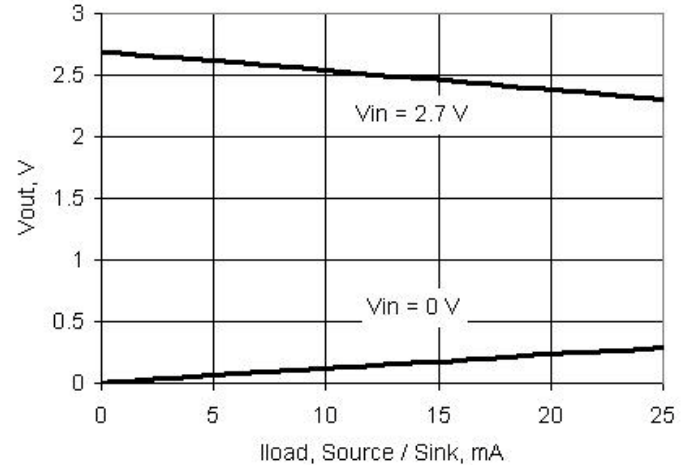


Figure 11-29. Opamp Operating Current vs V_{DDA} and Power Mode

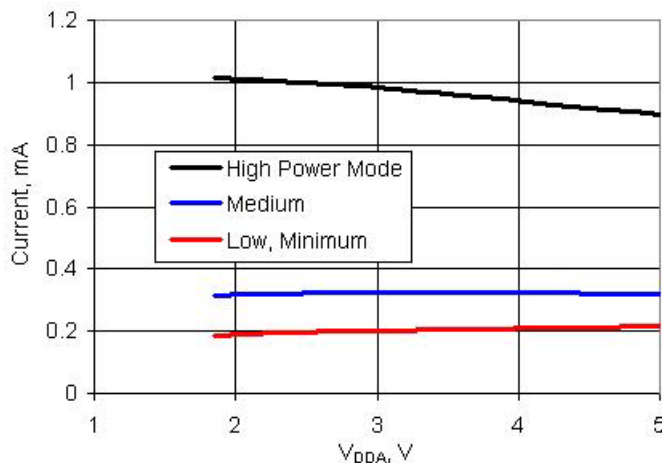


Table 11-20. Opamp AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW	Gain-bandwidth product	Power mode = minimum, 15 pF load	1	—	—	MHz
		Power mode = low, 15 pF load	2	—	—	MHz
		Power mode = medium, 200 pF load	1	—	—	MHz
		Power mode = high, 200 pF load	3	—	—	MHz
SR	Slew rate, 20% - 80%	Power mode = low, 15 pF load	1.1	—	—	V/μs
		Power mode = medium, 200 pF load	0.9	—	—	V/μs
		Power mode = high, 200 pF load	3	—	—	V/μs
e _n	Input noise density	Power mode = high, V _{DDA} = 5 V, at 100 kHz	—	45	—	nV/sqrtHz

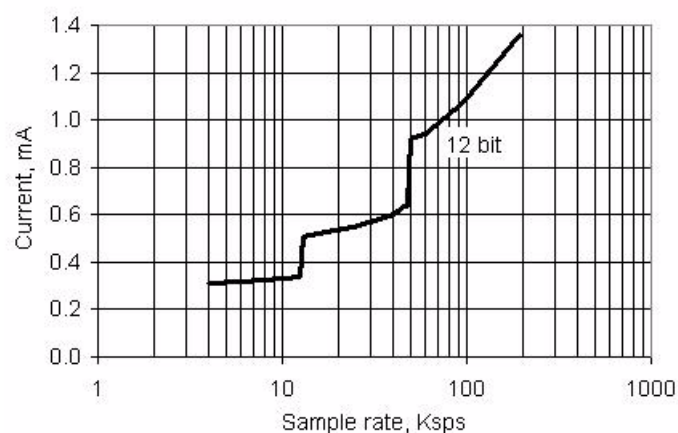
Table 11-22. Delta-sigma ADC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time		–	–	4	Samples
THD	Total harmonic distortion ^[51]	Buffer gain = 1, 12-bit, Range = ± 1.024 V	–	–	0.0032	%
12-Bit Resolution Mode						
SR12	Sample rate, continuous, high power ^[51]	Range = ± 1.024 V, unbuffered	4	–	192	ksps
BW12	Input bandwidth at max sample rate ^[51]	Range = ± 1.024 V, unbuffered	–	44	–	kHz
SINAD12int	Signal to noise ratio, 12-bit, internal reference ^[51]	Range = ± 1.024 V, unbuffered	66	–	–	dB
8-Bit Resolution Mode						
SR8	Sample rate, continuous, high power ^[51]	Range = ± 1.024 V, unbuffered	8	–	384	ksps
BW8	Input bandwidth at max sample rate ^[51]	Range = ± 1.024 V, unbuffered	–	88	–	kHz
SINAD8int	Signal to noise ratio, 8-bit, internal reference ^[51]	Range = ± 1.024 V, unbuffered	43	–	–	dB

Table 11-23. Delta-sigma ADC Sample Rates, Range = ± 1.024 V

Resolution, Bits	Continuous		Multi-Sample	
	Min	Max	Min	Max
8	8000	384000	1911	91701
9	6400	307200	1543	74024
10	5566	267130	1348	64673
11	4741	227555	1154	55351
12	4000	192000	978	46900

Figure 11-33. Delta-sigma ADC IDD vs sps, Range = ± 1.024 V, Continuous Sample Mode, Input Buffer Bypassed



Note

51. Based on device characterization (Not production tested).

Figure 11-40. IDAC Full Scale Error vs Temperature, Range = 255 μ A, Source Mode

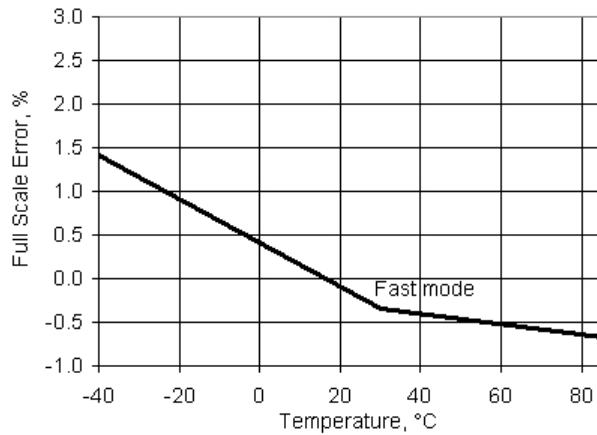


Figure 11-41. IDAC Full Scale Error vs Temperature, Range = 255 μ A, Sink Mode

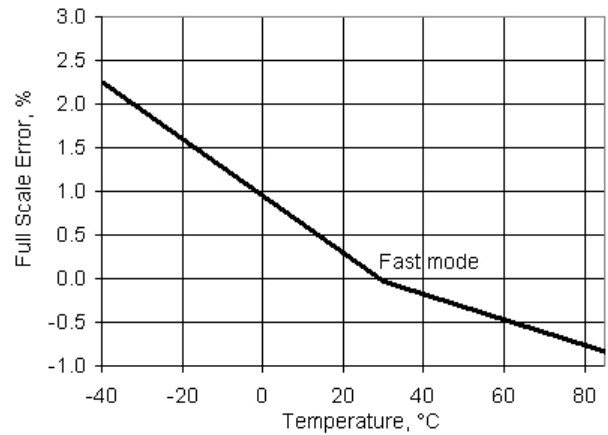


Figure 11-42. IDAC Operating Current vs Temperature, Range = 255 μ A, Code = 0, Source Mode

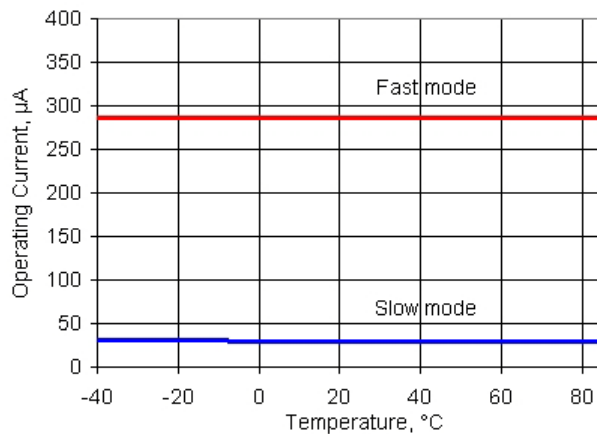


Figure 11-43. IDAC Operating Current vs Temperature, Range = 255 μ A, Code = 0, Sink Mode

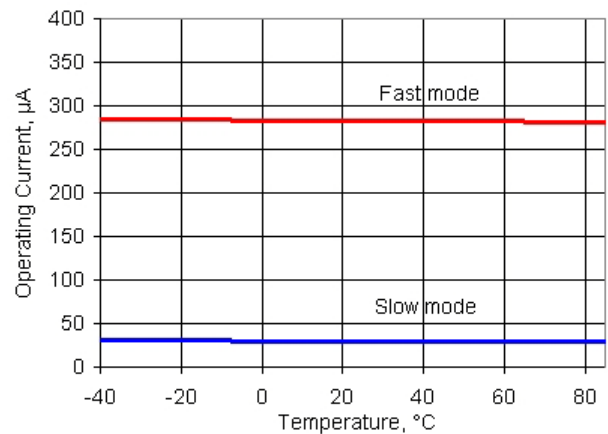


Figure 11-50. VDAC INL vs Temperature, 1 V Mode

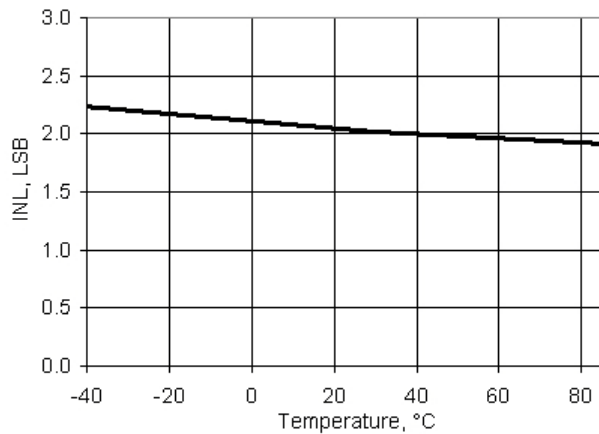


Figure 11-51. VDAC DNL vs Temperature, 1 V Mode

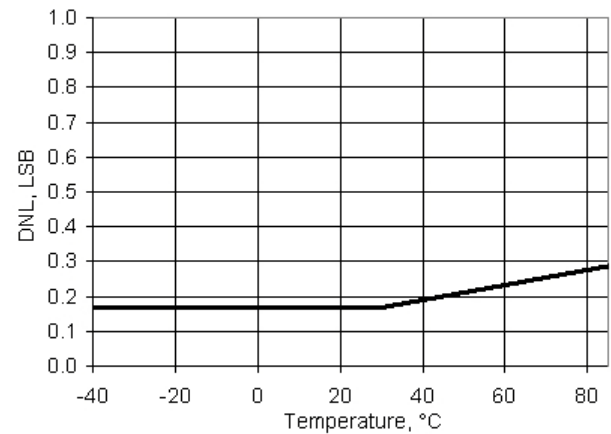


Figure 11-52. VDAC Full Scale Error vs Temperature, 1 V Mode

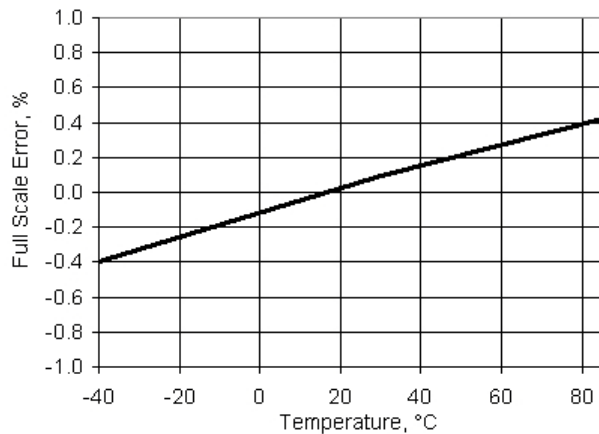


Figure 11-53. VDAC Full Scale Error vs Temperature, 4 V Mode

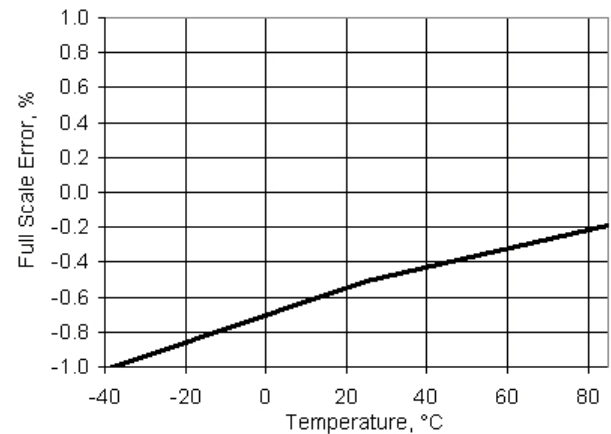


Figure 11-54. VDAC Operating Current vs Temperature, 1V Mode, Low speed mode

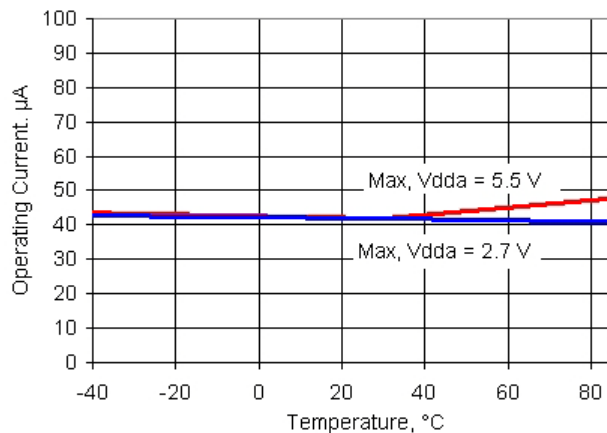
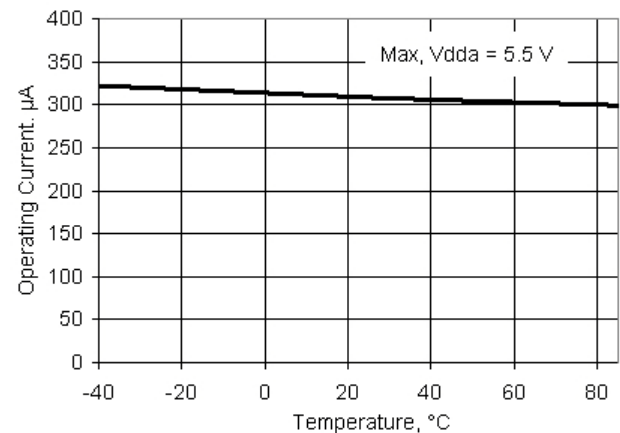


Figure 11-55. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode



11.7.5 External Memory Interface

Figure 11-64. Asynchronous Write and Read Cycle Timing, No Wait States

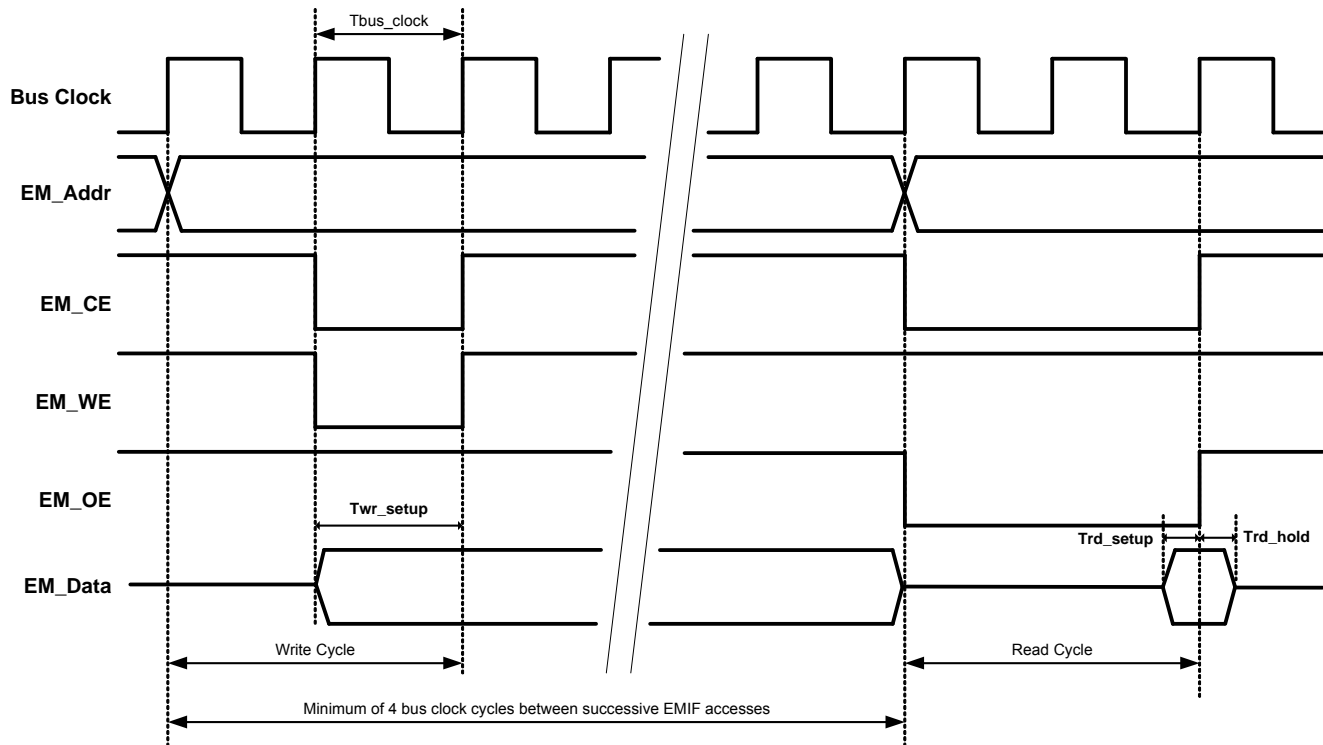


Table 11-61. Asynchronous Write and Read Timing Specifications^[60]

Parameter	Description	Conditions	Min	Typ	Max	Units
Fbus_clock	Bus clock frequency ^[61]		–	–	33	MHz
Tbus_clock	Bus clock period ^[62]		30.3	–	–	ns
Twr_Setup	Time from EM_data valid to rising edge of EM_WE and EM_CE		Tbus_clock – 10	–	–	ns
Trd_setup	Time that EM_data must be valid before rising edge of EM_OE		5	–	–	ns
Trd_hold	Time that EM_data must be valid after rising edge of EM_OE		5	–	–	ns

Notes

60. Based on device characterization (Not production tested).

61. EMIF signal timings are limited by GPIO frequency limitations. See “GPIO” section on page 79.

62. EMIF output signals are generally synchronized to bus clock, so EMIF signal timings are dependent on bus clock frequency.

Figure 11-66. Synchronous Read Cycle Timing

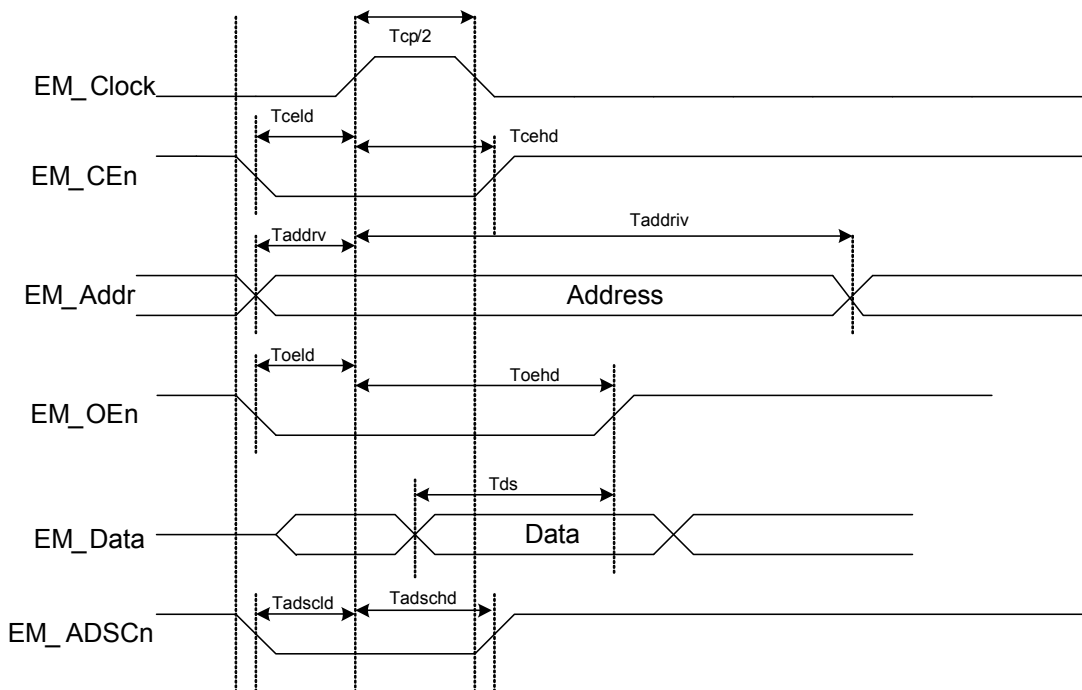


Table 11-63. Synchronous Read Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock period ^[66]	V _{DDA} ≥ 3.3 V	30.3	–	–	ns
T _{cp/2}	EM_Clock pulse high		T/2	–	–	ns
T _{cld}	EM_CEn low to EM_Clock high		5	–	–	ns
T _{cehd}	EM_Clock high to EM_CEn high		T/2 – 5	–	–	ns
T _{addrv}	EM_Addr valid to EM_Clock high		5	–	–	ns
T _{addriv}	EM_Clock high to EM_Addr invalid		T/2 – 5	–	–	ns
T _{oeld}	EM_OEn low to EM_Clock high		5	–	–	ns
T _{oehd}	EM_Clock high to EM_OEn high		T	–	–	ns
T _{ds}	Data valid before EM_OEn high		T + 15	–	–	ns
T _{dscl}	EM_ADSCn low to EM_Clock high		5	–	–	ns
T _{dschd}	EM_Clock high to EM_ADSCn high		T/2 – 5	–	–	ns

Note

66. Limited by GPIO output frequency, see Table 11-10 on page 80.

11.8 PSoC System Resources

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.8.1 POR with Brown Out

For brown out detect in regulated mode, V_{DDD} and V_{DDA} must be $\geq 2.0\text{ V}$. Brown out detect is not available in externally regulated mode.

Table 11-65. Precise Low-Voltage Reset (PRES) with Brown Out DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRESR	Rising trip voltage	Factory trim	1.64	–	1.68	V
PRESF	Falling trip voltage		1.62	–	1.66	V

Table 11-66. Power-on Reset (POR) with Brown Out AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
PRES_TR	Response time		–	–	0.5	μs
	V_{DDD}/V_{DDA} droop rate	Sleep mode	–	5	–	V/sec

11.8.2 Voltage Monitors

Table 11-67. Voltage Monitors DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI	Trip voltage					
	LVI_A/D_SEL[3:0] = 0000b		1.68	1.73	1.77	V
	LVI_A/D_SEL[3:0] = 0001b		1.89	1.95	2.01	V
	LVI_A/D_SEL[3:0] = 0010b		2.14	2.20	2.27	V
	LVI_A/D_SEL[3:0] = 0011b		2.38	2.45	2.53	V
	LVI_A/D_SEL[3:0] = 0100b		2.62	2.71	2.79	V
	LVI_A/D_SEL[3:0] = 0101b		2.87	2.95	3.04	V
	LVI_A/D_SEL[3:0] = 0110b		3.11	3.21	3.31	V
	LVI_A/D_SEL[3:0] = 0111b		3.35	3.46	3.56	V
	LVI_A/D_SEL[3:0] = 1000b		3.59	3.70	3.81	V
	LVI_A/D_SEL[3:0] = 1001b		3.84	3.95	4.07	V
	LVI_A/D_SEL[3:0] = 1010b		4.08	4.20	4.33	V
	LVI_A/D_SEL[3:0] = 1011b		4.32	4.45	4.59	V
	LVI_A/D_SEL[3:0] = 1100b		4.56	4.70	4.84	V
	LVI_A/D_SEL[3:0] = 1101b		4.83	4.98	5.13	V
	LVI_A/D_SEL[3:0] = 1110b		5.05	5.21	5.37	V
	LVI_A/D_SEL[3:0] = 1111b		5.30	5.47	5.63	V
HVI	Trip voltage		5.57	5.75	5.92	V

Table 11-68. Voltage Monitors AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Response time ^[68]		–	–	1	μs

Note

68. Based on device characterization (Not production tested).

11.9.5 External Clock Reference

Table 11-81. External Clock Reference AC Specifications^[76]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at $V_{DDIO}/2$	30	50	70	%
	Input edge rate	V_{IL} to V_{IH}	0.5	–	–	V/ns

11.9.6 Phase-Locked Loop

Table 11-82. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 24 MHz	–	200	–	μA

Table 11-83. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{PLLIN}	PLL input frequency ^[77]		1	–	48	MHz
	PLL intermediate frequency ^[78]	Output of prescaler	1	–	3	MHz
F _{PLLOUT}	PLL output frequency ^[77]		24	–	50	MHz
	Lock time at startup		–	–	250	μs
J _{period-rms}	Jitter (rms) ^[76]		–	–	250	ps

Notes

76. Based on device characterization (Not production tested).

77. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.

78. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T _A	Operating ambient temperature		–40	25.00	85	°C
T _J	Operating junction temperature		–40	–	100	°C
T _{JA}	Package θ_{JA} (48-pin SSOP)		–	49	–	°C/Watt
T _{JA}	Package θ_{JA} (48-pin QFN)		–	14	–	°C/Watt
T _{JA}	Package θ_{JA} (68-pin QFN)		–	15	–	°C/Watt
T _{JA}	Package θ_{JA} (100-pin TQFP)		–	34	–	°C/Watt
T _{JC}	Package θ_{JC} (48-pin SSOP)		–	24	–	°C/Watt
T _{JC}	Package θ_{JC} (48-pin QFN)		–	15	–	°C/Watt
T _{JC}	Package θ_{JC} (68-pin QFN)		–	13	–	°C/Watt
T _{JC}	Package θ_{JC} (100-pin TQFP)		–	10	–	°C/Watt

Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
48-pin SSOP	MSL 3
48-pin QFN	MSL 3
68-pin QFN	MSL 3
100-pin TQFP	MSL 3

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
μA	microamperes
μF	microfarads
μH	microhenrys
μs	microseconds
μV	microvolts
μW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts

Description Title: PSoC® 3: CY8C34 Family Datasheet Programmable System-on-Chip (PSoC®) (continued)
Document Number: 001-53304

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*V	4708125	03/31/2015	MKEA	Added INL4 and DNL4 specs in VDAC DC Specifications . Updated Figure 6-11 . Added second note after Figure 6-4 . Added a reference to Fig 6-1 in Section 6.1.1 and Section 6.1.2 . Updated Section 6.2.2 . Added Section 7.8.1 . Updated Boost specifications.
*W	4807497	06/23/2015	MKEA	Added reference to code examples in More Information. Updated typ value of TWRITE from 2 to 10 in EEPROM AC specs table. Changed "Device supply for USB operation" to "Device supply (VDDD) for USB operation" in USB DC Specifications. Clarified power supply sequencing and margin for VDDA and VDDD. Updated Serial Wire Debug Interface with limitations of debugging on Port 15. Updated Section 11.7.5. Updated Delta-sigma ADC DC Specifications
*X	4932879	09/24/2015	MKEA	Changed the Regulator Output Capacitor min and max from "-" to 0.9 and 1.1, respectively. Added reference to AN54439 in Section 11.9.3. Added MHz ECO DC specs table. Removed references to IPOR rearm issues in Section 6.3.1.1. Table 6-1: Changed DSI Fmax to 33 MHz. Figure 6-1: Changed External I/O or DSI to 0-33 MHz. Table 11-10: Changed Fgpioin Max to 33 MHz. Table 11-12: Changed Fsioin Max to 33 MHz.
*Y	5322536	06/27/2016	MKEA	Updated More Information . Corrected typos in External Electrical Connections . Added links to CAD Libraries in Section 2.