

Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3446lti-074t

1. Architectural Overview

Introducing the CY8C34 family of ultra low-power, flash Programmable System-on-Chip (PSoC®) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5 platform. The CY8C34 family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.

Figure 1-1. Simplified Block Diagram

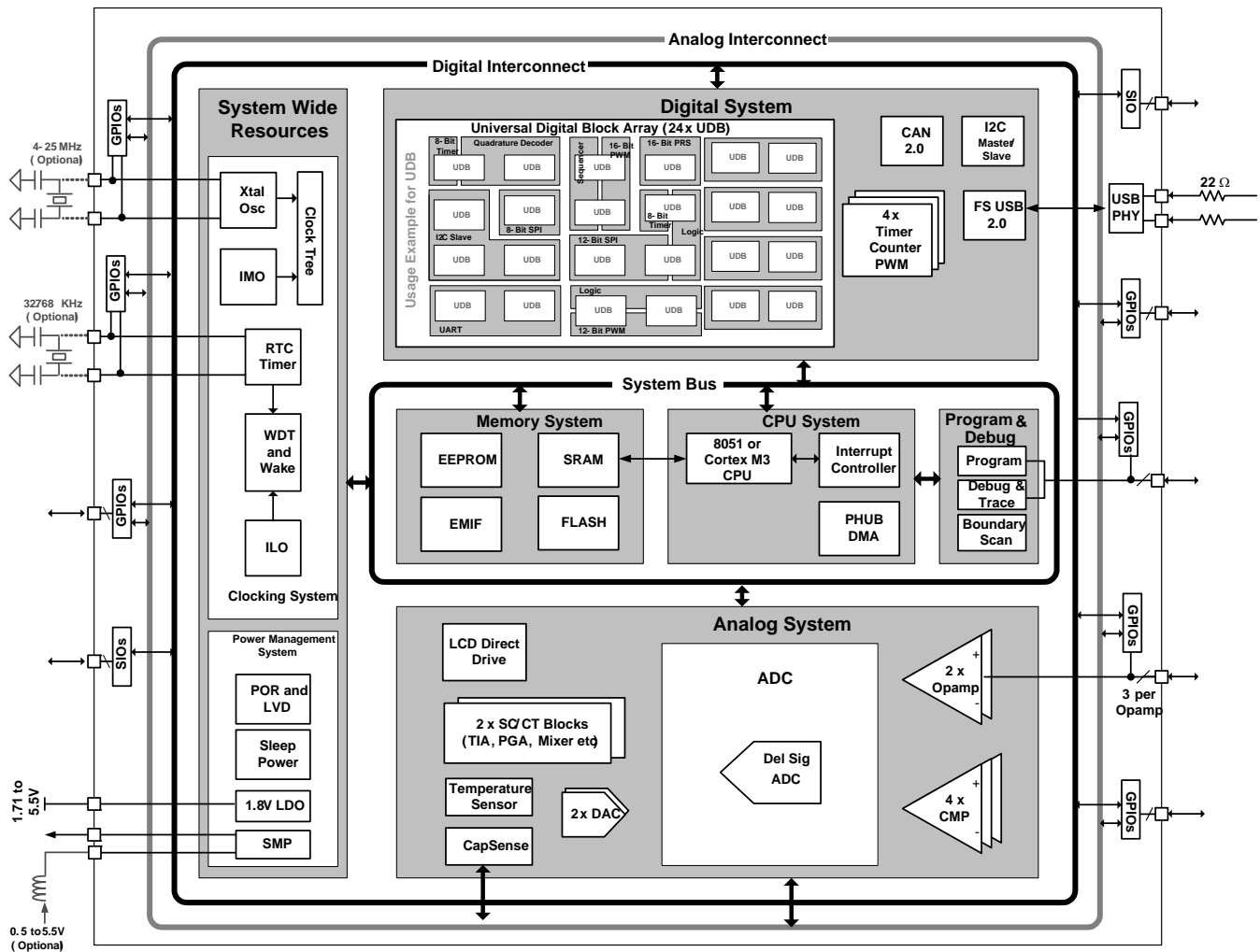


Figure 1-1 illustrates the major components of the CY8C34 family. They are:

- 8051 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem

■ Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the digital system interconnect (DSI). It also provides functional flexibility through an array of small, fast, low-power UDBs. PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. You can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/PLD functionality, together with a small state machine engine to support a wide variety of peripherals.

Figure 2-3. 48-pin SSOP Part Pinout

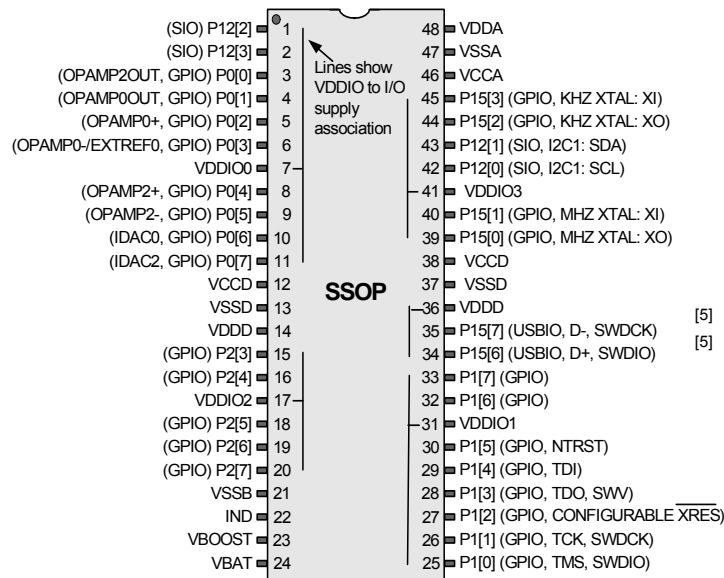
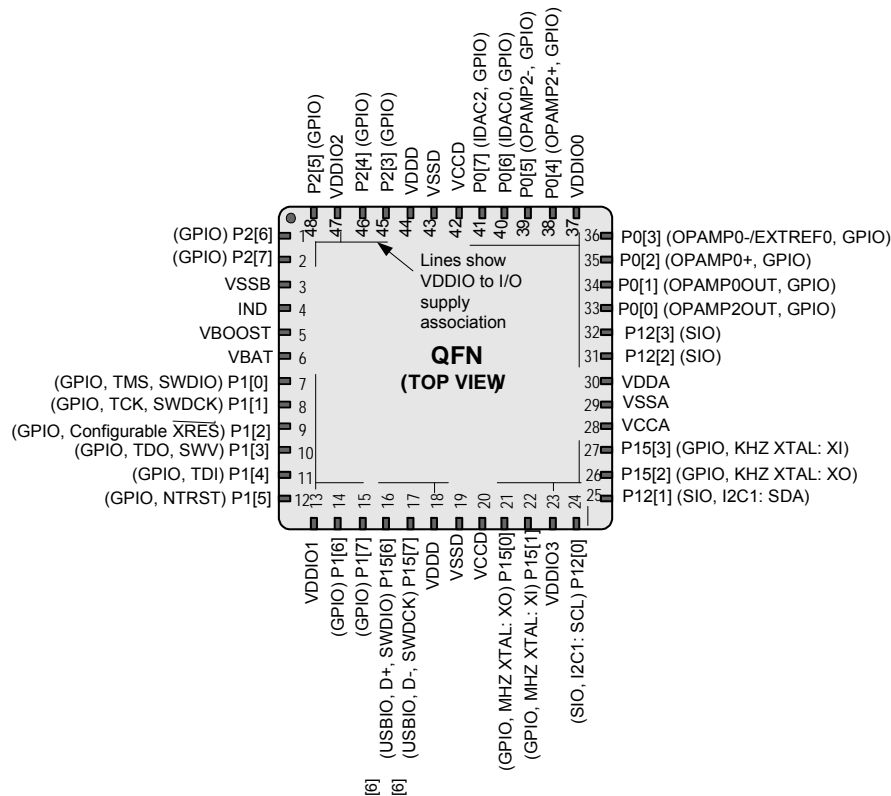


Figure 2-4. 48-pin QFN Part Pinout^[7]



Notes

- Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
- Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
- The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see [AN72845](#), Design Guidelines for QFN Devices.

USBIO, D+

Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D-

Provides D- connection directly to a USB 2.0 bus. May be used as a digital I/O pin. Pins are No Connect (NC) on devices without USB.

VBOOST

Power sense connection to boost pump.

VBAT

Battery supply to boost pump.

VCCA.

Output of the analog core regulator or the input to the analog core. Requires a 1uF capacitor to VSSA. The regulator output is not designed to drive external circuits. **Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V.** When using the internal core regulator, (internally regulated mode, the default), do not tie any power to this pin. For details see [Power System](#) on page 30.

VCCD.

Output of the digital core regulator or the input to the digital core. The two VCCD pins must be shorted together, with the trace between them as short as possible, and a 1uF capacitor to VSSD. The regulator output is not designed to drive external circuits. **Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V.** When using the internal core regulator (internally regulated mode, the default), do not tie any power to this pin. For details see [Power System](#) on page 30.

VDDA

Supply for all analog peripherals and analog core regulator. **VDDA must be the highest voltage present on the device. All other supply pins must be less than or equal to VDDA.**

VDDD

Supply for all digital peripherals and digital core regulator. VDDD must be less than or equal to VDDA.

VSSA

Ground for all analog peripherals.

VSSB

Ground connection for boost pump.

VSSD

Ground for all digital logic and I/O pins.

VDDIO0, VDDIO1, VDDIO2, VDDIO3

Supply for I/O pins. See pinouts for specific I/O pin to VDDIO mapping. Each VDDIO must be tied to a valid operating voltage (1.71 V to 5.5 V), and must be less than or equal to VDDA.

$\overline{\text{XRES}}$ (and configurable $\overline{\text{XRES}}$)

External reset pin. Active low with internal pull-up. Pin P1[2] may be configured to be a XRES pin; see [“Nonvolatile Latches \(NVLS\)”](#) on page 23.

4. CPU

4.1 8051 CPU

The CY8C34 devices use a single cycle 8051 CPU, which is fully compatible with the original MCS-51 instruction set. The CY8C34 family uses a pipelined RISC architecture, which executes most instructions in 1 to 2 cycles to provide peak performance of up to 24 MIPS with an average of 2 cycles per instruction. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor.

The 8051 CPU subsystem includes these features:

- Single cycle 8051 CPU
- Up to 64 KB of flash memory, up to 2 KB of EEPROM, and up to 8 KB of SRAM
- 512-byte instruction cache between CPU and flash
- Programmable nested vector interrupt controller
- Direct memory access (DMA) controller
- Peripheral HUB (PHUB)
- External memory interface (EMIF)

4.2 Addressing Modes

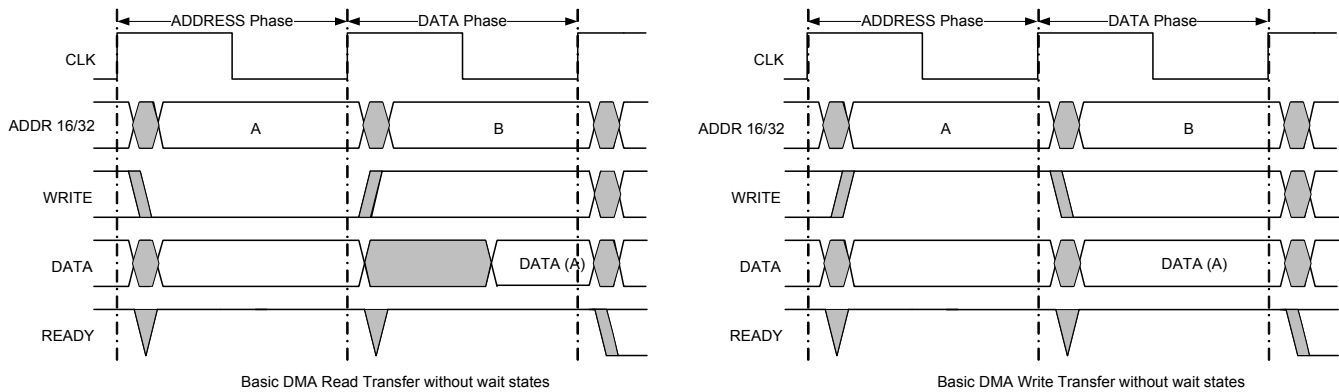
The following addressing modes are supported by the 8051:

- Direct Addressing: The operand is specified by a direct 8-bit address field. Only the internal RAM and the SFRs can be accessed using this mode.
- Indirect Addressing: The instruction specifies the register which contains the address of the operand. The registers R0 or R1 are used to specify the 8-bit address, while the data pointer (DPTR) register is used to specify the 16-bit address.
- Register Addressing: Certain instructions access one of the registers (R0 to R7) in the specified register bank. These instructions are more efficient because there is no need for an address field.
- Register Specific Instructions: Some instructions are specific to certain registers. For example, some instructions always act on the accumulator. In this case, there is no need to specify the operand.
- Immediate Constants: Some instructions carry the value of the constants directly instead of an address.
- Indexed Addressing: This type of addressing can be used only for a read of the program memory. This mode uses the Data Pointer as the base and the accumulator value as an offset to read a program memory.
- Bit Addressing: In this mode, the operand is one of 256 bits.

4.4.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location). The basic timing diagrams of DMA read and write cycles are shown in [Figure 4-1](#). For more description on other transfer modes, refer to the Technical Reference Manual.

Figure 4-1. DMA Timing Diagram



4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU

can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts

6: CPU acknowledges the interrupt request

7: ISR address is read by CPU for branching

8, 9: PEND and POST bits are cleared respectively after receiving the IRA from core

10: IRA bit is cleared after completing the current instruction and starting the instruction execution from ISR location (takes 7 cycles)

11: IRC is set to indicate the completion of ISR, Active int. status is restored with previous status

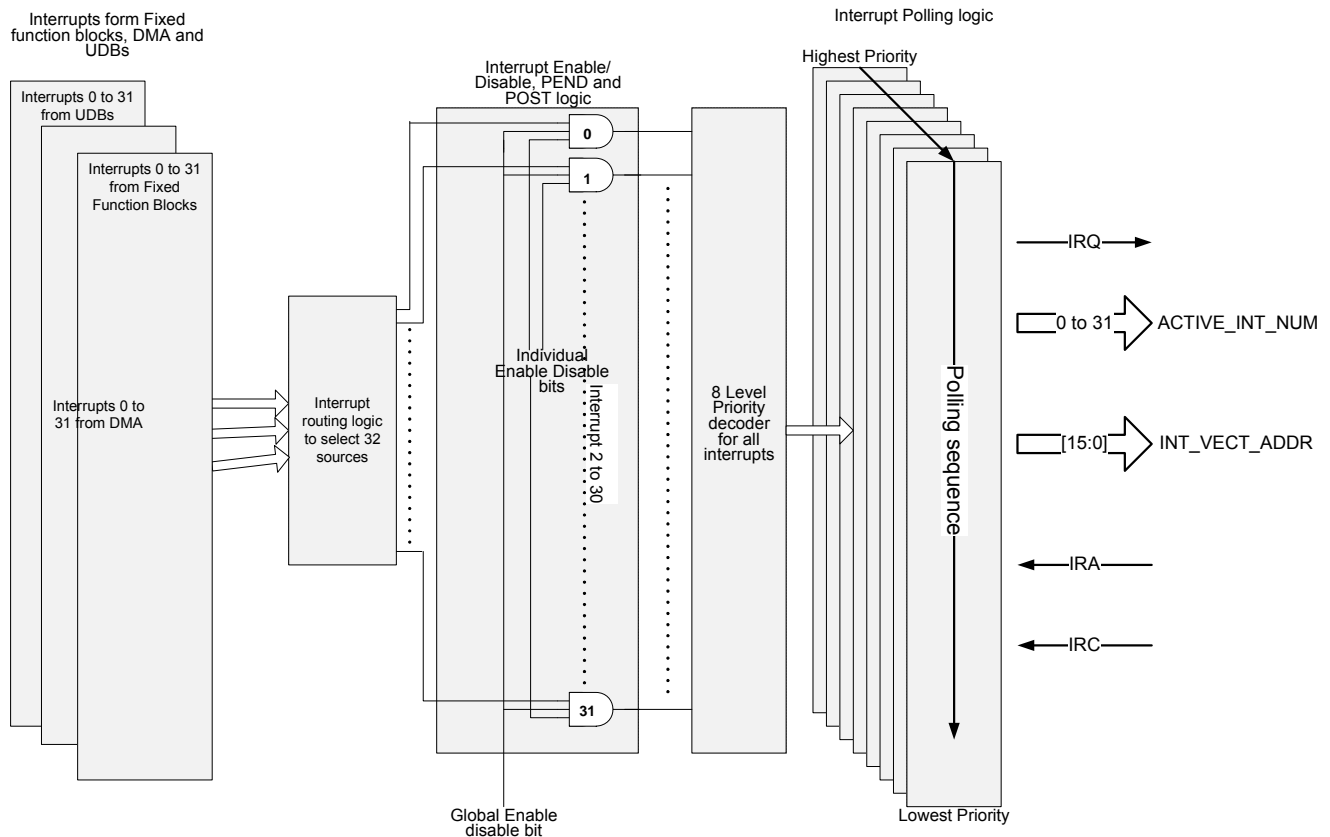
The total interrupt latency (ISR execution)

= POST + PEND + IRQ + IRA + Completing current instruction and branching

= 1+1+1+2+7 cycles

= 12 cycles

Figure 4-3. Interrupt Structure



5. Memory

5.1 Static RAM

CY8C34 Static RAM (SRAM) is used for temporary data storage. Up to 8 KB of SRAM is provided and can be accessed by the 8051 or the DMA controller. See [Memory Map](#) on page 25. Simultaneous access of SRAM by the 8051 and the DMA controller is possible if different 4-KB blocks are accessed.

5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data, bulk data storage, and optional ECC data. The main flash memory area contains up to 64 KB of user program space.

Up to an additional 8 KB of flash space is available for Error Correcting Codes (ECC). If ECC is not used this space can store device configuration data and bulk user data. User code may not be run out of the ECC flash memory section. ECC can correct one bit error and detect two bit errors per 8 bytes of firmware memory; an interrupt can be generated when an error is detected.

The CPU reads instructions located in flash through a cache controller. This improves instruction execution rate and reduces system power consumption by requiring less frequent flash access. The cache has 8 lines at 64 bytes per line for a total of 512 bytes. It is fully associative, automatically controls flash power, and can be enabled or disabled. If ECC is enabled, the cache controller also performs error checking and correction, and interrupt generation.

Flash programming is performed through a special interface and preempts code execution out of flash. The flash programming interface performs flash erasing, programming and setting code protection levels. Flash in-system serial programming (ISSP), typically used for production programming, is possible through both the SWD and JTAG interfaces. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as I²C, USB, UART, and SPI, or any communications protocol.

5.3 Flash Security

All PSoC devices include a flexible flash-protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of ECC or configuration data. A total of up to 256 blocks is provided on 64-KB flash devices.

The device offers the ability to assign one of four protection levels to each row of flash. [Table 5-1](#) lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a boot loader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the

“Device Security” section on page 68). For more information about how to take full advantage of the security features in PSoC, see the [PSoC 3 TRM](#).

Table 5-1. Flash Protection

Protection Setting	Allowed	Not Allowed
Unprotected	External read and write + internal read and write	-
Factory Upgrade	External write + internal read and write	External read
Field Upgrade	Internal read and write	External read and write
Full Protection	Internal read	External read and write + internal write

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

5.4 EEPROM

PSoC EEPROM memory is a byte-addressable nonvolatile memory. The CY8C34 has up to 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into 128 rows of 16 bytes each. The factory default values of all EEPROM bytes are 0.

Because the EEPROM is mapped to the 8051 xdata space, the CPU cannot execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

It can take as much as 20 milliseconds to write to EEPROM or flash. During this time the device should not be reset, or unexpected changes may be made to portions of EEPROM or flash. Reset sources (see [Section 6.3.1](#)) include XRES pin, software reset, and watchdog; care should be taken to make sure that these are not inadvertently activated. In addition, the low voltage detect circuits should be configured to generate an interrupt instead of a reset.

5.7 Memory Map

The CY8C34 8051 memory map is very similar to the MCS-51 memory map.

5.7.1 Code Space

The CY8C34 8051 code space is 64 KB. Only main flash exists in this space. See the “Flash Program Memory” section on page 22.

5.7.2 Internal Data Space

The CY8C34 8051 internal data space is 384 bytes, compressed within a 256-byte space. This space consists of 256 bytes of RAM (in addition to the SRAM mentioned in [Static RAM](#) on page 22) and a 128-byte space for Special Function Registers (SFRs). See [Figure 5-2](#). The lowest 32 bytes are used for 4 banks of registers R0-R7. The next 16 bytes are bit-addressable.

Figure 5-2. 8051 Internal Data Space

0x00 0x1F	4 Banks, R0-R7 Each	
0x20 0x2F	Bit-Addressable Area	
0x30 0x7F	Lower Core RAM Shared with Stack Space (direct and indirect addressing)	
0x80 0xFF	Upper Core RAM Shared with Stack Space (indirect addressing)	SFR Special Function Registers (direct addressing)

In addition to the register or bit address modes used with the lower 48 bytes, the lower 128 bytes can be accessed with direct or indirect addressing. With direct addressing mode, the upper 128 bytes map to the SFRs. With indirect addressing mode, the upper 128 bytes map to RAM. Stack operations use indirect addressing; the 8051 stack space is 256 bytes. See the “Addressing Modes” section on page 12

5.7.3 SFRs

The Special Function Register (SFR) space provides access to frequently accessed registers. The memory map for the SFR memory space is shown in [Table 5-4](#).

Table 5-4. SFR Map

Address	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	SFRPRT15DR	SFRPRT15PS	SFRPRT15SEL					
0xF0	B		SFRPRT12SEL					
0xE8	SFRPRT12DR	SFRPRT12PS	MXAX					
0xE0	ACC							
0xD8	SFRPRT6DR	SFRPRT6PS	SFRPRT6SEL					
0xD0	PSW							
0xC8	SFRPRT5DR	SFRPRT5PS	SFRPRT5SEL					
0xC0	SFRPRT4DR	SFRPRT4PS	SFRPRT4SEL					
0xB8								
0xB0	SFRPRT3DR	SFRPRT3PS	SFRPRT3SEL					
0xA8	IE							
0xA0	P2AX		SFRPRT1SEL					
0x98	SFRPRT2DR	SFRPRT2PS	SFRPRT2SEL					
0x90	SFRPRT1DR	SFRPRT1PS		DPX0		DPX1		
0x88		SFRPRT0PS	SFRPRT0SEL					
0x80	SFRPRT0DR	SP	DPL0	DPH0	DPL1	DPH1	DPS	

The CY8C34 family provides the standard set of registers found on industry standard 8051 devices. In addition, the CY8C34 devices add SFRs to provide direct access to the I/O ports on the device. The following sections describe the SFRs added to the CY8C34 family.

5.7.4 XData Space Access SFRs

The 8051 core features dual DPTR registers for faster data transfer operations. The data pointer select SFR, DPS, selects which data pointer register, DPTR0 or DPTR1, is used for the following instructions:

- MOVX @DPTR, A
- MOVX A, @DPTR
- MOVC A, @A+DPTR
- JMP @A+DPTR
- INC DPTR
- MOV DPTR, #data16

The extended data pointer SFRs, DPX0, DPX1, MXAX, and P2AX, hold the most significant parts of memory addresses during access to the xdata space. These SFRs are used only with the MOVX instructions.

During a MOVX instruction using the DPTR0/DPTR1 register, the most significant byte of the address is always equal to the contents of DPX0/DPX1. During a MOVX instruction using the R0 or R1 register, the most significant byte of the address is always equal to the contents of MXAX, and the next most significant byte is always equal to the contents of P2AX.

5.7.5 I/O Port SFRs

The I/O ports provide digital input sensing, output drive, pin interrupts, connectivity for analog inputs and outputs, LCD, and access to peripherals through the DSI. Full information on I/O ports is found in [I/O System and Routing](#) on page 36.

I/O ports are linked to the CPU through the PHUB and are also available in the SFRs. Using the SFRs allows faster access to a limited set of I/O port registers, while using the PHUB allows boot configuration and access to all I/O port registers.

Each SFR supported I/O port provides three SFRs:

- SFRPRTxDR sets the output data state of the port (where x is port number and includes ports 0-6, 12 and 15)
- The SFRPRTxSEL selects whether the PHUB PRTxDR register or the SFRPRTxDR controls each pin's output buffer within the port. If a SFRPRTxSEL[y] bit is high, the corresponding SFRPRTxDR[y] bit sets the output state for that pin. If a SFRPRTxSEL[y] bit is low, the corresponding PRTxDR[y] bit sets the output state of the pin (where y varies from 0 to 7).
- The SFRPRTxPS is a read only register that contains pin state values of the port pins.

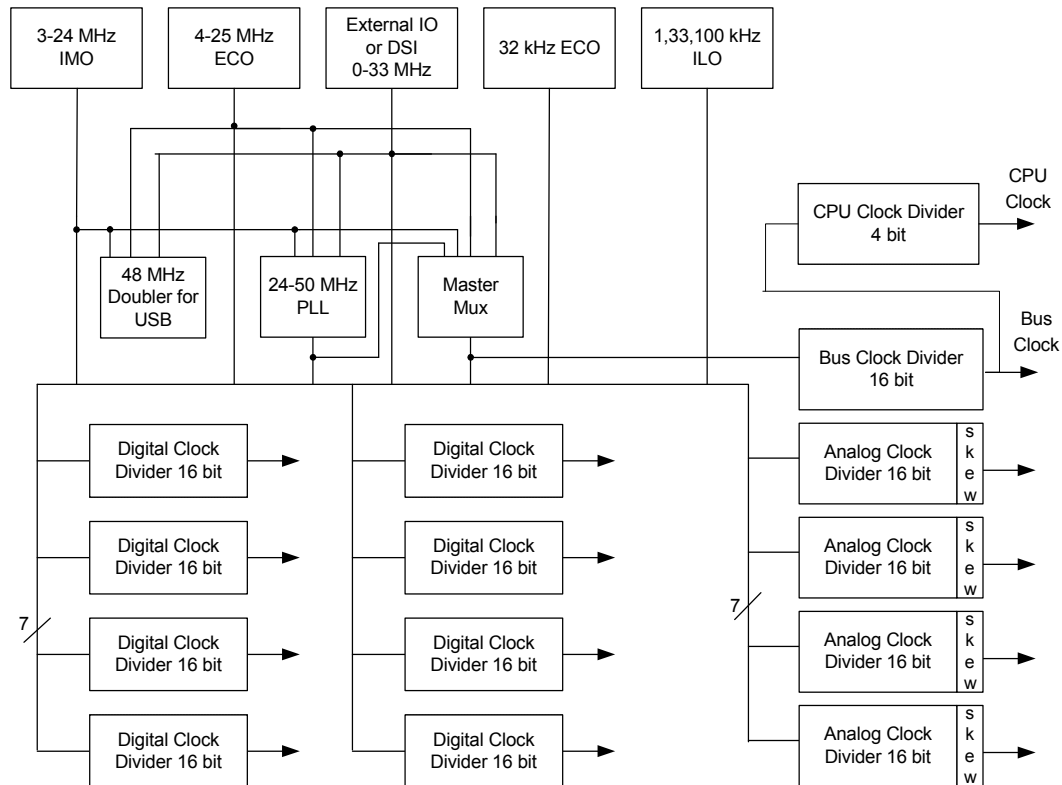
5.7.5.1 xdata Space

The 8051 xdata space is 24-bit, or 16 MB in size. The majority of this space is not “external”—it is used by on-chip components. See [Table 5-5](#). External, that is, off-chip, memory can be accessed using the EMIF. See [External Memory Interface](#) on page 24.

Table 5-5. XDATA Data Address Map

Address Range	Purpose
0x00 0000 – 0x00 1FFF	SRAM
0x00 4000 – 0x00 42FF	Clocking, PLLs, and oscillators
0x00 4300 – 0x00 43FF	Power management
0x00 4400 – 0x00 44FF	Interrupt controller
0x00 4500 – 0x00 45FF	Ports interrupt control
0x00 4700 – 0x00 47FF	Flash programming interface
0x00 4800 – 0x00 48FF	Cache controller
0x00 4900 – 0x00 49FF	I ² C controller
0x00 4E00 – 0x00 4EFF	Decimator
0x00 4F00 – 0x00 4FFF	Fixed timer/counter/PWMs
0x00 5000 – 0x00 51FF	I/O ports control
0x00 5400 – 0x00 54FF	External Memory Interface (EMIF) control registers
0x00 5800 – 0x00 5FFF	Analog Subsystem interface
0x00 6000 – 0x00 60FF	USB controller
0x00 6400 – 0x00 6FFF	UDB Working Registers
0x00 7000 – 0x00 7FFF	PHUB configuration
0x00 8000 – 0x00 8FFF	EEPROM
0x00 A000 – 0x00 A400	CAN
0x01 0000 – 0x01 FFFF	Digital Interconnect configuration
0x05 0220 – 0x05 02F0	Debug controller
0x08 0000 – 0x08 1FFF	Flash ECC bytes
0x80 0000 – 0xFF FFFF	External Memory Interface

Figure 6-1. Clocking Subsystem



6.1.1 Internal Oscillators

Figure 6-1 shows that there are two internal oscillators. They can be routed directly or divided. The direct routes may not have a 50% duty cycle. Divided clocks have a 50% duty cycle.

6.1.1.1 Internal Main Oscillator

In most designs the IMO is the only clock source required, due to its ± 2 -percent accuracy. The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from ± 2 percent at 3 MHz, up to ± 4 percent at 24 MHz. The IMO, in conjunction with the PLL, allows generation of other clocks up to the device's maximum frequency (see [Phase-Locked Loop](#)).

The IMO provides clock outputs at 3, 6, 12, and 24 MHz.

6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works at input frequency of 24 MHz, providing 48 MHz for the USB. It can be configured to use a clock from the IMO, MHzECO, or the DSI (external pin).

6.1.1.3 Phase-Locked Loop

The PLL allows low-frequency, high-accuracy clocks to be multiplied to higher frequencies. This is a trade off between higher clock frequency and accuracy and, higher power consumption and increased startup time.

The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 50 MHz. Its input and feedback dividers supply 4032 discrete ratios to create almost any desired clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz, where it is most accurate to generate the other clocks up to the device's maximum frequency.

The PLL achieves phase lock within 250 μ s (verified by bit setting). It can be configured to use a clock from the IMO, MHzECO or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low-power modes.

6.1.1.4 Internal Low-Speed Oscillator

The ILO provides clock frequencies for low-power consumption, including the watchdog timer, and sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz.

The 1 kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to low-power supervisory operations such as the watchdog timer and long sleep intervals using the central timewheel (CTW).

The central timewheel is a 1 kHz, free running, 13-bit counter clocked by the ILO. The central timewheel is always enabled except in hibernate mode and when the CPU is stopped during

Figure 6-10. SIO Input/Output Block Diagram

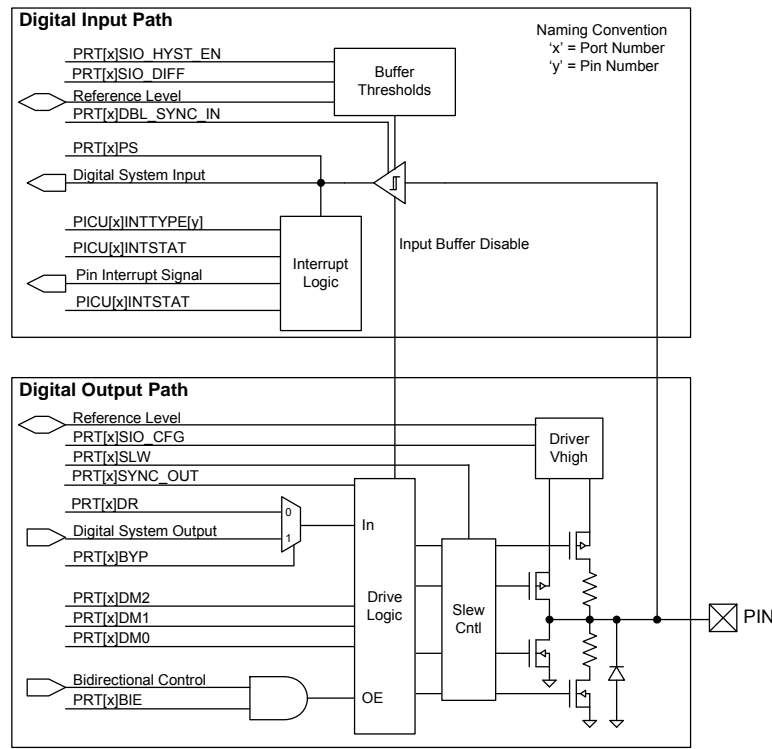
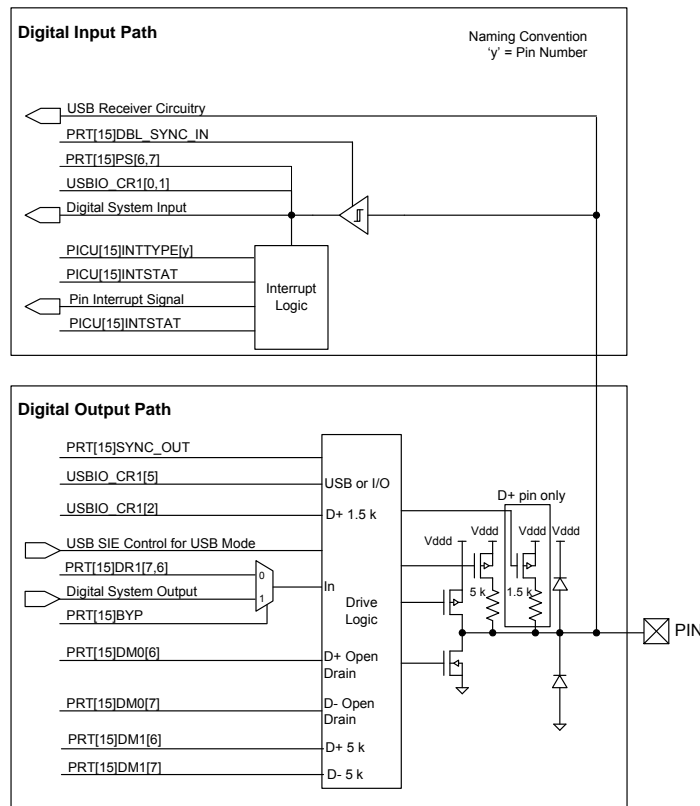


Figure 6-11. USBIO Block Diagram



6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-6. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-12 depicts a simplified pin view based on each of the eight drive modes. Table 6-6 shows the I/O pin's drive state based on the port data register value or digital array signal

if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-12. Drive Mode

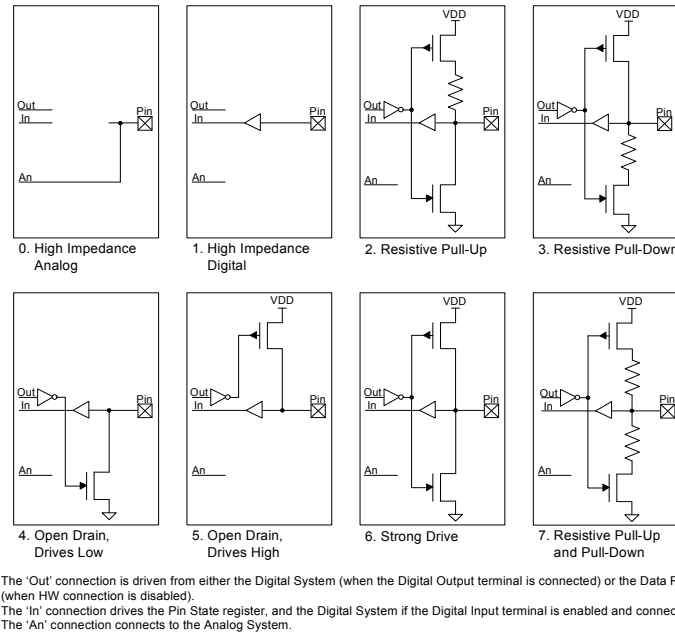


Table 6-6. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedance analog	0	0	0	High Z	High Z
1	High Impedance digital	0	0	1	High Z	High Z
2	Resistive pull-up ^[14]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down ^[14]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down ^[14]	1	1	1	Res High (5K)	Res Low (5K)

Note

¹⁴. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

The USBIO pins (P15[7] and P15[6]), when enabled for I/O mode, have limited drive mode control. The drive mode is set using the PRT15.DM0[7, 6] register. A resistive pull option is also available at the USBIO pins, which can be enabled using the PRT15.DM1[7, 6] register. When enabled for USB mode, the drive mode control has no impact on the configuration of the USB pins. Unlike the GPIO and SIO configurations, the port wide configuration registers do not configure the USB drive mode bits. Table 6-7 shows the drive mode configuration for the USBIO pins.

Table 6-7. USBIO Drive Modes (P15[7] and P15[6])

PRT15.DM1[7,6] Pull up enable	PRT15.DM0[7,6] Drive Mode enable	PRT15.DR[7,6] = 1	PRT15.DR[7,6] = 0	Description
0	0	High Z	Strong Low	Open Drain, Strong Low
0	1	Strong High	Strong Low	Strong Outputs
1	0	Res High (5k)	Strong Low	Resistive Pull Up, Strong Low
1	1	Strong High	Strong Low	Strong Outputs

■ High impedance analog

The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

■ High impedance digital

The input buffer is enabled for digital signal input. This is the standard high impedance (High Z) state recommended for digital inputs.

■ Resistive pull-up or resistive pull-down

Resistive pull-up or pull-down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

■ Open drain, drives high and open drain, drives low

Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I²C bus signal lines.

■ Strong drive

Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

■ Resistive pull-up and pull-down

Similar to the resistive pull-up and resistive pull-down modes except the pin is always in series with a resistor. The high data state is pull-up while the low data state is pull-down. This mode is most often used when other signals that may cause shorts can drive the bus. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

6.4.3 Bidirectional Mode

High-speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRT×DM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRT×SLW registers.

8.2.3 Start of Conversion Input

The SoC signal is used to start an ADC conversion. A digital clock or UDB output can be used to drive this input. It can be used when the sampling period must be longer than the ADC conversion time or when the ADC must be synchronized to other hardware. This signal is optional and does not need to be connected if ADC is running in a continuous mode.

8.2.4 End of Conversion Output

The EoC signal goes high at the end of each ADC conversion. This signal may be used to trigger either an interrupt or DMA request.

8.3 Comparators

The CY8C34 family of devices contains four comparators in a device. Comparators have these features:

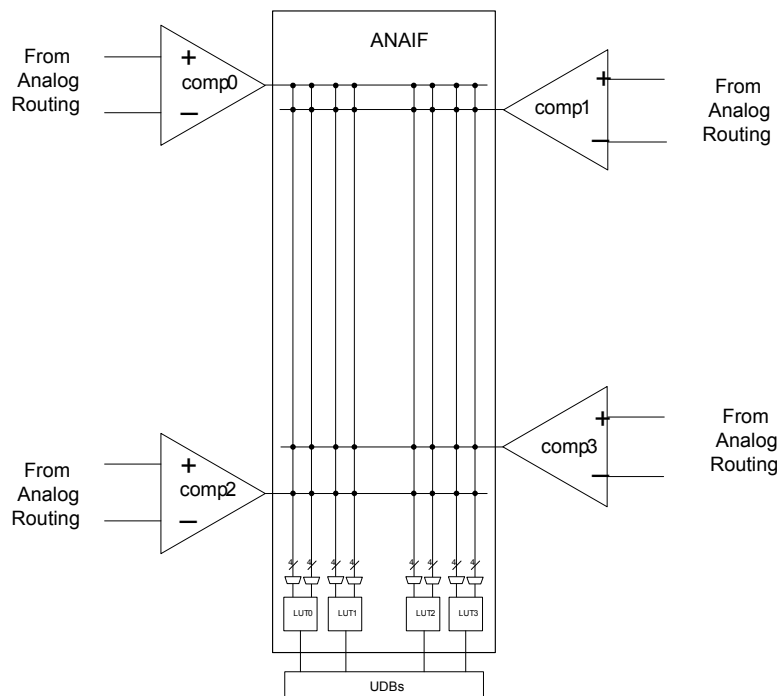
- Input offset factory trimmed to less than 5 mV
- Rail-to-rail common mode input range (V_{SSA} to V_{DDA})

- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low-power
- Comparator outputs can be routed to lookup tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB Digital System Interface.

Figure 8-5. Analog Comparator



10. Development Support

The CY8C34 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit psoc.cypress.com/getting-started to find out more.

10.1 Documentation

A suite of documentation, supports the CY8C34 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component data sheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

10.2 Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

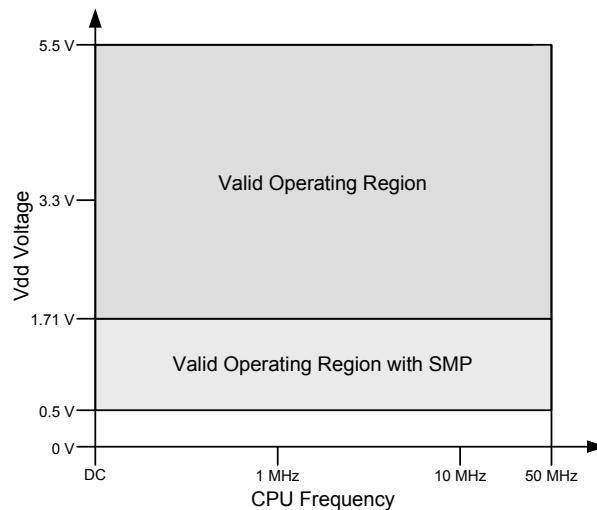
10.3 Tools

With industry standard cores, programming, and debugging interfaces, the CY8C34 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 11-3. AC Specifications^[33]

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{CPU}	CPU frequency	1.71 V ≤ V _{DD} ≤ 5.5 V	DC	–	50.01	MHz
F _{BUSCLK}	Bus frequency	1.71 V ≤ V _{DD} ≤ 5.5 V	DC	–	50.01	MHz
Svdd	V _{DD} ramp rate	–	–	–	0.066	V/μs
T _{IO_INIT}	Time from V _{DD} /V _{DDA} /V _{CCD} /V _{CCA} ≥ IPOR to I/O ports set to their reset states	–	–	–	10	μs
T _{STARTUP}	Time from V _{DD} /V _{DDA} /V _{CCD} /V _{CCA} ≥ PRES to CPU executing code at reset vector	V _{CCA} /V _{CCD} = regulated from V _{DDA} /V _{DD} , no PLL used, IMO boot mode (12 MHz typ.)	–	–	74	μs
T _{SLEEP}	Wakeup from sleep mode – Application of non-LVD interrupt to beginning of execution of next CPU instruction		–	–	15	μs
T _{HIBERNATE}	Wakeup from hibernate mode – Application of external interrupt to beginning of execution of next CPU instruction		–	–	100	μs

Figure 11-4. F_{CPU} vs. V_{DD}



Note

33. Based on device characterization (Not production tested).

11.3.3 Inductive Boost Regulator

Unless otherwise specified, operating conditions are: $V_{BAT} = 0.5\text{ V} - 3.6\text{ V}$, $V_{OUT} = 1.8\text{ V} - 5.0\text{ V}$, $I_{OUT} = 0\text{ mA} - 50\text{ mA}$, $L_{BOOST} = 4.7\text{ }\mu\text{H} - 22\text{ }\mu\text{H}$, $C_{BOOST} = 22\text{ }\mu\text{F} \parallel 3 \times 1.0\text{ }\mu\text{F} \parallel 3 \times 0.1\text{ }\mu\text{F}$, $C_{BAT} = 22\text{ }\mu\text{F}$, $I_F = 1.0\text{ A}$. Unless otherwise specified, all charts and graphs show typical values.

Table 11-6. Inductive Boost Regulator DC Specifications

Parameter	Description	Conditions		Min	Typ	Max	Units
V _{OUT}	Boost output voltage ^[34]	vsel = 1.8 V in register BOOST_CR0		1.71	1.8	1.89	V
		vsel = 1.9 V in register BOOST_CR0		1.81	1.90	2.00	V
		vsel = 2.0 V in register BOOST_CR0		1.90	2.00	2.10	V
		vsel = 2.4 V in register BOOST_CR0		2.16	2.40	2.64	V
		vsel = 2.7 V in register BOOST_CR0		2.43	2.70	2.97	V
		vsel = 3.0 V in register BOOST_CR0		2.70	3.00	3.30	V
		vsel = 3.3 V in register BOOST_CR0		2.97	3.30	3.63	V
		vsel = 3.6 V in register BOOST_CR0		3.24	3.60	3.96	V
		vsel = 5.0 V in register BOOST_CR0		4.50	5.00	5.50	V
V _{BAT}	Input voltage to boost ^[35]	I _{OUT} = 0 mA–5 mA	vsel = 1.8 V–2.0 V, T _A = 0 °C–70 °C	0.5	–	0.8	V
		I _{OUT} = 0 mA–15 mA	vsel = 1.8 V–5.0 V ^[36] , T _A = –10 °C–85 °C	1.6	–	3.6	V
		I _{OUT} = 0 mA–25 mA	vsel = 1.8 V–2.7 V, T _A = –10 °C–85 °C	0.8	–	1.6	V
		I _{OUT} = 0 mA–50 mA	vsel = 1.8 V–3.3 V ^[36] , T _A = –40 °C–85 °C	1.8	–	2.5	V
			vsel = 1.8 V–3.3 V ^[36] , T _A = –10 °C–85 °C	1.3	–	2.5	V
			vsel = 2.5 V–5.0 V ^[36] , T _A = –10 °C–85 °C	2.5	–	3.6	V
		I _{OUT}	Output current	T _A = 0 °C–70 °C	V _{BAT} = 0.5 V–0.8 V	0	–
T _A = –10 °C–85 °C	V _{BAT} = 1.6 V–3.6 V			0	–	15	mA
	V _{BAT} = 0.8 V–1.6 V			0	–	25	mA
	V _{BAT} = 1.3 V–2.5 V			0	–	50	mA
	V _{BAT} = 2.5 V–3.6 V			0	–	50	mA
T _A = –40 °C–85 °C	V _{BAT} = 1.8 V–2.5 V			0	–	50	mA
I _{LPK}	Inductor peak current					–	–
I _Q	Quiescent current	Boost active mode		–	250	–	μA
		Boost sleep mode, I _{OUT} < 1 μA		–	25	–	μA
Reg _{LOAD}	Load regulation			–	–	10	%
Reg _{LINE}	Line regulation			–	–	10	%

Notes

34. Listed v_{sel} options are characterized. Additional v_{sel} options are valid and guaranteed by design.

35. The boost will start at all valid V_{BAT} conditions including down to $V_{BAT} = 0.5\text{ V}$.

36. If V_{BAT} is greater than or equal to V_{OUT} boost setting, then V_{OUT} will be less than V_{BAT} due to resistive losses in the boost circuit.

Table 11-7. Recommended External Components for Boost Circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
L_{BOOST}	Boost inductor	4.7 μH nominal	3.7	4.7	5.7	μH
		10 μH nominal	8.0	10.0	12.0	μH
		22 μH nominal	17.0	22.0	27.0	μH
C_{BOOST}	Total capacitance sum of V_{DD} , V_{DDA} , V_{DDIO} ^[37]		17.0	26.0	31.0	μF
C_{BAT}	Battery filter capacitor		17.0	22.0	27.0	μF
I_{F}	Schottky diode average forward current		1.0	–	–	A
V_{R}	Schottky reverse voltage		20.0	–	–	V

Figure 11-8. T_{A} range over V_{BAT} and V_{OUT}

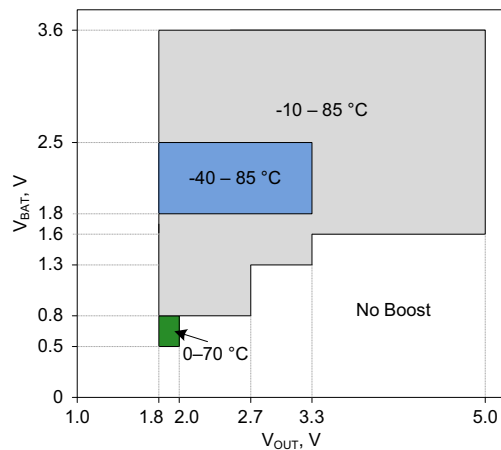


Figure 11-9. I_{OUT} range over V_{BAT} and V_{OUT}

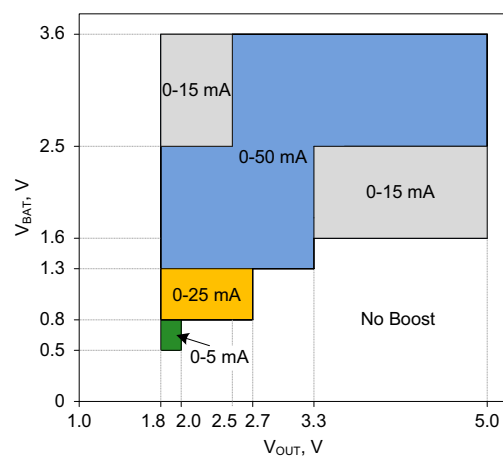
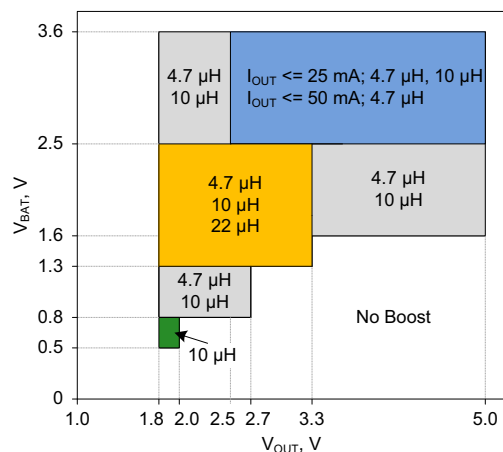


Figure 11-10. L_{BOOST} values over V_{BAT} and V_{OUT}



Note

37. Based on device characterization (Not production tested).

**Figure 11-24. USBIO Output Rise and Fall Times, GPIO Mode,
 $V_{DD} = 3.3\text{ V}$, 25 pF Load**

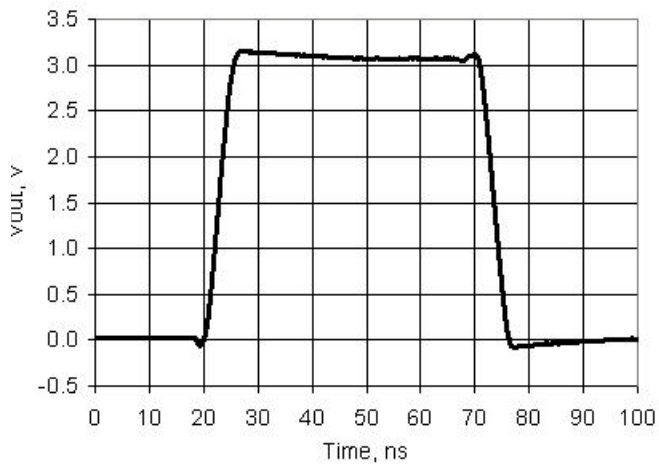


Table 11-16. USB Driver AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	V_{USB_5} , $V_{USB_3.3}$, see USB DC Specifications on page 107	90%	–	111%	
Vcrs	Output signal crossover voltage		1.3	–	2	V

Figure 11-50. VDAC INL vs Temperature, 1 V Mode

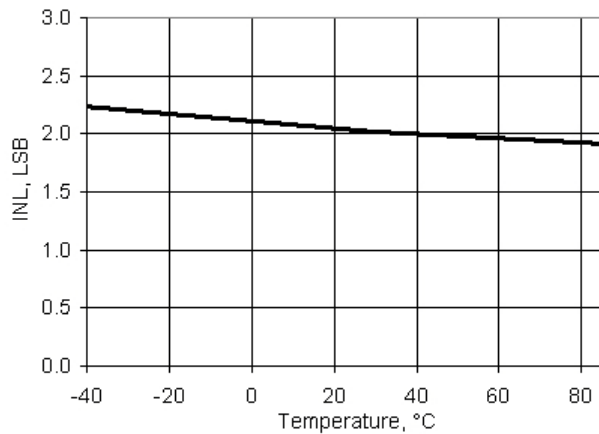


Figure 11-51. VDAC DNL vs Temperature, 1 V Mode

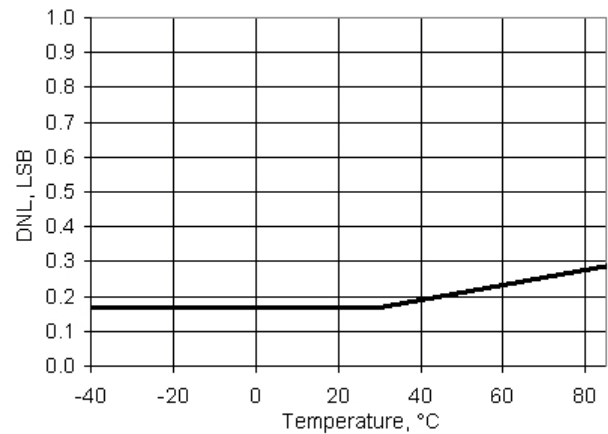


Figure 11-52. VDAC Full Scale Error vs Temperature, 1 V Mode

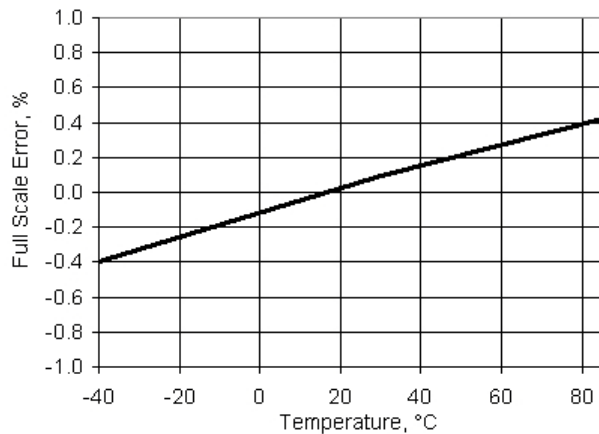


Figure 11-53. VDAC Full Scale Error vs Temperature, 4 V Mode

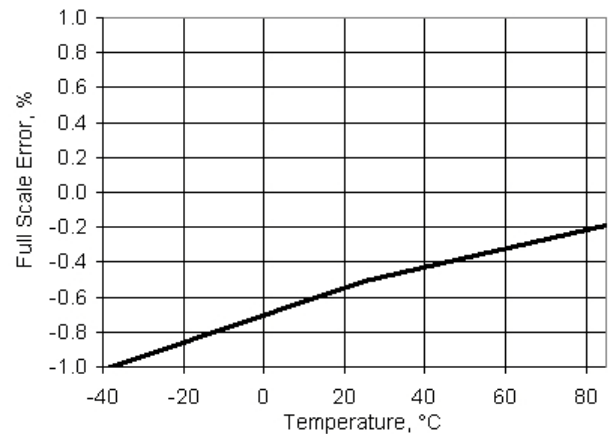


Figure 11-54. VDAC Operating Current vs Temperature, 1V Mode, Low speed mode

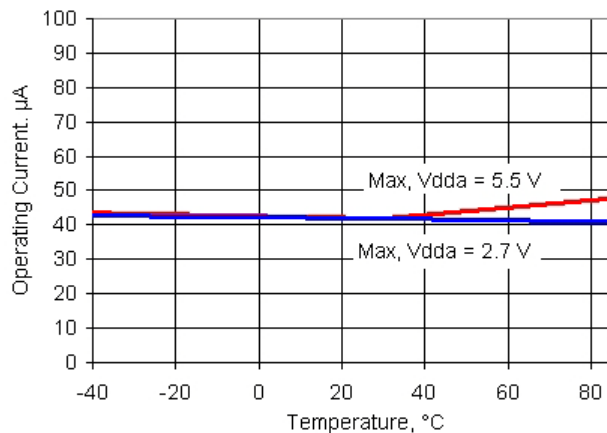
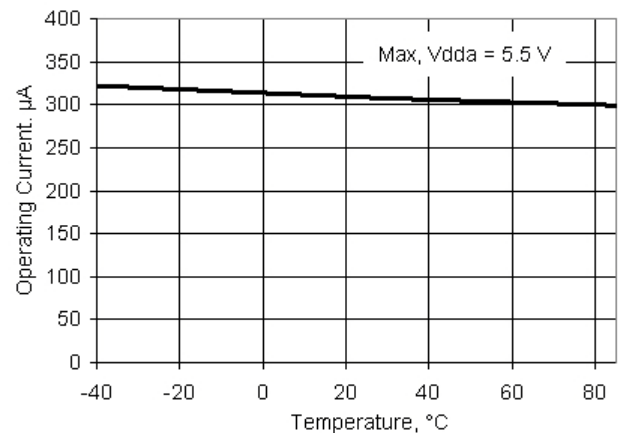


Figure 11-55. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode



Description Title: PSoC® 3: CY8C34 Family Datasheet Programmable System-on-Chip (PSoC®) (continued)
Document Number: 001-53304

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*N	3645908	06/14/2012	MKEA	<p>Added paragraph clarifying that to achieve low hibernate current, you must limit the frequency of IO input signals.</p> <p>Revised description of IPOR and clarified PRES term.</p> <p>Changed footnote to state that all GPIO input voltages - not just analog voltages - must be less than Vddio.</p> <p>Updated 100-TQFP package drawing</p> <p>Clarified description of opamp lout spec</p> <p>Changed "compliant with I2C" to "compatible with I2C"</p> <p>Updated 48-QFN package drawing</p> <p>Changed reset status register description text to clarify that not all reset sources are in the register</p> <p>Updated example PCB layout figure</p> <p>Removed text stating that FTW is a wakeup source</p> <p>Changed supply ramp rate spec from 1 V/ns to 0.066 V/μs</p> <p>Added "based on char" footnote to voltage monitors response time spec</p> <p>Changed analog global spec descriptions and values</p> <p>Added spec for ESDhbm for when Vssa and Vssd are separate</p> <p>Added a statement about support for JTAG programmers and file formats</p> <p>Changed comparator specs and conditions</p> <p>Added text describing flash cache, and updated related text</p> <p>Changed text and added figures describing Vddio source and sink</p> <p>Added a statement about support for JTAG programmers and file formats.</p> <p>Changed comparator specs and conditions</p> <p>Added text on adjustability of buzz frequency</p> <p>Updated terminology for "master" and "system" clock</p> <p>Deleted the text "debug operations are possible while the device is reset"</p> <p>Deleted and updated text regarding SIO performance under certain power ramp conditions</p> <p>Removed from boost mention of 22 μH inductors. This included deleting some graph figures.</p> <p>Changed DAC high and low speed/power mode descriptions and conditions</p> <p>Changed IMO startup time spec</p> <p>Added text on XRES and PRES re-arm times</p> <p>Added text about usage in externally regulated mode</p> <p>Updated package diagram spec 001-45616 to *D revision.</p> <p>Changed supply ramp rate spec from 1 V/ns to 0.066 V/μs</p> <p>Changed text describing SIO modes for overvoltage tolerance</p> <p>Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions</p> <p>Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions</p> <p>Changed load cap conditions in opamp specs</p> <p>Updated del-sig ADC spec tables, to replace three the instances of "16 bit" with "12 bit"</p>
*O	3648803	06/18/2012	WKA/ MKEA	No changes. EROS update.