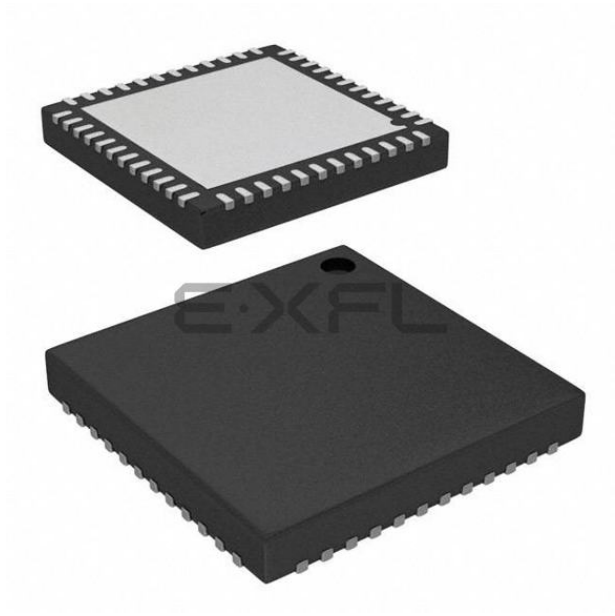

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3446lti-083t

Contents

The device provides a PLL to generate clock frequencies up to 50 MHz from the IMO, external crystal, or external reference clock. It also contains a separate, very low-power Internal low-speed oscillator (ILO) for the sleep and watchdog timers. A 32.768-kHz external watch crystal is also supported for use in RTC applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C34 family supports a wide supply operating range from 1.71 V to 5.5 V. This allows operation from regulated supplies such as 1.8 V ± 5 percent, 2.5 V ±10 percent, 3.3 V ± 10 percent, or 5.0 V ± 10 percent, or directly from a wide range of battery types. In addition, it provides an integrated high efficiency synchronous boost converter that can power the device from supply voltages as low as 0.5 V. This enables the device to be powered directly from a single battery or solar cell. In addition, you can use the boost converter to generate other voltages required by the device, such as a 3.3-V supply for LCD glass drive. The boost's output is available on the V_{BOOST} pin, allowing other devices in the application to be powered from the PSoC.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a 1-µA sleep mode with RTC. In the second mode the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

The details of the PSoC power modes are covered in the "Power System" section on page 30 of this data sheet.

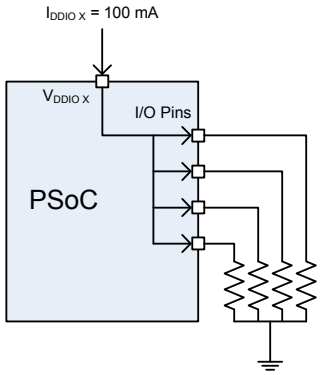
PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for 'printf' style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces enables you to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4 KB instruction and data race memory for debug. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 65 of this data sheet.

2. Pinouts

Each VDDIO pin powers a specific set of I/O pins. (The USBIOs are powered from VDDD.) Using the VDDIO pins, a single PSoC can support multiple voltage levels, reducing the need for off-chip level shifters. The black lines drawn on the pinout diagrams in Figure 2-3 through Figure 2-6, as well as Table 2-1, show the pins that are powered by each VDDIO.

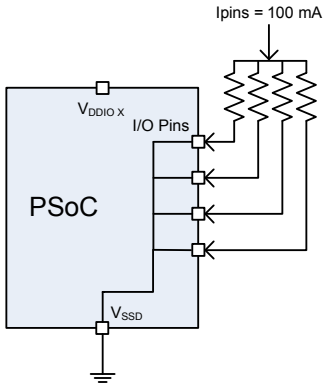
Each VDDIO may source up to 100 mA total to its associated I/O pins, as shown in Figure 2-1.

Figure 2-1. VDDIO Current Limit



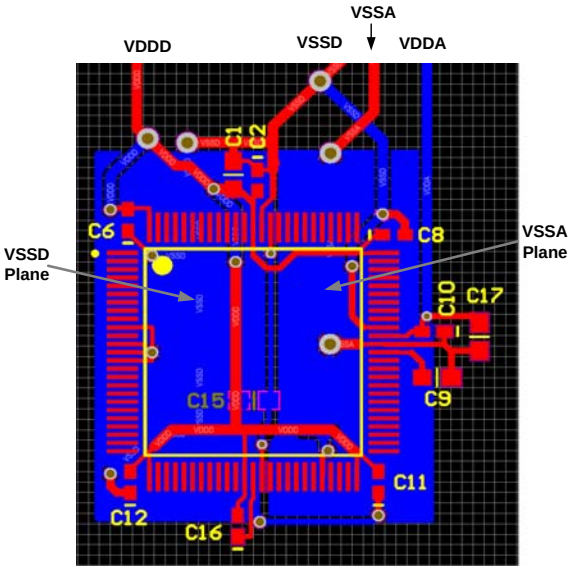
Conversely, for the 100-pin and 68-pin devices, the set of I/O pins associated with any VDDIO may sink up to 100 mA total, as shown in Figure 2-2.

Figure 2-2. I/O Pins Current Limit



For the 48-pin devices, the set of I/O pins associated with VDDIO0 plus VDDIO2 may sink up to 100 mA total. The set of I/O pins associated with VDDIO1 plus VDDIO3 may sink up to a total of 100 mA.

Figure 2-8. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC2

Low resistance output pin for high current DACs (IDAC).

OpAmp0out, OpAmp2out

High current output of uncommitted opamp[11].

Extref0, Extref1

External reference input to the analog system.

Opamp0–, Opamp2–

Inverting input to uncommitted opamp.

Opamp0+, Opamp2+

Noninverting input to uncommitted opamp.

GPIO

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[11].

I2C0: SCL, I2C1: SCL

I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA

I^2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SDA if wake from sleep is not required.

Ind

Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi

32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi

4- to 25-MHz crystal oscillator pin.

nTRST

Optional JTAG test reset programming and debug port connection to reset the JTAG connection.

SIO

Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK

Serial wire debug clock programming and debug port connection.

SWDIO

Serial wire debug input and output programming and debug port connection.

SWV

Single wire viewer debug output.

TCK

JTAG test clock programming and debug port connection.

TDI

JTAG test data In programming and debug port connection.

TDO

JTAG test data out programming and debug port connection.

TMS

JTAG test mode select programming and debug port connection.

Note
11. GPIOs with opamp outputs are not recommended for use with CapSense.

4.3 Instruction Set

The 8051 instruction set is highly optimized for 8-bit handling and Boolean operations. The types of instructions supported include:

- Arithmetic instructions
- Logical instructions
- Data transfer instructions
- Boolean instructions
- Program branching instructions

4.3.1 Instruction Set Summary

4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. Table 4-1 lists the different arithmetic instructions.

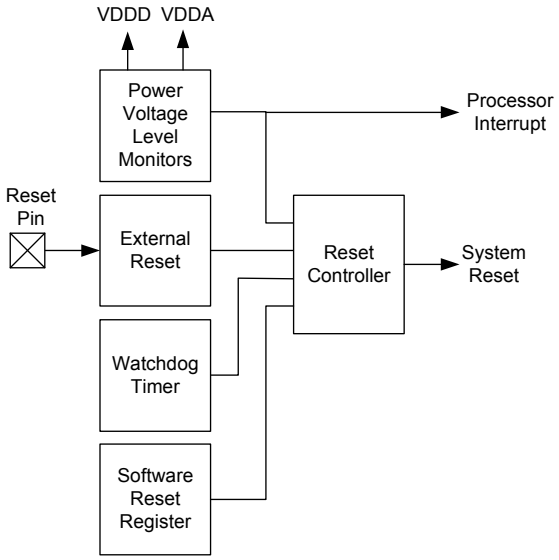
Table 4-1. Arithmetic Instructions

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A,Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A,Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3

Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	Cache/ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	I^2C	phub_termout0[15]	udb_intr[15]
16	CAN	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	LCD	phub_termout1[11]	udb_intr[27]
28	Reserved	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]
31	EEPROM Fault Int	phub_termout1[15]	udb_intr[31]

Figure 6-8. Resets



The term **device reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to detect and report certain exception conditions. This register is cleared after a power-on reset. For details see the Technical Reference Manual.

6.3.1 Reset Sources

6.3.1.1 Power Voltage Level Monitors

- IPOR – Initial Power-on Reset

  At initial power on, IPOR monitors the power voltages V_{DDD}, V_{DDA}, V_{CCD} and V_{CCA}. The trip level is not precise. It is set to approximately 1 volt, which is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 150 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

  After boot, the IPOR circuit is disabled and voltage supervision is handed off to the precise low-voltage reset (PRES) circuit.

- PRES – Precise Low Voltage Reset

  This circuit monitors the outputs of the analog and digital internal regulators after power up. The regulator outputs are compared to a precise reference voltage. The response to a PRES trip is identical to an IPOR reset.

  In normal operating mode, the program cannot disable the digital PRES circuit. The analog regulator can be disabled, which also disables the analog portion of the PRES. The PRES circuit is disabled automatically during sleep and hibernate modes, with one exception: During sleep mode the regulators are periodically activated (buzzed) to provide supervisory services and to reduce wakeup time. At these times the PRES circuit is also buzzed to allow periodic voltage monitoring.

- ALVI, DLVI, AHVI – Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

  Interrupt circuits are available to detect when VDDA and VDDD go outside a voltage range. For AHVI, VDDA is compared to a fixed trip level. For ALVI and DLVI, VDDA and VDDD are compared to trip levels that are programmable, as listed in Table 6-5. ALVI and DLVI can also be configured to generate a device reset instead of an interrupt.

Table 6-5. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings
DLVI	VDDD	1.71 V to 5.5 V	1.70 V to 5.45 V in 250 mV increments
ALVI	VDDA	1.71 V to 5.5 V	1.70 V to 5.45 V in 250 mV increments
AHVI	VDDA	1.71 V to 5.5 V	5.75 V

The monitors are disabled until after IPOR. During sleep mode these circuits are periodically activated (buzzed). If an interrupt occurs during buzzing then the system first enters its wake up sequence. The interrupt is then recognized and may be serviced.

The buzz frequency is adjustable, and should be set to be less than the minimum time that any voltage is expected to be out of range. For details on how to adjust the buzz frequency, see the TRM.

6.3.1.2 Other Reset Sources

- XRES – External Reset

  PSoC 3 has either a single GPIO pin that is configured as an external reset or a dedicated XRES pin. Either the dedicated XRES pin or the GPIO pin, if configured, holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset.

  After XRES has been deasserted, at least 10 µs must elapse before it can be reasserted.

  The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

- SRES – Software Reset

  A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

  Another register bit exists to disable this function.

- WRES – Watchdog Timer Reset

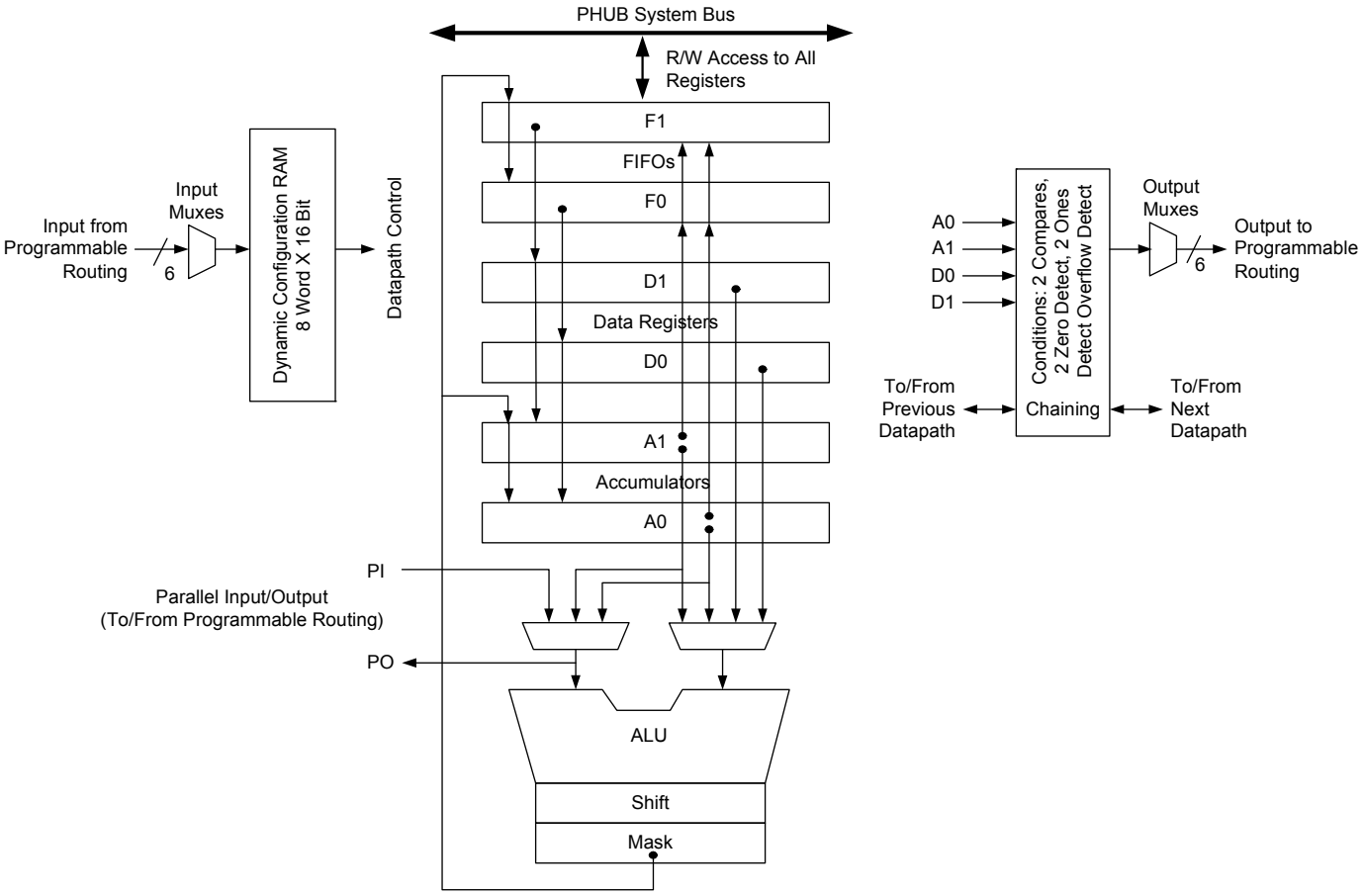
  The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

  Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power-on reset event.

7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-4. Datapath Top Level



7.2.2.1 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.2 Dynamic Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word × 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND

7.8 I²C

PSoC includes a single fixed-function I²C peripheral. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

The I²C peripheral provides a synchronous two-wire interface designed to interface the PSoC device with a two-wire I²C serial communication bus. It is compatible[16] with I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I2C-bus specification and user manual (UM10204). The I²C bus I/O may be implemented with GPIO or SIO in open-drain modes.

To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master)[17]. In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through DSI routing and allows direct connections to any GPIO or SIO pins.

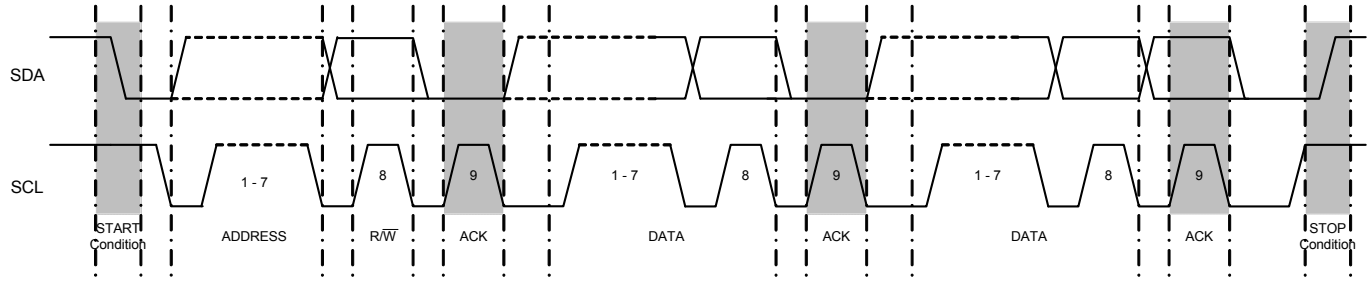
I²C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low-power modes on a 7-bit hardware address match. If wakeup functionality is required, I²C pin connections are limited to one of two specific pairs of SIO pins. See descriptions of SCL and SDA pins in Pin Descriptions on page 11.

I²C features include:

- Slave and Master, Transmitter, and Receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support – SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low-power modes on address match
- Glitch filtering (active and alternate-active modes only)

Data transfers follow the format shown in Figure 7-18. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

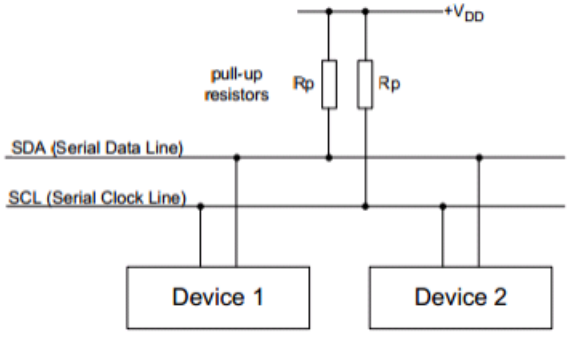
Figure 7-18. I²C Complete Transfer Timing



7.8.1 External Electrical Connections

As Figure 7-19 shows, the I²C bus requires external pull-up resistors (R_P). These resistors are primarily determined by the supply voltage, bus speed, and bus capacitance. For detailed information on how to calculate the optimum pull-up resistor value for your design, we recommend using the UM10204 I2C-bus specification and user manual Rev 6, or newer, available from the NXP website at www.nxp.com.

Figure 7-19. Connection of Devices to the I²C Bus



Notes

16. The I²C peripheral is non-compliant with the NXP I²C specification in the following areas: analog glitch filter, I/O V_{OL}/I_{OL}, I/O hysteresis. The I²C Block has a digital glitch filter (not available in sleep mode). The Fast-mode minimum fall-time specification can be met by setting the I/Os to slow speed mode. See the I/O Electrical Specifications in "Inputs and Outputs" section on page 79 for details.
17. Fixed-block I²C does not support undefined bus conditions, nor does it support Repeated Start in Slave mode. These conditions should be avoided, or the UDB-based I²C component should be used instead.

Analog local buses (abus) are routing resources located within the analog subsystem and are used to route signals between different analog blocks. There are eight abus routes in CY8C34, four in the left half (abusl [0:3]) and four in the right half (abusr [0:3]) as shown in Figure 8-2. Using the abus saves the analog globals and analog mux buses from being used for interconnecting the analog blocks.

Multiplexers and switches exist on the various buses to direct signals into and out of the analog blocks. A multiplexer can have only one connection on at a time, whereas a switch can have multiple connections on simultaneously. In Figure 8-2, multiplexers are indicated by grayed ovals and switches are indicated by transparent ovals.

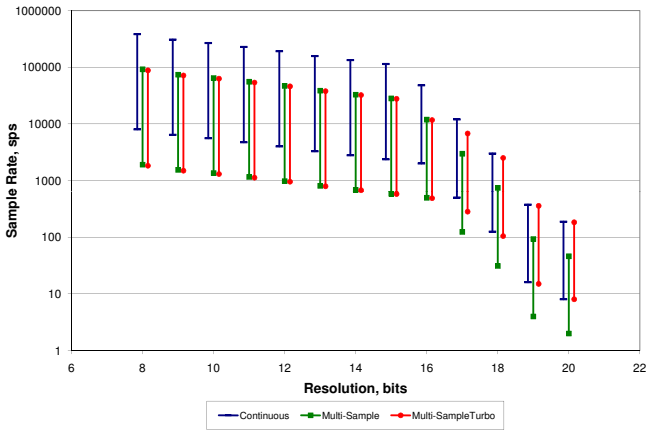
8.2 Delta-sigma ADC

The CY8C34 device contains one delta-sigma ADC. This ADC offers differential input, high resolution and excellent linearity, making it a good ADC choice for measurement applications. The converter can be configured to output 12-bit resolution at data rates of up to 192 ksps. At a fixed clock rate, resolution can be traded for faster data rates as shown in Table 8-1 and Figure 8-3.

Table 8-1. Delta-sigma ADC Performance

Bits	Maximum Sample Rate (sps)	SINAD (dB)
12	192 k	66
8	384 k	43

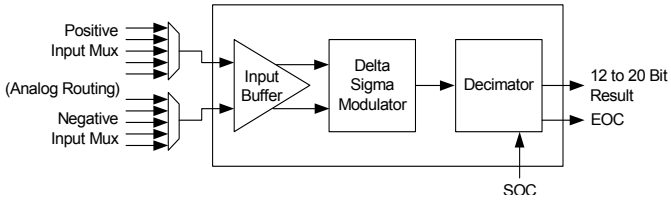
Figure 8-3. Delta-sigma ADC Sample Rates, Range = ±1.024 V



8.2.1 Functional Description

The ADC connects and configures three basic components, input buffer, delta-sigma modulator, and decimator. The basic block diagram is shown in Figure 8-4. The signal from the input muxes is delivered to the delta-sigma modulator either directly or through the input buffer. The delta-sigma modulator performs the actual analog to digital conversion. The modulator over-samples the input and generates a serial data stream output. This high speed data stream is not useful for most applications without some type of post processing, and so is passed to the decimator through the Analog Interface block. The decimator converts the high speed serial data stream into parallel ADC results. The modulator/decimator frequency response is $[(\sin x)/x]^4$.

Figure 8-4. Delta-sigma ADC Block Diagram



Resolution and sample rate are controlled by the Decimator. Data is pipelined in the decimator; the output is a function of the last four samples. When the input multiplexer is switched, the output data is not valid until after the fourth sample after the switch.

8.2.2 Operational Modes

The ADC can be configured by the user to operate in one of four modes: Single Sample, Multi Sample, Continuous, or Multi Sample (Turbo). All four modes are started by either a write to the start bit in a control register or an assertion of the Start of Conversion (SoC) signal. When the conversion is complete, a status bit is set and the output signal End of Conversion (EoC) asserts high and remains high until the value is read by either the DMA controller or the CPU.

8.2.2.1 Single Sample

In Single Sample mode, the ADC performs one sample conversion on a trigger. In this mode, the ADC stays in standby state waiting for the SoC signal to be asserted. When SoC is signaled the ADC performs four successive conversions. The first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

More information on output formats is provided in the Technical Reference Manual.

11.2 Device Level Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions		Min	Typ[25]	Max	Units
V_{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled		1.8	–	5.5	V
V_{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled		1.71	1.8	1.89	V
V_{DDD}	Digital supply voltage relative to V_{SSD}	Digital core regulator enabled		1.8	–	V_{DDA}[21]	V
				–	–	V_{DDA} + 0.1[27]	
V_{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled		1.71	1.8	1.89	V
V_{DDIO}[22]	I/O supply voltage relative to V_{SSIO}			1.71	–	V_{DDA}[21]	V
				–	–	V_{DDA} + 0.1[27]	
V_{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled		1.71	1.8	1.89	V
V_{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled		1.71	1.8	1.89	V
I_{DD} [23, 24]	**Active Mode**						
	Only IMO and CPU clock enabled. CPU executing simple loop from instruction buffer.	V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 6 MHz[26]	T = –40 °C	–	1.2	2.9	mA
			T = 25 °C	–	1.2	3.1	
			T = 85 °C	–	4.9	7.7	
	IMO enabled, bus clock and CPU clock enabled. CPU executing program from flash.	V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 3 MHz[26]	T = –40 °C	–	1.3	2.9	
			T = 25 °C	–	1.6	3.2	
			T = 85 °C	–	4.8	7.5	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 6 MHz	T = –40 °C	–	2.1	3.7	
			T = 25 °C	–	2.3	3.9	
			T = 85 °C	–	5.6	8.5	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 12 MHz[26]	T = –40 °C	–	3.5	5.2	
			T = 25 °C	–	3.8	5.5	
			T = 85 °C	–	7.1	9.8	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 24 MHz[26]	T = –40 °C	–	6.3	8.1	
			T = 25 °C	–	6.6	8.3	
			T = 85 °C	–	10	13	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 48 MHz[26]	T = –40 °C	–	11.5	13.5	
			T = 25 °C	–	12	14	
			T = 85 °C	–	15.5	18.5	

Notes

21. The power supplies can be brought up in any sequence however once stable V_{DDA} must be greater than or equal to all other supplies.
22. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
23. Total current for all power domains: digital (I_{DDD}), analog (I_{DDA}), and I/Os ($I_{DDIO0, 1, 2, 3}$). Boost not included. All I/Os floating.
24. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find the CPU current at the frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.
25. V_{DDX} = 3.3 V.
26. Based on device characterization (Not Production tested).
27. Guaranteed by design, not production tested.

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ[25]	Max	Units
	Sleep Mode[28]						
	CPU = OFF RTC = ON (= ECO32K ON, in low-power mode) Sleep timer = ON (= ILO ON at 1 kHz)[29] WDT = OFF I2C Wake = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V - 5.5 V	T = –40 °C	–	1.1	2.3	µA
			T = 25 °C	–	1.1	2.2	
			T = 85 °C	–	15	30	
		$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V	T = –40 °C	–	1	2.2	
			T = 25 °C	–	1	2.1	
			T = 85 °C	–	12	28	
		$V_{DD} = V_{DDIO}$ = 1.71 V – 1.95 V[30]	T = 25 °C	–	2.2	4.2	
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I2C Wake = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V[31]	T = 25 °C	–	2.2	2.7	
	I2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V[31]	T = 25 °C	–	2.2	2.8	
	Hibernate Mode[28]						
	Hibernate mode current All regulators and oscillators off SRAM retention GPIO interrupts are active Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V - 5.5 V	T = –40 °C	–	0.2	1.5	µA
			T = 25 °C	–	0.5	1.5	
			T = 85 °C	–	4.1	5.3	
		$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V	T = –40 °C	–	0.2	1.5	
			T = 25 °C	–	0.2	1.5	
			T = 85 °C	–	3.2	4.2	
		$V_{DD} = V_{DDIO}$ = 1.71 V – 1.95 V[30]	T = –40 °C	–	0.2	1.5	
			T = 25 °C	–	0.3	1.5	
			T = 85 °C	–	3.3	4.3	
I_{DDAR}	Analog current consumption while device is reset[32]	$V_{DDA} \leq 3.6$ V		–	0.3	0.6	mA
		$V_{DDA} > 3.6$ V		–	1.4	3.3	mA
I_{DDDR}	Digital current consumption while device is reset[32]	$V_{DDD} \leq 3.6$ V		–	1.1	3.1	mA
		$V_{DDD} > 3.6$ V		–	0.7	3.1	mA

Table 11-12. SIO AC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
Fsioout	SIO output operating frequency					
	2.7 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	1.71 V < V_{DDIO} < 2.7 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	16	MHz
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	5	MHz
	1.71 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	4	MHz
	2.7 V < V_{DDIO} < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	1.71 V < V_{DDIO} < 2.7 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	10	MHz
	1.71 V < V_{DDIO} < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ V_{DDIO} ≤ 5.5 V	90/10% V_{DDIO}	–	–	33	MHz

Figure 11-20. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

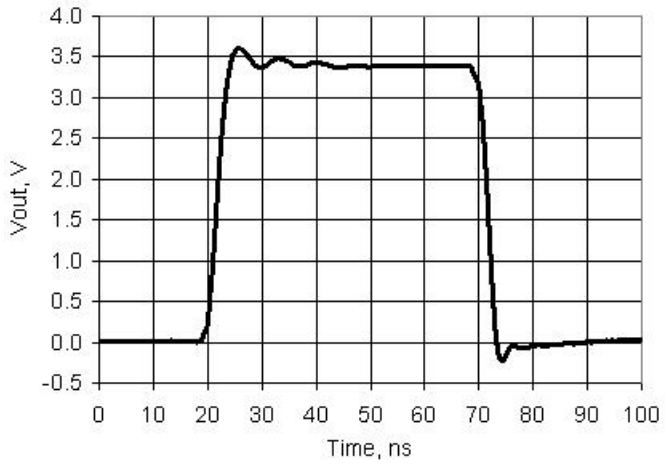
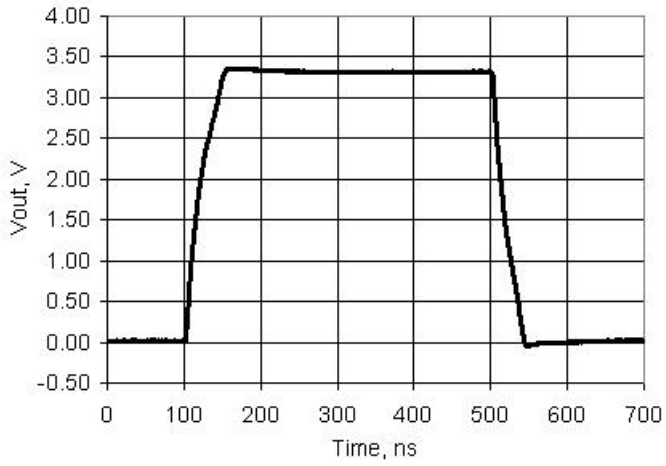


Figure 11-21. SIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load



11.4.4 XRES

Table 11-17. XRES DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold		$0.7 \times V_{DDIO}$	–	–	V
V_{IL}	Input voltage low threshold		–	–	$0.3 \times V_{DDIO}$	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
C_{IN}	Input capacitance[46]		–	3	–	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[46]		–	100	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	µA

Table 11-18. XRES AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESET}	Reset pulse width		1	–	–	µs

Note
46. Based on device characterization (Not production tested).

Figure 11-40. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode

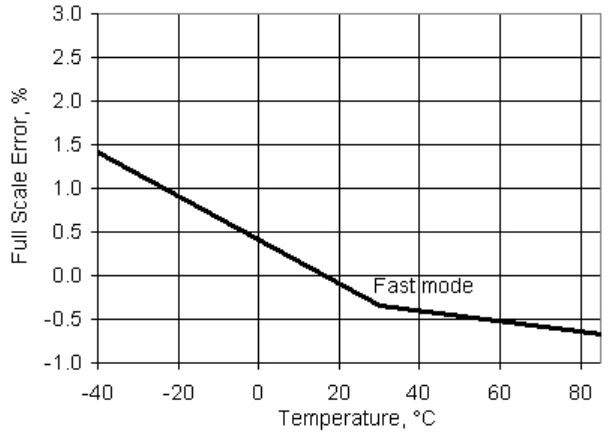


Figure 11-41. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode

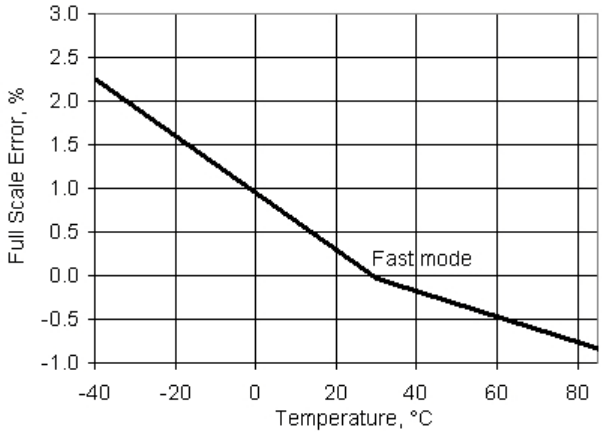


Figure 11-42. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

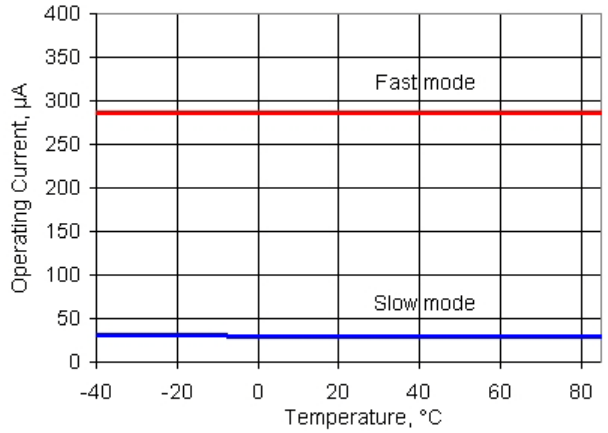


Figure 11-43. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

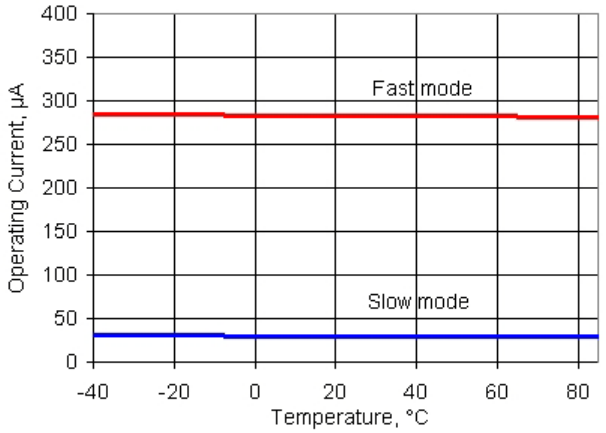
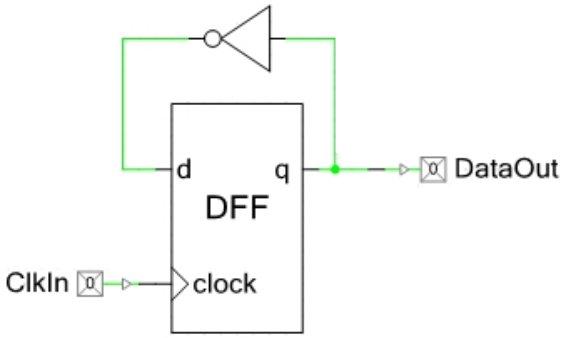


Figure 11-63. Clock to Output Performance



11.7 Memory

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-53. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	1.71	–	5.5	V

Table 11-54. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Row write time (erase + program)		–	15	20	ms
T_{ERASE}	Row erase time		–	10	13	ms
	Row program time		–	5	7	ms
T_{BULK}	Bulk erase time (16 KB to 64 KB)		–	–	35	ms
	Sector erase time (8 KB to 16 KB)		–	–	15	ms
T_{PROG}	Total device programming time	No overhead[59]	–	1.5	2	seconds
	Flash data retention time, retention period measured from last erase cycle	Average ambient temp. T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	years
		Average ambient temp. T_A ≤ 85 °C, 10 K erase/program cycles	10	–	–	years

Note
59. See PSoC® 3 Device Programming Specifications for a description of a low-overhead method of programming PSoC 3 flash.

11.8.3 Interrupt Controller

Table 11-69. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Delay from interrupt signal input to ISR code execution from ISR code	Includes worse case completion of longest instruction DIV with 6 cycles	–	–	25	Tcy CPU

11.8.4 JTAG Interface

Figure 11-68. JTAG Interface Timing

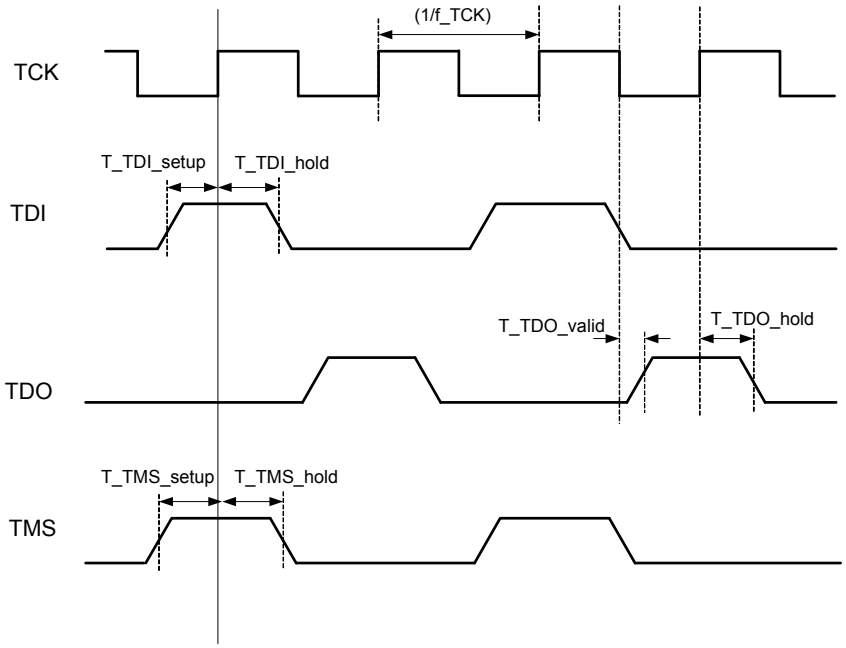


Table 11-70. JTAG Interface AC Specifications[69]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_TCK	TCK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	14[70]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[70]	MHz
T_TDI_setup	TDI setup before TCK high		(T/10) – 5	–	–	ns
T_TMS_setup	TMS setup before TCK high		T/4	–	–	
T_TDI_hold	TDI, TMS hold after TCK high	T = 1/f_TCK max	T/4	–	–	
T_TDO_valid	TCK low to TDO valid	T = 1/f_TCK max	–	–	2T/5	
T_TDO_hold	TDO hold after TCK high	T = 1/f_TCK max	T/4	–	–	

Notes
69. Based on device characterization (Not production tested).
70. f_TCK must also be no more than 1/3 CPU clock frequency.

11.9.5 External Clock Reference

Table 11-81. External Clock Reference AC Specifications[76]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at $V_{DDIO}/2$	30	50	70	%
	Input edge rate	V_{IL} to V_{IH}	0.5	–	–	V/ns

11.9.6 Phase-Locked Loop

Table 11-82. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-83. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[77]		1	–	48	MHz
	PLL intermediate frequency[78]	Output of prescaler	1	–	3	MHz
Fpllout	PLL output frequency[77]		24	–	50	MHz
	Lock time at startup		–	–	250	µs
Jperiod-rms	Jitter (rms)[76]		–	–	250	ps

Notes
76. Based on device characterization (Not production tested).
77. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
78. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C34 device includes: a precision on-chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I^2C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C34 derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C34 Family with Single Cycle 8051

Part Number	MCU Core				Analog								Digital				I/O[81]				Package	JTAG ID[82]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks[79]	Opamps	DFB	CapSense	UDBs[80]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
16 KB Flash																						
CY8C3444LTI-110	50	16	2	0.5	✔	12-bit Del-Sig	2	4	2	2	–	✔	16	4	–	–	46	38	8	0	68-pin QFN	0×1E06E069
CY8C3444LTI-119	50	16	2	0.5	✔	12-bit Del-Sig	2	4	2	2	–	✔	16	4	–	–	29	25	4	0	48-pin QFN	0×1E077069
CY8C3444PVI-100	50	16	2	0.5	✔	12-bit Del-Sig	2	4	2	2	–	✔	16	4	–	–	29	25	4	0	48-pin SSOP	0×1E064069
32 KB Flash																						
CY8C3445AXI-104	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	–	–	70	62	8	0	100-pin TQFP	0×1E068069
CY8C3445LTI-079	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	–	–	46	38	8	0	68-pin QFN	0×1E04F069
CY8C3445LTI-078	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	–	–	29	25	4	0	48-pin QFN	0×1E04E069
CY8C3445PVI-094	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	–	–	29	25	4	0	48-pin SSOP	0×1E05E069
CY8C3445AXI-108	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	✔	–	72	62	8	2	100-pin TQFP	0×1E06C069
CY8C3445LTI-081	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	✔	–	48	38	8	2	68-pin QFN	0×1E051069
CY8C3445PVI-090	50	32	4	1	✔	12-bit Del-Sig	2	4	2	2	–	✔	20	4	✔	–	31	25	4	2	48-pin SSOP	0×1E05A069
64 KB Flash																						
CY8C3446LTI-073	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	✔	–	31	25	4	2	48-pin QFN	0×1E049069
CY8C3446LTI-074	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	–	–	46	38	8	0	68-pin QFN	0×1E04A069
CY8C3446LTI-083	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	–	–	29	25	4	0	48-pin QFN	0x1E053069
CY8C3446AXI-099	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	✔	–	72	62	8	2	100-pin TQFP	0×1E063069
CY8C3446AXI-105	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	–	–	70	62	8	0	100-pin TQFP	0x1E069069
CY8C3446LTI-085	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	✔	–	48	38	8	2	68-pin QFN	0×1E055069
CY8C3446PVI-076	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	✔	–	31	25	4	2	48-pin SSOP	0×1E04C069
CY8C3446PVI-102	50	64	8	2	✔	12-bit Del-Sig	2	4	2	2	–	✔	24	4	–	✔	29	25	4	0	48-pin SSOP	0x1E066069

Notes

79. Analog blocks support a wide variety of functionality including TIA, PGA, and mixers. See the Example Peripherals on page 43 for more information on how analog blocks can be used.
80. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the Example Peripherals on page 43 for more information on how UDBs can be used.
81. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the I/O System and Routing on page 36 for details on the functionality of each of these types of I/O.
82. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise low-voltage reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

15. Reference Documents

PSoC® 3, PSoC® 5 Architecture TRM

PSoC® 3 Registers TRM

Description Title: PSoC® 3: CY8C34 Family Datasheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-53304				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*N	3645908	06/14/2012	MKEA	Added paragraph clarifying that to achieve low hibernate current, you must limit the frequency of IO input signals. Revised description of IPOR and clarified PRES term. Changed footnote to state that all GPIO input voltages - not just analog voltages - must be less than Vddio. Updated 100-TQFP package drawing Clarified description of opamp Iout spec Changed “compliant with I2C” to “compatible with I2C” Updated 48-QFN package drawing Changed reset status register description text to clarify that not all reset sources are in the register Updated example PCB layout figure Removed text stating that FTW is a wakeup source Changed supply ramp rate spec from 1 V/ns to 0.066 V/µs Added “based on char” footnote to voltage monitors response time spec Changed analog global spec descriptions and values Added spec for ESDhbm for when Vssa and Vssd are separate Added a statement about support for JTAG programmers and file formats Changed comparator specs and conditions Added text describing flash cache, and updated related text Changed text and added figures describing Vddio source and sink Added a statement about support for JTAG programmers and file formats. Changed comparator specs and conditions Added text on adjustability of buzz frequency Updated terminology for “master” and “system” clock Deleted the text “debug operations are possible while the device is reset” Deleted and updated text regarding SIO performance under certain power ramp conditions Removed from boost mention of 22 µH inductors. This included deleting some graph figures. Changed DAC high and low speed/power mode descriptions and conditions Changed IMO startup time spec Added text on XRES and PRES re-arm times Added text about usage in externally regulated mode Updated package diagram spec 001-45616 to *D revision. Changed supply ramp rate spec from 1 V/ns to 0.066 V/µs Changed text describing SIO modes for overvoltage tolerance Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions Changed load cap conditions in opamp specs Updated del-sig ADC spec tables, to replace three the instances of “16 bit” with “12 bit”
*O	3648803	06/18/2012	WKA/ MKEA	No changes. EROS update.