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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K × 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3446lti-085

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





Figure 2-3. 48-pin SSOP Part Pinout





Notes

- 5. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
- 6. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
- The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see AN72845, Design Guidelines for QFN Devices.



Figure 2-5. 68-Pin QFN Part Pinout^[9]



Notes

Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
 The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see AN72845, Design Guidelines for QFN Devices.



USBIO, D+

Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D-

Provides D– connection directly to a USB 2.0 bus. May be used as a digital I/O pin. Pins are No Connect (NC) on devices without USB.

VBOOST

Power sense connection to boost pump.

VBAT

Battery supply to boost pump.

VCCA.

Output of the analog core regulator or the input to the analog core. Requires a 1uF capacitor to VSSA. The regulator output is not designed to drive external circuits. Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V. When using the internal core regulator, (internally regulated mode, the default), do not tie any power to this pin. For details see Power System on page 30.

VCCD.

Output of the digital core regulator or the input to the digital core. The two VCCD pins must be shorted together, with the trace between them as short as possible, and a 1uF capacitor to VSSD. The regulator output is not designed to drive external circuits. Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V. When using the internal core regulator (internally regulated mode, the default), do not tie any power to this pin. For details see Power System on page 30.

VDDA

Supply for all analog peripherals and analog core regulator. VDDA must be the highest voltage present on the device. All other supply pins must be less than or equal to VDDA.

VDDD

Supply for all digital peripherals and digital core regulator. VDDD must be less than or equal to VDDA.

VSSA

Ground for all analog peripherals.

VSSB

Ground connection for boost pump.

VSSD

Ground for all digital logic and I/O pins.

VDDIO0, VDDIO1, VDDIO2, VDDIO3

Supply for I/O pins. See pinouts for specific I/O pin to VDDIO mapping. Each VDDIO must be tied to a valid operating voltage (1.71 V to 5.5 V), and must be less than or equal to VDDA.

XRES (and configurable XRES)

External reset pin. Active low with internal pull-up. Pin P1[2] may be configured to be a XRES pin; see "Nonvolatile Latches (NVLs)" on page 23.

4. CPU

4.1 8051 CPU

The CY8C34 devices use a single cycle 8051 CPU, which is fully compatible with the original MCS-51 instruction set. The CY8C34 family uses a pipelined RISC architecture, which executes most instructions in 1 to 2 cycles to provide peak performance of up to 24 MIPS with an average of 2 cycles per instruction. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor.

The 8051 CPU subsystem includes these features:

- Single cycle 8051 CPU
- Up to 64 KB of flash memory, up to 2 KB of EEPROM, and up to 8 KB of SRAM
- 512-byte instruction cache between CPU and flash
- Programmable nested vector interrupt controller
- Direct memory access (DMA) controller
- Peripheral HUB (PHUB)
- External memory interface (EMIF)

4.2 Addressing Modes

The following addressing modes are supported by the 8051:

- Direct Addressing: The operand is specified by a direct 8-bit address field. Only the internal RAM and the SFRs can be accessed using this mode.
- Indirect Addressing: The instruction specifies the register which contains the address of the operand. The registers R0 or R1 are used to specify the 8-bit address, while the data pointer (DPTR) register is used to specify the 16-bit address.
- Register Addressing: Certain instructions access one of the registers (R0 to R7) in the specified register bank. These instructions are more efficient because there is no need for an address field.
- Register Specific Instructions: Some instructions are specific to certain registers. For example, some instructions always act on the accumulator. In this case, there is no need to specify the operand.
- Immediate Constants: Some instructions carry the value of the constants directly instead of an address.
- Indexed Addressing: This type of addressing can be used only for a read of the program memory. This mode uses the Data Pointer as the base and the accumulator value as an offset to read a program memory.
- Bit Addressing: In this mode, the operand is one of 256 bits.



4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight Multi-layer AHB Bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8, 16, 24, and 32-bit addressing and data

Table 4-6. PHUB Spokes and Peripherals

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, CAN, I ² C, Timers, Counters, and PWMs
5	Reserved
6	UDBs group 1
7	UDBs group 2

4.4.2 DMA Features

- Twenty-four DMA channels
- Each channel has one or more Transaction Descriptors (TDs) to configure channel behavior. Up to 128 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel

- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64 KB
- TDs may be nested and/or chained for complex transactions

4.4.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100 percent of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in Table 4-7 after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

Table 4-7. Priority Levels

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

4.4.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:





5.5 Nonvolatile Latches (NVLs)

PSoC has a 4-byte array of nonvolatile latches (NVLs) that are used to configure the device at reset. The NVL register map is shown in Table 5-2.

 Table 5-2. Device Configuration NVL Register Map

Register Address	7	6	5	4	3	2	1	0				
0x00	PRT3RDM[1:0]		00 PRT3RDM[1:0] PRT2RDM[1:0] PRT1RDM[1:0]		PRT2RDM[1:0] PRT1RDM[1:0]		1:0] PRT2RDM[1:0]		RDM[1:0] PRT1RDM[1:0]		PRT0	RDM[1:0]
0x01	PRT12R	DM[1:0]	PRT6RDM[1:0] PRT5RDM[1:0]		PRT4	RDM[1:0]						
0x02	XRESMEN	DBGEN				PRT18	5RDM[1:0]					
0x03		DIG_PHS_I	DLY[3:0] ECCEN DPS		DLY[3:0]		[1:0]					

The details for individual fields and their factory default settings are shown in Table 5-3:.

Table 5-3. Fields and Factory Default Settings

Field	Description	Settings
PRTxRDM[1:0]	Controls reset drive mode of the corresponding IO port. See "Reset Configuration" on page 42. All pins of the port are set to the same mode.	00b (default) - high impedance analog 01b - high impedance digital 10b - resistive pull up 11b - resistive pull down
XRESMEN	Controls whether pin P1[2] is used as a GPIO or as an external reset. See "Pin Descriptions" on page 11, XRES description.	0 (default for 68-pin 72-pin, and 100-pin parts) - GPIO 1 (default for 48-pin parts) - external reset
DBGEN	Debug Enable allows access to the debug system, for third-party programmers.	0 - access disabled 1 (default) - access enabled
DPS[1:0]	Controls the usage of various P1 pins as a debug port. See "Programming, Debug Interfaces, Resources" on page 65.	00b - 5-wire JTAG 01b (default) - 4-wire JTAG 10b - SWD 11b - debug ports disabled
ECCEN	Controls whether ECC flash is used for ECC or for general configuration and data storage. See "Flash Program Memory" on page 22.	0 - ECC disabled 1 (default) - ECC enabled
DIG_PHS_DLY[3:0]	Selects the digital clock phase delay.	See the TRM for details.

Although PSoC Creator provides support for modifying the device configuration NVLs, the number of NVL erase / write cycles is limited – see "Nonvolatile Latches (NVL))" on page 109.



The USBIO pins (P15[7] and P15[6]), when enabled for I/O mode, have limited drive mode control. The drive mode is set using the PRT15.DM0[7, 6] register. A resistive pull option is also available at the USBIO pins, which can be enabled using the PRT15.DM1[7, 6] register. When enabled for USB mode, the drive mode control has no impact on the configuration of the USB pins. Unlike the GPIO and SIO configurations, the port wide configuration registers do not configure the USB drive mode bits. Table 6-7 shows the drive mode configuration for the USBIO pins.

PRT15.DM1[7,6] Pull up enable	PRT15.DM0[7,6] Drive Mode enable	PRT15.DR[7,6] = 1	PRT15.DR[7,6] = 0	Description
0	0	High Z	Strong Low	Open Drain, Strong Low
0	1	Strong High	Strong Low	Strong Outputs
1	0	Res High (5k)	Strong Low	Resistive Pull Up, Strong Low
1	1	Strong High	Strong Low	Strong Outputs

Table 6-7. USBIO Drive Modes (P15[7] and P15[6])

High impedance analog

The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

High impedance digital

The input buffer is enabled for digital signal input. This is the standard high impedance (High Z) state recommended for digital inputs.

Resistive pull-up or resistive pull-down

Resistive pull-up or pull-down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

Open drain, drives high and open drain, drives low

Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I^2C bus signal lines.

Strong drive

Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs. Resistive pull-up and pull-down

Similar to the resistive pull-up and resistive pull-down modes except the pin is always in series with a resistor. The high data state is pull-up while the low data state is pull-down. This mode is most often used when other signals that may cause shorts can drive the bus. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

6.4.3 Bidirectional Mode

High-speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRT×DM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRTxSLW registers.





Figure 7-8. Function Mapping Example in a Bank of UDBs

7.4 DSI Routing Interface Description

The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-9 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

Signals in this category include:

- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.

Figure 7-9. Digital System Interconnect Timer Interrupt DMA IO Port Global I2C CAN Counters Pins Controller Controlle Clocks Digital System Routing I/F **UDB ARRAY** Digital System Routing I/F Global IO Port SC/CT FMIF Comparators Del-Sig DACs Blocks Clocks Pins

Interrupt and DMA routing is very flexible in the CY8C34 programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-10 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

Figure 7-10. Interrupt and DMA Processing in the IDMUX

Interrupt and DMA Processing in IDMUX





Figure 7-14. CAN Bus System Implementation



7.5.1 CAN Features

- CAN2.0A/B protocol implementation ISO 11898 compliant
 Standard and extended frames with up to 8 bytes of data per frame
 - Message filter capabilities
 - Remote Transmission Request (RTR) support
- Programmable bit rate up to 1 Mbps
- Listen Only mode
- SW readable error counter and indicator
- Sleep mode: Wake the device from sleep with activity on the Rx pin
- Supports two or three wire interface to external transceiver (Tx, Rx, and Enable). The three-wire interface is compatible with the Philips PHY; the PHY is not included on-chip. The three wires can be routed to any I/O
- Enhanced interrupt controller
- CAN receive and transmit buffers status
- CAN controller error status including BusOff

- Receive path
 - **□** 16 receive buffers each with its own message filter
 - Enhanced hardware message filter implementation that covers the ID, IDE and RTR
 - DeviceNet addressing support
 - Multiple receive buffers linkable to build a larger receive message array
 - a Automatic transmission request (RTR) response handler
 - Lost received message notification
- Transmit path
 - Eight transmit buffers
 - Programmable transmit priority
 - Round robin
 - · Fixed priority
 - Message transmissions abort capability

7.5.2 Software Tools Support

CAN Controller configuration integrated into PSoC Creator:

- CAN Configuration walkthrough with bit timing analyzer
- Receive filter setup



For most designs, the default values in Table 7-2 will provide excellent performance without any calculations. The default values were chosen to use standard resistor values between the minimum and maximum limits. The values in Table 7-2 work for designs with 1.8 V to 5.0V V_{DD}, less than 200-pF bus capacitance (C_B), up to 25 μ A of total input leakage (I_{IL}), up to 0.4 V output voltage level (V_{OL}), and a max V_{IH} of 0.7 * V_{DD}. Standard Mode and Fast Mode can use either GPIO or SIO PSoC pins. Fast Mode Plus requires use of SIO pins to meet the V_{OL} spec at 20 mA. Calculation of custom pull-up resistor values is required; if your design does not meet the default assumptions, you use series resistors (RS) to limit injected noise, or you need to maximize the resistor value for low power consumption.

Table 7-2.	Recommended	default	Pull-up	Resistor	Values
------------	-------------	---------	---------	----------	--------

	R _P	Units
Standard Mode – 100 kbps	4.7 k, 5%	Ω
Fast Mode – 400 kbps	1.74 k, 1%	Ω
Fast Mode Plus – 1 Mbps	620, 5%	Ω

Calculation of the ideal pull-up resistor value involves finding a value between the limits set by three equations detailed in the NXP I^2C specification. These equations are:

Equation 1:

$$R_{PMIN} = (V_{DD}(max) - V_{OL}(max))/(I_{OL}(min))$$

Equation 2:

$$R_{PMAX} = T_R(max)/0.8473 \times C_R(max)$$

Equation 3:

$$R_{PMAX} = V_{DD}(min) - V_{IH}(min) + V_{NH}(min) / I_{IH}(max)$$

Equation parameters:

 V_{DD} = Nominal supply voltage for I²C bus

V_{OL} = Maximum output low voltage of bus devices.

 I_{OL} = Low-level output current from I²C specification

 T_R = Rise Time of bus from I²C specification

C_B = Capacitance of each bus line including pins and PCB traces

V_{IH} = Minimum high-level input voltage of all bus devices

 V_{NH} = Minimum high-level input noise margin from I^2C specification

 I_{IH} = Total input leakage current of all devices on the bus

The supply voltage (V_{DD}) limits the minimum pull-up resistor value due to bus devices maximum low output voltage (V_{OL}) specifications. Lower pull-up resistance increases current through the pins and can, therefore, exceed the spec conditions of V_{OL}. Equation 1 is derived using Ohm's law to determine the minimum resistance that will still meet the V_{OL} specification at 3 mA for standard and fast modes, and 20 mA for fast mode plus at the given V_{DD}.

Equation 2 determines the maximum pull-up resistance due to bus capacitance. Total bus capacitance is comprised of all pin, wire, and trace capacitance on the bus. The higher the bus capacitance, the lower the pull-up resistance required to meet the specified bus speeds rise time due to RC delays. Choosing a pull-up resistance higher than allowed can result in failing timing requirements resulting in communication errors. Most designs with five or less I^2C devices and up to 20 centimeters of bus trace length have less than 100 pF of bus capacitance.

A secondary effect that limits the maximum pull-up resistor value is total bus leakage calculated in Equation 3. The primary source of leakage is I/O pins connected to the bus. If leakage is too high, the pull-ups will have difficulty maintaining an acceptable V_{IH} level causing communication errors. Most designs with five or less I^2C devices on the bus have less than 10 μA of total leakage current.



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C34 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane × 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization



8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers via DMA.

8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.



11.2 Device Level Specifications

Specifications are valid for -40 $^{\circ}C \le T_A \le 85 ^{\circ}C$ and $T_J \le 100 ^{\circ}C$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions			Typ ^[25]	Max	Units
V _{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulat	or enabled	1.8	-	5.5	V
V _{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled		1.71	1.8	1.89	V
Vaaa	Digital supply voltage relative to Vaca	Digital core regulato	or enabled	1.8	_	V _{DDA} ^[21]	V
•000				-	-	V _{DDA} + 0.1 ^[27]	v
V _{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulate	or disabled	1.71	1.8	1.89	V
Vpp10 ^[22]	I/O supply voltage relative to Vacua			1.71	-	V _{DDA} ^[21]	V
				-	-	V _{DDA} + 0.1 ^[27]	
V _{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulat	or disabled	1.71	1.8	1.89	V
V _{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled		1.71	1.8	1.89	V
	Active Mode						
	Only IMO and CPU clock enabled. CPU executing simple loop from instruction buffer.	V _{DDX} = 2.7 V – 5.5 V; F _{CPU} = 6 MHz ^[26]	T = -40 °C	-	1.2	2.9	-
			T = 25 °C	_	1.2	3.1	
			T = 85 °C	-	4.9	7.7	
		V _{DDX} = 2.7 V – 5.5 V; F _{CPU} = 3 MHz ^[26]	T = -40 °C	-	1.3	2.9	
			T = 25 °C	-	1.6	3.2	
			T = 85 °C	-	4.8	7.5	
		$V_{DDX} = 2.7 V - 5.5 V$	T = -40 °C	-	2.1	3.7	
100 o 41		5.5 V, F _{CPU} = 6 MHz	T = 25 °C	-	2.3	3.9	
I _{DD} ^[23, 24]			T = 85 °C	-	5.6	8.5	mA
	IMO enabled, bus clock and CPU clock	$V_{DDX} = 2.7 V - $	T = -40 °C	-	3.5	5.2	
	enabled. CPU executing program from	5.5 V; $F_{CDU} = 12 \text{ MHz}^{[26]}$	T = 25 °C	-	3.8	5.5	
	nasn.		T = 85 °C	-	7.1	9.8	
		V _{DDX} = 2.7 V –	T = -40 °C	-	6.3	8.1	
		5.5 V; Eopu = 24 MHz ^[26]	T = 25 °C	-	6.6	8.3	
			T = 85 °C	-	10	13	
		$V_{DDX} = 2.7 V -$	T = -40 °C	_	11.5	13.5	
		5.5 V; Foru = 48 MHz ^[26]	T = 25 °C	-	12	14	
		$T = 85^{\circ}$		-	15.5	18.5	

Notes

 21. The power supplies can be brought up in any sequence however once stable V_{DDA} must be greater than or equal to all other supplies.
 22. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
 23. Total current for all power domains: digital (I_{DDD}), analog (I_{DDA}), and I/Os (I_{DDIO0,1,2,3}). Boost not included. All I/Os floating.
 24. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find the CPU current at the frequency of interest and add peripheral currents for your next integrated design environment. particular system from the device datasheet and component datasheets. 25. $V_{DDX} = 3.3 V$.

26. Based on device characterization (Not Production tested).

27. Guaranteed by design, not production tested.



11.4 Inputs and Outputs

Specifications are valid for –40 °C \leq T_A \leq 85 °C and T_J \leq 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

When the power supplies ramp up, there are low-impedance connections between each GPIO pin and its V_{DDIO} supply. This causes the pin voltages to track V_{DDIO} until both V_{DDIO} and V_{DDA} reach the IPOR voltage, which can be as high as 1.45 V. At that point, the low-impedance connections no longer exist and the pins change to their normal NVL settings.

11.4.1 GPIO

Table 11-9. GPIO DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
V _{IH}	Input voltage high threshold	CMOS Input, PRT[×]CTL = 0	$0.7 \times V_{DDIO}$	-	-	V
V _{IL}	Input voltage low threshold	CMOS Input, PRT[×]CTL = 0	_	-	$0.3 \times V_{DDIO}$	V
V _{IH}	Input voltage high threshold	LVTTL Input, PRT[×]CTL = 1,V _{DDIO} < 2.7 V	$0.7 \times V_{DDIO}$	_	-	V
V _{IH}	Input voltage high threshold	LVTTL Input, PRT[×]CTL = 1, $V_{DDIO} \ge 2.7V$	2.0	-	-	V
V _{IL}	Input voltage low threshold	LVTTL Input, PRT[×]CTL = 1,V _{DDIO} < 2.7 V	_	-	$0.3 \times V_{DDIO}$	V
V _{IL}	Input voltage low threshold	LVTTL Input, PRT[×]CTL = 1, $V_{DDIO} \ge 2.7V$	_	_	0.8	V
V _{OH}	Output voltage high	I _{OH} = 4 mA at 3.3 V _{DDIO}	$V_{DDIO} - 0.6$	-	-	V
		I _{OH} = 1 mA at 1.8 V _{DDIO}	$V_{DDIO} - 0.5$	-	-	V
V _{OL}	Output voltage low	I _{OL} = 8 mA at 3.3 V _{DDIO}	_	_	0.6	V
		I _{OL} = 4 mA at 1.8 V _{DDIO}	_	-	0.6	V
		I _{OL} = 3 mA at 3.3 V _{DDIO}	-	-	0.4	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull-down resistor		3.5	5.6	8.5	kΩ
IIL	Input leakage current (absolute value) ^[39]	25 °C, V _{DDIO} = 3.0 V	-	-	2	nA
C _{IN}	Input capacitance ^[39]	GPIOs not shared with opamp outputs, MHz ECO or kHzECO	-	4	7	pF
		GPIOs shared with MHz ECO or kHzECO ^[40]	-	5	7	pF
		GPIOs shared with opamp outputs	-	-	18	pF
V _H	Input voltage hysteresis (Schmitt-Trigger) ^[39]		-	40	-	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		-	_	100	μA
Rglobal	Resistance pin to analog global bus	25 °C, V _{DDIO} = 3.0 V	-	320	_	Ω
Rmux	Resistance pin to analog mux bus	25 °C, V _{DDIO} = 3.0 V	_	220	_	Ω

Notes

39. Based on device characterization (Not production tested).

40. For information on designing with PSoC oscillators, refer to the application note, AN54439 - PSoC® 3 and PSoC 5 External Oscillator.



Figure 11-22. USBIO Output High Voltage and Current, GPIO Mode







Table 11-15. USBIO AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
Tdrate	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		-8	_	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		-5	_	5	ns
Tdj1	Driver differential jitter to next transition		-3.5	-	3.5	ns
Tdj2	Driver differential jitter to pair transition		-4	-	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		-2	-	5	ns
Tfeopt	Source SE0 interval of EOP		160	-	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	-	-	ns
Tfst	Width of SE0 interval during differential transition		-	-	14	ns
Fgpio_out	GPIO mode output operating	$3 \text{ V} \leq \text{V}_{DDD} \leq 5.5 \text{ V}$	-	-	20	MHz
	frequency	V _{DDD} = 1.71 V	-	-	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% V _{DDD}	V _{DDD} > 3 V, 25 pF load	-	-	12	ns
		V _{DDD} = 1.71 V, 25 pF load	-	-	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V _{DDD}	V _{DDD} > 3 V, 25 pF load	_	-	12	ns
		V _{DDD} = 1.71 V, 25 pF load	-	-	40	ns



Table 11-37. PGA AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
BW1	–3 dB bandwidth	Power mode = high, gain = 1, input = 100 mV peak-to-peak	6.7	8	-	MHz
SR1	Slew rate	Power mode = high, gain = 1, 20% to 80%	3	-	-	V/µs
e _n	Input noise density	Power mode = high, V _{DDA} = 5 V, at 100 kHz	_	43	_	nV/sqrtHz

Figure 11-61. Bandwidth vs. Temperature, at Different Gain Settings, Power Mode = High



Figure 11-62. Noise vs. Frequency, $V_{DDA} = 5 V$, Power Mode = High



11.5.11 Temperature Sensor

Table 11-38. Temperature Sensor Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
	Temp sensor accuracy	Range: –40 °C to +85 °C	_	±5	-	°C

11.5.12 LCD Direct Drive

Table 11-39. LCD Direct Drive DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
I _{CC}	LCD system operating current	Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 Mhz, $V_{DDIO} = V_{DDA} = 3 V$, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	_	38	-	μΑ
I _{CC_SEG}	Current per segment driver	Strong drive mode	-	260	-	μA
V _{BIAS}	LCD bias range (V _{BIAS} refers to the main output voltage(V0) of LCD DAC)	$V_{DDA} \ge 3 \text{ V} \text{ and } V_{DDA} \ge V_{BIAS}$	2	-	5	V
	LCD bias step size	$V_{DDA} \ge 3 V$ and $V_{DDA} \ge V_{BIAS}$	-	9.1 × V _{DDA}	-	mV
	LCD capacitance per segment/common driver	Drivers may be combined	_	500	5000	pF
	Long term segment offset		-	_	20	mV
I _{OUT}	Output drive current per segment driver)	V_{DDIO} = 5.5 V, strong drive mode	355	-	710	μA

Table 11-40. LCD Direct Drive AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
f _{LCD}	LCD frame rate		10	50	150	Hz



Figure 11-63. Clock to Output Performance



11.7 Memory

Specifications are valid for –40 °C \leq T_A \leq 85 °C and T_J \leq 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-53. Flash DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
	Erase and program voltage	V _{DDD} pin	1.71	1	5.5	V

Table 11-54. Flash AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
T _{WRITE}	Row write time (erase + program)		-	15	20	ms
T _{ERASE}	Row erase time		-	10	13	ms
	Row program time		-	5	7	ms
T _{BULK}	Bulk erase time (16 KB to 64 KB)		-	-	35	ms
	Sector erase time (8 KB to 16 KB)		-	-	15	ms
T _{PROG}	Total device programming time	No overhead ^[59]	-	1.5	2	seconds
	Flash data retention time, retention period measured from last erase cycle	Average ambient temp. T _A \leq 55 °C, 100 K erase/program cycles	20	-	_	years
		Average ambient temp. $T_A \le 85$ °C, 10 K erase/program cycles	10	_	_	years







Table 11-64. Synchronous Write Cycle Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
Т	EMIF clock Period ^[67]	$V_{DDA} \ge 3.3 V$	30.3	-	-	ns
Tcp/2	EM_Clock pulse high		T/2	-	-	ns
Tceld	EM_CEn low to EM_Clock high		5	-	-	ns
Tcehd	EM_Clock high to EM_CEn high		T/2 – 5	-	-	ns
Taddrv	EM_Addr valid to EM_Clock high		5	-	-	ns
Taddriv	EM_Clock high to EM_Addr invalid		T/2 – 5	-	-	ns
Tweld	EM_WEn low to EM_Clock high		5	-	-	ns
Twehd	EM_Clock high to EM_WEn high		T/2 – 5	-	-	ns
Tds	Data valid before EM_Clock high		5	-	-	ns
Tdh	Data invalid after EM_Clock high		Т	-	-	ns
Tadscld	EM_ADSCn low to EM_Clock high		5	-	-	ns
Tadschd	EM_Clock high to EM_ADSCn high		T/2 – 5	_	-	ns



□ 6: 64 KB

12.1 Part Numbering Conventions

PSoC 3 devices follow the part numbering convention described here. All fields are single character alphanumeric (0, 1, 2, ..., 9, A, B, ..., Z) unless stated otherwise.

CY8Cabcdefg-xxx	
 a: Architecture 3: PSoC 3 5: PSoC 5 b: Family group within architecture 4: CY8C34 family 6: CY8C36 family 8: CY8C38 family c: Speed grade 4: 50 MHz 	 ■ ef: Package code □ Two character alphanumeric □ AX: TQFP
	□ LT: QFN □ PV: SSOP
	 ■ g: Temperature range □ C: commercial
	□ I: industrial □ A: automotive
□ 6: 67 MHz	■ xxx: Peripheral set
 ■ d: Flash capacity □ 4: 16 KB □ 5: 32 KB 	 Three character numeric No meaning is associated with these three characters.

Example	$\begin{array}{c c} CY8C & 3 & 4 & 4 & 6 \\ \hline CY8C & 3 & 4 & 4 & 6 \\ \hline \end{array} \begin{array}{c} P & V & I \\ \hline \end{array} \begin{array}{c} - x & x \\ \hline \end{array}$	x
	Cypress Prefix	
3: PSoC 3	Architecture	
4: CY8C34 Family	Family Group within Architecture	
4: 50 MHz	Speed Grade	
6: 64 KB	Flash Capacity	
PV: SSOP	Package Code	
I: Industrial	Temperature Range ————————————————————————————————————	
	Peripheral Set	

Tape and reel versions of these devices are available and are marked with a "T" at the end of the part number.

All devices in the PSoC 3 CY8C34 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration data sheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other "end of life" requirements.



13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Тур	Max	Units
T _A	Operating ambient temperature		-40	25.00	85	°C
TJ	Operating junction temperature		-40	-	100	°C
T _{JA}	Package θ_{JA} (48-pin SSOP)		-	49	-	°C/Watt
T _{JA}	Package θ_{JA} (48-pin QFN)		-	14	-	°C/Watt
T _{JA}	Package θ_{JA} (68-pin QFN)		-	15	-	°C/Watt
T _{JA}	Package θ_{JA} (100-pin TQFP)		-	34	-	°C/Watt
T _{JC}	Package θ_{JC} (48-pin SSOP)		-	24	-	°C/Watt
T _{JC}	Package θ_{JC} (48-pin QFN)		-	15	-	°C/Watt
T _{JC}	Package θ_{JC} (68-pin QFN)		-	13	-	°C/Watt
T _{JC}	Package θ_{JC} (100-pin TQFP)		-	10	_	°C/Watt

Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
48-pin SSOP	MSL 3
48-pin QFN	MSL 3
68-pin QFN	MSL 3
100-pin TQFP	MSL 3



Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise low-voltage reset
PRS	pseudo random sequence
PS	port read data register
PSoC [®]	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

15. Reference Documents

PSoC® 3, PSoC® 5 Architecture TRM PSoC® 3 Registers TRM



16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
μA	microamperes
μF	microfarads
μH	microhenrys
μs	microseconds
μV	microvolts
μW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
S	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts