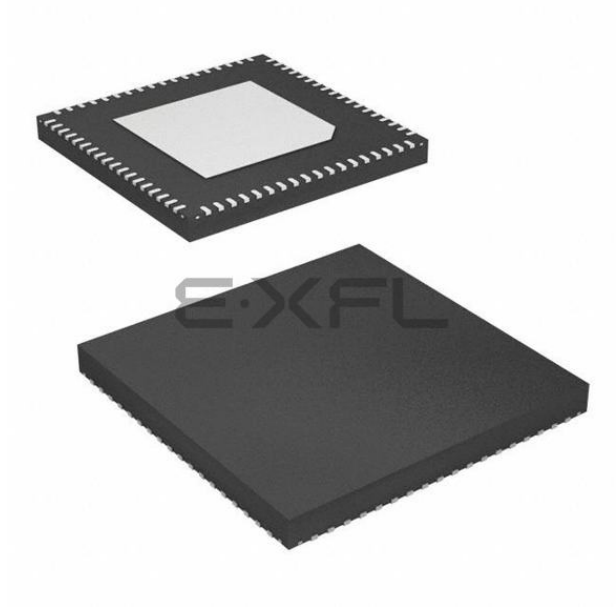

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	147.456MHz
Non-Volatile Memory	ROM (32kB)
On-Chip RAM	32kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	72-VFQFN Exposed Pad, CSP
Supplier Device Package	72-LFCSP-VQ (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1450wbcpz

Auxiliary ADC

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, AVDD = 3.3 V ± 10%, IOVDD = 1.8 V − 10% to 3.3 V + 10%, unless otherwise noted.

Table 5.

Parameter	Min	Typ	Max	Unit
RESOLUTION		10		Bits
FULL-SCALE ANALOG INPUT		AVDD		V
NONLINEARITY				
Integrated Nonlinearity (INL)	−2		+2	LSB
Differential Nonlinearity (DNL)	−2		+2	LSB
GAIN ERROR	−2		+2	LSB
INPUT IMPEDANCE		200		kΩ
SAMPLE RATE		f_{CORE}/6144		Hz

TIMING SPECIFICATIONS

Master Clock Input

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 10% to 3.3 V + 10%, unless otherwise noted.

Table 6.

Parameter	Min	Max	Unit	Description
MASTER CLOCK INPUT (MCLK)				
f_{MCLK}	2.375	36	MHz	MCLK frequency
t_{MCLK}	27.8	421	ns	MCLK period
t_{MCLKD}	25	75	%	MCLK duty cycle
t_{MCLKH}	0.25 × t_{MCLK}	0.75 × t_{MCLK}	ns	MCLK width high
t_{MCLKL}	0.25 × t_{MCLK}	0.75 × t_{MCLK}	ns	MCLK width low
CLKOUT Jitter	12	106	ps	Cycle-to-cycle rms average
CORE CLOCK				
f_{CORE}				
ADAU1452 and ADAU1451	152	294.912	MHz	System (DSP core) clock frequency; PLL feedback divider ranges from 64 to 108
ADAU1450	76	147.456	MHz	System (DSP core) clock frequency; PLL feedback divider ranges from 64 to 108
t_{CORE}				
ADAU1452 and ADAU1451	3.39		ns	System (DSP core) clock period
ADAU1450	6.78		ns	System (DSP core) clock period

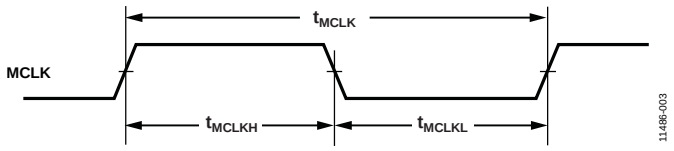

Figure 3. Master Clock Input Timing Specifications

Reset

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 10% to 3.3 V + 10%.

Table 7.

Parameter	Min	Max	Unit	Description
$\overline{\text{RESET}}$				
t_{WRST}	10		ns	Reset pulse width low

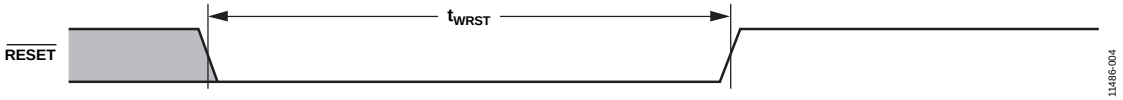

Figure 4. Reset Timing Specification

I²C Interface—Master

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 10% to 3.3 V + 10%.

Table 13.

Parameter	Min	Max	Unit	Description
I²C MASTER PORT				
f_{SCL}		400	kHz	SCL clock frequency
t_{SCLH}	0.6		µs	SCL pulse width high
t_{SCLL}	1.3		µs	SCL pulse width low
t_{SCS}	0.6		µs	Start and repeated start condition setup time
t_{SCH}	0.6		µs	Start condition hold time
t_{DS}	100		ns	Data setup time
t_{DH}	0.9		µs	Data hold time
t_{SCLR}		300	ns	SCL rise time
t_{SCLF}		300	ns	SCL fall time
t_{SDR}		300	ns	SDA rise time
t_{SDF}		300	ns	SDA fall time
t_{BFT}	1.3		µs	Bus-free time between stop and start
t_{SUSTO}	0.6		µs	Stop condition setup time

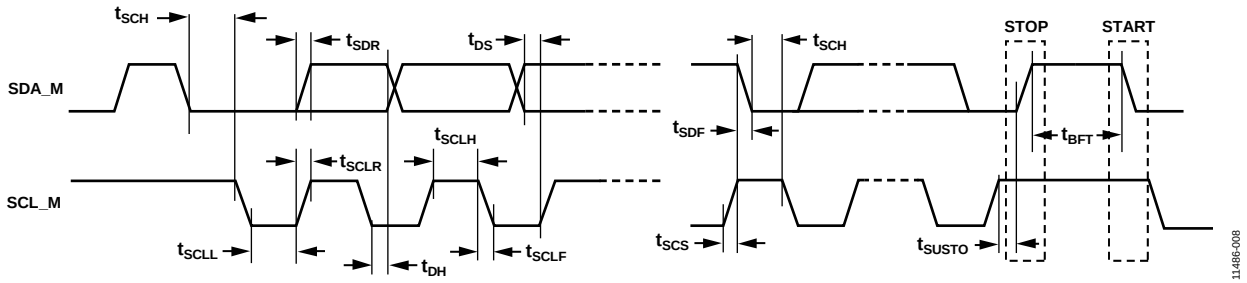

Figure 8. I²C Master Port Timing Specifications

INITIALIZATION

Power-Up Sequence

The first step in the initialization sequence is to power up the device. First, apply voltage to the power pins. All power pins can be supplied simultaneously. If the power pins are not supplied simultaneously, then supply IOVDD first because the internal ESD protection diodes are referenced to the IOVDD voltage. AVDD, DVDD, and PVDD can be supplied at the same time as IOVDD or after, but they must not be supplied prior to IOVDD. The order in which AVDD, DVDD, and PVDD are supplied does not matter.

When the internal regulator is not used and DVDD is directly supplied, no special sequence is required when providing the proper voltages to AVDD, DVDD, and PVDD.

When the internal regulator is used, DVDD is generated by the regulator, in combination with an external pass transistor, after AVDD, IOVDD, and PVDD are supplied. See the Power Supplies section for more information.

Each power supply domain has its own power-on reset (POR) circuits (also known as power OK circuits) to ensure that the level shifters attached to each power domain can be initialized properly. AVDD and PVDD must reach their nominal level before the auxiliary ADC and PLL can be used, respectively.

However, the AVDD and PVDD supplies have no role in the rest of the power-up sequence. After AVDD power reaches its nominal threshold, the regulator becomes active and begins to charge up the DVDD supply. The DVDD also has a POR circuit to ensure that the level shifters initialize during power-up.

The POR signals are combined into three global level shifter resets that properly initialize the signal crossings between each separate power domain and DVDD.

The digital circuits remain in reset until the IOVDD to DVDD level shifter reset is released. At that point, the digital circuits exit reset.

When a crystal is in use, the crystal oscillator circuit must provide a stable master clock to the XTALIN/MCLK pin by the time the PVDD supply reaches its nominal level. The XTALIN/MCLK pin is restricted from passing into the PLL circuitry until the DVDD POR signal becomes active and the PVDD to DVDD level shifter is initialized.

When all four POR circuits signal that the power-on conditions are met, a reset synchronizer circuit releases the internal digital circuitry from reset, provided the following conditions are met:

- A valid MCLK signal is provided to the digital circuitry and the PLL.
- The $\overline{\text{RESET}}$ pin is high.

When the internal digital circuitry becomes active, the DSP core runs eight lines of initialization code stored in ROM, requiring eight cycles of the MCLK signal. For a 12.288 MHz MCLK input, this process takes 650 ns.

After the ROM program completes its execution, the PLL is ready to be configured using register writes to Register 0xF000 (PLL_CTRL0), Register 0xF001 (PLL_CTRL1), Register 0xF002 (PLL_CLK_SRC), and Register 0xF003 (PLL_ENABLE).

When the PLL is configured and enabled, the PLL starts to lock to the incoming master clock signal. The absolute maximum PLL lock time is 32 × 1024 = 32,768 clock cycles on the clock signal (after the input prescaler), which is fed to the input of the PLL. In a standard 48 kHz use case, the PLL input clock frequency after the prescaler is 3.072 MHz; therefore, the maximum PLL lock time is 10.666 ms.

Typically, the PLL locks much faster than 10.666 ms. In most systems, the PLL locks within about 3.5 ms. The PLL_LOCK register (Address 0xF004) can be polled via the control port until Bit 0 (PLL_LOCK) goes high, signifying that the PLL lock has completed successfully.

While the PLL is attempting to lock to the input clock, the I^2C slave and SPI slave control ports are inactive; therefore, no other registers are accessible over the control port. While the PLL is attempting to lock, all attempts to write to the control port fail.

Clock Generators

Three clock generators are available to generate audio clocks for the serial ports, DSP, ASRCs, and other audio related functional blocks in the system. Each clock generator can be configured to generate a base frequency and several fractions or multiples of that base frequency, creating a total of 15 clock domains available for use in the system. Each of the 15 clock domains can create the appropriate LRCLK (frame clock) and BCLK (bit clock) signals for the serial ports. Five BCLK signals are generated at frequencies of 32 BCLK/sample, 64 BCLK/sample, 128 BCLK/sample, 256 BCLK/sample, and 512 BCLK/sample to deal with TDM data. Thus, with a single master clock input frequency, 15 different frame clock frequencies and 75 different bit clock frequencies can be generated for use in the system.

The nominal output of each clock generator is determined by the following formula:

$$Output\_Frequency = (Input\_Frequency \times N)/(1024 \times M)$$

where:
Input_Frequency is the PLL output (nominally 294.912 MHz).
Output_Frequency is the frame clock output frequency.
N and *M* are integers that are configured by writing to the clock generator configuration registers.

These calculations are also accurate in the case of the ADAU1450, even though the output rate of its PLL is half of that of the ADAU1452/ADAU1451.

In addition to the nominal output, four additional output signals are generated at double, quadruple, half, and a quarter of the frequency of the nominal output frequency.

For Clock Generator 1 and Clock Generator 2, the integer numerator (N) and the integer denominator (M) are each nine bits long. For Clock Generator 3, N and M are each 16 bits long, allowing for a higher precision when generating arbitrary clock frequencies.

Figure 18 shows a basic block diagram of the PLL and clock generators. Each division operator symbolizes that the frequency of the clock is divided when passing through that block. Each multiplication operator symbolizes that the frequency of the clock is multiplied when passing through that block.

Figure 19 shows an example where the master clock input has a frequency of 12.288 MHz, and the default settings are used for the PLL predivider, feedback divider, and Clock Generator 1 and Clock Generator 2. The resulting system clock is

12.288 MHz ÷ 4 × 96 = 294.912 MHz

The base output of Clock Generator 1 is

294.912 MHz ÷ 1024 × 1 ÷ 6 = 48 kHz

The base output of Clock Generator 2 is

294.912 MHz ÷ 1024 × 1 ÷ 9 = 32 kHz

In this example, Clock Generator 3 is configured with N = 49 and M = 320; therefore, the resulting base output of Clock Generator 3 is

294.912 MHz ÷ 1024 × 49 ÷ 320 = 44.1 kHz

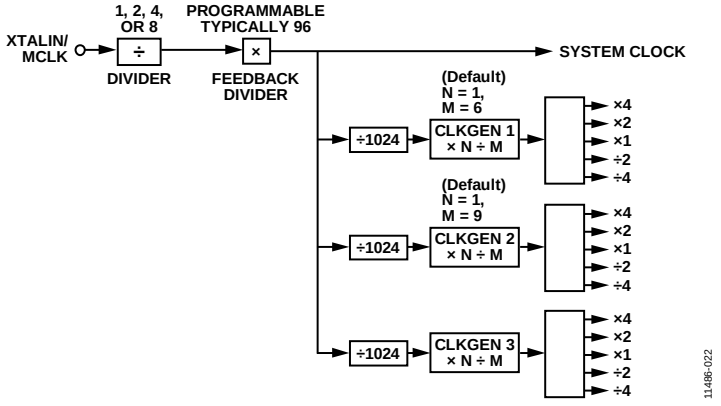

Figure 18. PLL and Clock Generators Block Diagram

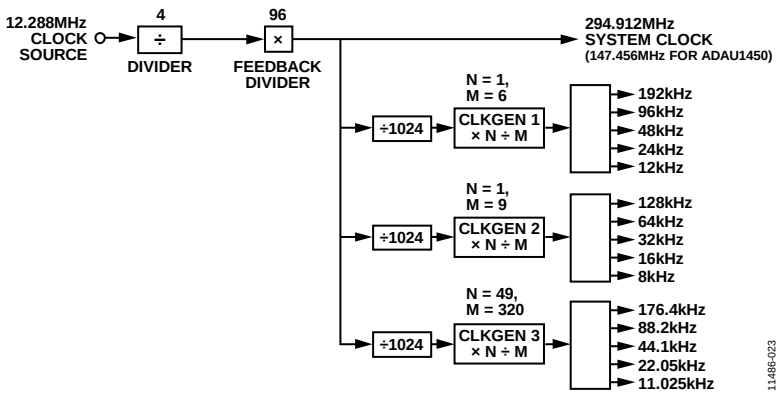

Figure 19. PLL and Audio Clock Generators with Default Settings and Resulting Clock Frequencies Labeled, XTALIN/MCLK = 12.288 MHz

Asynchronous Sample Rate Converter Input Routing

Any asynchronous input can be routed to the ASRCs to be resynchronized to a desired target sample rate (see Figure 50). The source signals for any ASRC can come from any of the serial inputs, any of the DSP-to-ASRC channels, the S/PDIF receiver, or the digital PDM microphone inputs. There are eight ASRCs, each with two input channels and two output channels. This means a total of 16 channels can pass through the ASRCs.

Asynchronous input signals (either serial inputs, PDM microphone inputs, or the S/PDIF input) typically need to be routed to an ASRC and then synchronized to the DSP core rate. They are then available for input to the DSP core for processing.

In the example shown in Figure 51, the two channels from the S/PDIF receiver are routed to one of the ASRCs and then to the DSP core. For this example, the corresponding ASRC input selector register (Register 0xF100 to Register 0xF107, ASRC_INPUTx), Bits[2:0] (ASRC_SOURCE) is set to 0b011 to take the input from the S/PDIF receiver. Likewise, the corresponding ASRC output rate selector register (Register 0xF140 to Register 0xF147, ASRC_OUT_RATEx, Bits[3:0] (ASRC_RATE)) is set to 0b0101 to synchronize the ASRC output data to the DSP core sample rate.

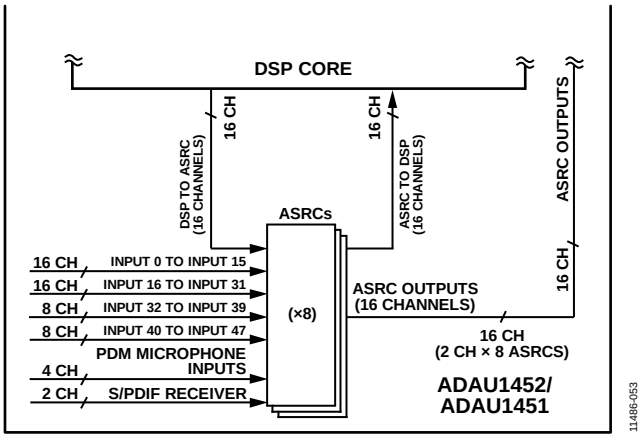

Figure 50. Channel Routing to ASRC Inputs

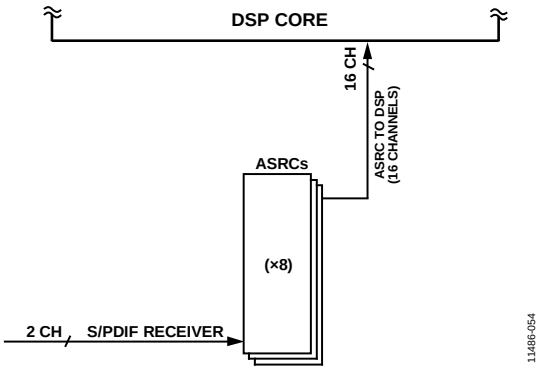

Figure 51. Example ASRC Routing for Asynchronous Input to the DSP Core

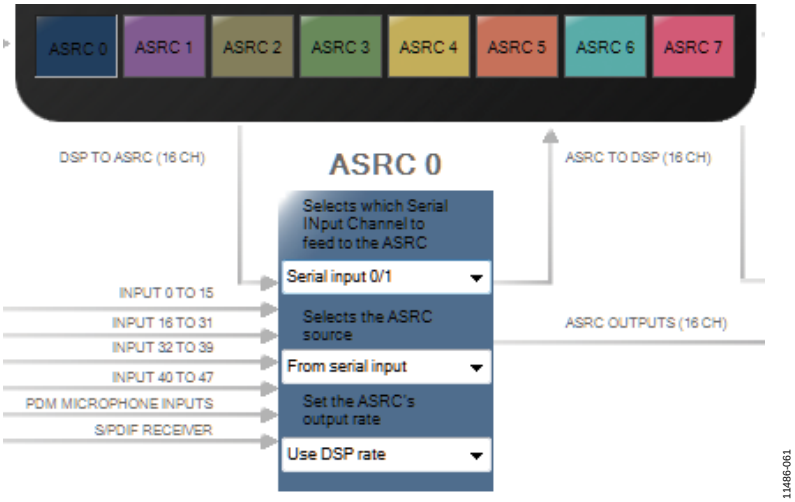

Figure 59. Configuring the ASRC Input Source and Target Rate in SigmaStudio

CONTROL REGISTERS

All control registers store 16 bits (two bytes) of data. The register map for the ADAU1452/ADAU1451/ADAU1450 is defined in Table 64.

Table 64. Control Register Summary

Address	Register Name	Description	Reset	RW
0xF000	PLL_CTRL0	PLL feedback divider	0x0060	RW
0xF001	PLL_CTRL1	PLL prescale divider	0x0000	RW
0xF002	PLL_CLK_SRC	PLL clock source	0x0000	RW
0xF003	PLL_ENABLE	PLL enable	0x0000	RW
0xF004	PLL_LOCK	PLL lock	0x0000	R
0xF005	MCLK_OUT	CLKOUT control	0x0000	RW
0xF006	PLL_WATCHDOG	Analog PLL watchdog control	0x0001	RW
0xF020	CLK_GEN1_M	Denominator (M) for Clock Generator 1	0x0006	RW
0xF021	CLK_GEN1_N	Numerator (N) for Clock Generator 1	0x0001	RW
0xF022	CLK_GEN2_M	Denominator (M) for Clock Generator 2	0x0009	RW
0xF023	CLK_GEN2_N	Numerator (N) for Clock Generator 2	0x0001	RW
0xF024	CLK_GEN3_M	Denominator (M) for Clock Generator 3	0x0000	RW
0xF025	CLK_GEN3_N	Numerator for (N) Clock Generator 3	0x0000	RW
0xF026	CLK_GEN3_SRC	Input Reference for Clock Generator 3	0x000E	RW
0xF027	CLK_GEN3_LOCK	Lock Bit for Clock Generator 3 input reference	0x0000	R
0xF050	POWER_ENABLE0	Power Enable 0	0x0000	RW
0xF051	POWER_ENABLE1	Power Enable 1	0x0000	RW
0xF100	ASRC_INPUT0	ASRC input selector (ASRC 0, Channel 0 and Channel 1)	0x0000	RW
0xF101	ASRC_INPUT1	ASRC input selector (ASRC 1, Channel 2 and Channel 3)	0x0000	RW
0xF102	ASRC_INPUT2	ASRC input selector (ASRC 2, Channel 4 and Channel 5)	0x0000	RW
0xF103	ASRC_INPUT3	ASRC input selector (ASRC 3, Channel 6 and Channel 7)	0x0000	RW
0xF104	ASRC_INPUT4	ASRC input selector (ASRC 4, Channel 8 and Channel 9)	0x0000	RW
0xF105	ASRC_INPUT5	ASRC input selector (ASRC 5, Channel 10 and Channel 11)	0x0000	RW
0xF106	ASRC_INPUT6	ASRC input selector (ASRC 6, Channel 12 and Channel 13)	0x0000	RW
0xF107	ASRC_INPUT7	ASRC input selector (ASRC 7, Channel 14 and Channel 15)	0x0000	RW
0xF140	ASRC_OUT_RATE0	ASRC output rate (ASRC 0, Channel 0 and Channel 1)	0x0000	RW
0xF141	ASRC_OUT_RATE1	ASRC output rate (ASRC 1, Channel 2 and Channel 3)	0x0000	RW
0xF142	ASRC_OUT_RATE2	ASRC output rate (ASRC 2, Channel 4 and Channel 5)	0x0000	RW
0xF143	ASRC_OUT_RATE3	ASRC output rate (ASRC 3, Channel 6 and Channel 7)	0x0000	RW
0xF144	ASRC_OUT_RATE4	ASRC output rate (ASRC 4, Channel 8 and Channel 9)	0x0000	RW
0xF145	ASRC_OUT_RATE5	ASRC output rate (ASRC 5, Channel 10 and Channel 11)	0x0000	RW
0xF146	ASRC_OUT_RATE6	ASRC output rate (ASRC 6, Channel 12 and Channel 13)	0x0000	RW
0xF147	ASRC_OUT_RATE7	ASRC output rate (ASRC 7, Channel 14 and Channel 15)	0x0000	RW
0xF180	SOUT_SOURCE0	Source of data for serial output ports (Channel 0 and Channel 1)	0x0000	RW
0xF181	SOUT_SOURCE1	Source of data for serial output ports (Channel 2 and Channel 3)	0x0000	RW
0xF182	SOUT_SOURCE2	Source of data for serial output ports (Channel 4 and Channel 5)	0x0000	RW
0xF183	SOUT_SOURCE3	Source of data for serial output ports (Channel 6 and Channel 7)	0x0000	RW
0xF184	SOUT_SOURCE4	Source of data for serial output ports (Channel 8 and Channel 9)	0x0000	RW
0xF185	SOUT_SOURCE5	Source of data for serial output ports (Channel 10 and Channel 11)	0x0000	RW
0xF186	SOUT_SOURCE6	Source of data for serial output ports (Channel 12 and Channel 13)	0x0000	RW
0xF187	SOUT_SOURCE7	Source of data for serial output ports (Channel 14 and Channel 15)	0x0000	RW
0xF188	SOUT_SOURCE8	Source of data for serial output ports (Channel 16 and Channel 17)	0x0000	RW
0xF189	SOUT_SOURCE9	Source of data for serial output ports (Channel 18 and Channel 19)	0x0000	RW
0xF18A	SOUT_SOURCE10	Source of data for serial output ports (Channel 20 and Channel 21)	0x0000	RW
0xF18B	SOUT_SOURCE11	Source of data for serial output ports (Channel 22 and Channel 23)	0x0000	RW
0xF18C	SOUT_SOURCE12	Source of data for serial output ports (Channel 24 and Channel 25)	0x0000	RW
0xF18D	SOUT_SOURCE13	Source of data for serial output ports (Channel 26 and Channel 27)	0x0000	RW
0xF18E	SOUT_SOURCE14	Source of data for serial output ports (Channel 28 and Channel 29)	0x0000	RW
0xF18F	SOUT_SOURCE15	Source of data for serial output ports (Channel 30 and Channel 31)	0x0000	RW
0xF190	SOUT_SOURCE16	Source of data for serial output ports (Channel 32 and Channel 33)	0x0000	RW

Address	Register Name	Description	Reset	RW
0xF394	FTDM_OUT20	FTDM mapping for the serial outputs (Port 2, Channel 5, Bits[31:24])	0x0000	RW
0xF395	FTDM_OUT21	FTDM mapping for the serial outputs (Port 2, Channel 5, Bits[23:16])	0x0000	RW
0xF396	FTDM_OUT22	FTDM mapping for the serial outputs (Port 2, Channel 5, Bits[15:8])	0x0000	RW
0xF397	FTDM_OUT23	FTDM mapping for the serial outputs (Port 2, Channel 5, Bits[7:0])	0x0000	RW
0xF398	FTDM_OUT24	FTDM mapping for the serial outputs (Port 2, Channel 6, Bits[31:24])	0x0000	RW
0xF399	FTDM_OUT25	FTDM mapping for the serial outputs (Port 2, Channel 6, Bits[23:16])	0x0000	RW
0xF39A	FTDM_OUT26	FTDM mapping for the serial outputs (Port 2, Channel 6, Bits[15:8])	0x0000	RW
0xF39B	FTDM_OUT27	FTDM mapping for the serial outputs (Port 2, Channel 6, Bits[7:0])	0x0000	RW
0xF39C	FTDM_OUT28	FTDM mapping for the serial outputs (Port 2, Channel 7, Bits[31:24])	0x0000	RW
0xF39D	FTDM_OUT29	FTDM mapping for the serial outputs (Port 2, Channel 7, Bits[23:16])	0x0000	RW
0xF39E	FTDM_OUT30	FTDM mapping for the serial outputs (Port 2, Channel 7, Bits[15:8])	0x0000	RW
0xF39F	FTDM_OUT31	FTDM mapping for the serial outputs (Port 2, Channel 7, Bits[7:0])	0x0000	RW
0xF3A0	FTDM_OUT32	FTDM mapping for the serial outputs (Port 3, Channel 0, Bits[31:24])	0x0000	RW
0xF3A1	FTDM_OUT33	FTDM mapping for the serial outputs (Port 3, Channel 0, Bits[23:16])	0x0000	RW
0xF3A2	FTDM_OUT34	FTDM mapping for the serial outputs (Port 3, Channel 0, Bits[15:8])	0x0000	RW
0xF3A3	FTDM_OUT35	FTDM mapping for the serial outputs (Port 3, Channel 0, Bits[7:0])	0x0000	RW
0xF3A4	FTDM_OUT36	FTDM mapping for the serial outputs (Port 3, Channel 1, Bits[31:24])	0x0000	RW
0xF3A5	FTDM_OUT37	FTDM mapping for the serial outputs (Port 3, Channel 1, Bits[23:16])	0x0000	RW
0xF3A6	FTDM_OUT38	FTDM mapping for the serial outputs (Port 3, Channel 1, Bits[15:8])	0x0000	RW
0xF3A7	FTDM_OUT39	FTDM mapping for the serial outputs (Port 3, Channel 1, Bits[7:0])	0x0000	RW
0xF3A8	FTDM_OUT40	FTDM mapping for the serial outputs (Port 3, Channel 2, Bits[31:24])	0x0000	RW
0xF3A9	FTDM_OUT41	FTDM mapping for the serial outputs (Port 3, Channel 2, Bits[23:16])	0x0000	RW
0xF3AA	FTDM_OUT42	FTDM mapping for the serial outputs (Port 3, Channel 2, Bits[15:8])	0x0000	RW
0xF3AB	FTDM_OUT43	FTDM mapping for the serial outputs (Port 3, Channel 2, Bits[7:0])	0x0000	RW
0xF3AC	FTDM_OUT44	FTDM mapping for the serial outputs (Port 3, Channel 3, Bits[31:24])	0x0000	RW
0xF3AD	FTDM_OUT45	FTDM mapping for the serial outputs (Port 3, Channel 3, Bits[23:16])	0x0000	RW
0xF3AE	FTDM_OUT46	FTDM mapping for the serial outputs (Port 3, Channel 3, Bits[15:8])	0x0000	RW
0xF3AF	FTDM_OUT47	FTDM mapping for the serial outputs (Port 3, Channel 3, Bits[7:0])	0x0000	RW
0xF3B0	FTDM_OUT48	FTDM mapping for the serial outputs (Port 3, Channel 4, Bits[31:24])	0x0000	RW
0xF3B1	FTDM_OUT49	FTDM mapping for the serial outputs (Port 3, Channel 4, Bits[23:16])	0x0000	RW
0xF3B2	FTDM_OUT50	FTDM mapping for the serial outputs (Port 3, Channel 4, Bits[15:8])	0x0000	RW
0xF3B3	FTDM_OUT51	FTDM mapping for the serial outputs (Port 3, Channel 4, Bits[7:0])	0x0000	RW
0xF3B4	FTDM_OUT52	FTDM mapping for the serial outputs (Port 3, Channel 5, Bits[31:24])	0x0000	RW
0xF3B5	FTDM_OUT53	FTDM mapping for the serial outputs (Port 3, Channel 5, Bits[23:16])	0x0000	RW
0xF3B6	FTDM_OUT54	FTDM mapping for the serial outputs (Port 3, Channel 5, Bits[15:8])	0x0000	RW
0xF3B7	FTDM_OUT55	FTDM mapping for the serial outputs (Port 3, Channel 5, Bits[7:0])	0x0000	RW
0xF3B8	FTDM_OUT56	FTDM mapping for the serial outputs (Port 3, Channel 6, Bits[31:24])	0x0000	RW
0xF3B9	FTDM_OUT57	FTDM mapping for the serial outputs (Port 3, Channel 6, Bits[23:16])	0x0000	RW
0xF3BA	FTDM_OUT58	FTDM mapping for the serial outputs (Port 3, Channel 6, Bits[15:8])	0x0000	RW
0xF3BB	FTDM_OUT59	FTDM mapping for the serial outputs (Port 3, Channel 6, Bits[7:0])	0x0000	RW
0xF3BC	FTDM_OUT60	FTDM mapping for the serial outputs (Port 3, Channel 7, Bits[31:24])	0x0000	RW
0xF3BD	FTDM_OUT61	FTDM mapping for the serial outputs (Port 3, Channel 7, Bits[23:16])	0x0000	RW
0xF3BE	FTDM_OUT62	FTDM mapping for the serial outputs (Port 3, Channel 7, Bits[15:8])	0x0000	RW
0xF3BF	FTDM_OUT63	FTDM mapping for the serial outputs (Port 3, Channel 7, Bits[7:0])	0x0000	RW
0xF400	HIBERNATE	Hibernate setting	0x0000	RW
0xF401	START_PULSE	Start pulse selection	0x0002	RW
0xF402	START_CORE	Instruction to start the core	0x0000	RW
0xF403	KILL_CORE	Instruction to stop the core	0x0000	RW
0xF404	START_ADDRESS	Start address of the program	0x0000	RW
0xF405	CORE_STATUS	Core status	0x0000	R
0xF421	PANIC_CLEAR	Clear the panic manager	0x0000	RW
0xF422	PANIC_PARITY_MASK	Panic parity	0x0003	RW
0xF423	PANIC_SOFTWARE_MASK	Panic Mask 0	0x0000	RW
0xF424	PANIC_WD_MASK	Panic Mask 1	0x0000	RW

Address	Register Name	Description	Reset	RW
0xF53A	MP10_READ	Multipurpose pin read value (LRCLK_IN0/MP10)	0x0000	R
0xF53B	MP11_READ	Multipurpose pin read value (LRCLK_IN1/MP11)	0x0000	R
0xF53C	MP12_READ	Multipurpose pin read value (LRCLK_IN2/MP12)	0x0000	R
0xF53D	MP13_READ	Multipurpose pin read value (LRCLK_IN3/MP13)	0x0000	R
0xF560	DMIC_CTRL0	Digital PDM microphone control (Channel 0 and Channel 1)	0x4000	RW
0xF561	DMIC_CTRL1	Digital PDM microphone control (Channel 2 and Channel 3)	0x4000	RW
0xF580	ASRC_LOCK	ASRC lock status	0x0000	R
0xF581	ASRC_MUTE	ASRC mute	0x0000	RW
0xF582	ASRC0_RATIO	ASRC ratio (ASRC 0, Channel 0 and Channel 1)	0x0000	R
0xF583	ASRC1_RATIO	ASRC ratio (ASRC 1, Channel 2 and Channel 3)	0x0000	R
0xF584	ASRC2_RATIO	ASRC ratio (ASRC 2, Channel 4 and Channel 5)	0x0000	R
0xF585	ASRC3_RATIO	ASRC ratio (ASRC 3, Channel 6 and Channel 7)	0x0000	R
0xF586	ASRC4_RATIO	ASRC ratio (ASRC 4, Channel 8 and Channel 9)	0x0000	R
0xF587	ASRC5_RATIO	ASRC ratio (ASRC 5, Channel 10 and Channel 11)	0x0000	R
0xF588	ASRC6_RATIO	ASRC ratio (ASRC 6, Channel 12 and Channel 13)	0x0000	R
0xF589	ASRC7_RATIO	ASRC ratio (ASRC 7, Channel 14 and Channel 15)	0x0000	R
0xF5A0	ADC_READ0	Auxiliary ADC read value (AUXADC0)	0x0000	R
0xF5A1	ADC_READ1	Auxiliary ADC read value (AUXADC1)	0x0000	R
0xF5A2	ADC_READ2	Auxiliary ADC read value (AUXADC2)	0x0000	R
0xF5A3	ADC_READ3	Auxiliary ADC read value (AUXADC3)	0x0000	R
0xF5A4	ADC_READ4	Auxiliary ADC read value (AUXADC4)	0x0000	R
0xF5A5	ADC_READ5	Auxiliary ADC read value (AUXADC5)	0x0000	R
0xF600	SPDIF_LOCK_DET	S/PDIF receiver lock bit detection	0x0000	R
0xF601	SPDIF_RX_CTRL	S/PDIF receiver control	0x0000	RW
0xF602	SPDIF_RX_DECODE	Decoded signals from the S/PDIF receiver	0x0000	R
0xF603	SPDIF_RX_COMPRMODE	Compression mode from the S/PDIF receiver	0x0000	R
0xF604	SPDIF_RESTART	Automatically resume S/PDIF receiver audio input	0x0000	RW
0xF605	SPDIF_LOSS_OF_LOCK	S/PDIF receiver loss of lock detection	0x0000	R
0xF608	SPDIF_AUX_EN	S/PDIF receiver auxiliary outputs enable	0x0000	RW
0xF60F	SPDIF_RX_AUXBIT_READY	S/PDIF receiver auxiliary bits ready flag	0x0000	R
0xF610	SPDIF_RX_CS_LEFT_0	S/PDIF receiver channel status bits (left)	0x0000	R
0xF611	SPDIF_RX_CS_LEFT_1	S/PDIF receiver channel status bits (left)	0x0000	R
0xF612	SPDIF_RX_CS_LEFT_2	S/PDIF receiver channel status bits (left)	0x0000	R
0xF613	SPDIF_RX_CS_LEFT_3	S/PDIF receiver channel status bits (left)	0x0000	R
0xF614	SPDIF_RX_CS_LEFT_4	S/PDIF receiver channel status bits (left)	0x0000	R
0xF615	SPDIF_RX_CS_LEFT_5	S/PDIF receiver channel status bits (left)	0x0000	R
0xF616	SPDIF_RX_CS_LEFT_6	S/PDIF receiver channel status bits (left)	0x0000	R
0xF617	SPDIF_RX_CS_LEFT_7	S/PDIF receiver channel status bits (left)	0x0000	R
0xF618	SPDIF_RX_CS_LEFT_8	S/PDIF receiver channel status bits (left)	0x0000	R
0xF619	SPDIF_RX_CS_LEFT_9	S/PDIF receiver channel status bits (left)	0x0000	R
0xF61A	SPDIF_RX_CS_LEFT_10	S/PDIF receiver channel status bits (left)	0x0000	R
0xF61B	SPDIF_RX_CS_LEFT_11	S/PDIF receiver channel status bits (left)	0x0000	R
0xF620	SPDIF_RX_CS_RIGHT_0	S/PDIF receiver channel status bits (right)	0x0000	R
0xF621	SPDIF_RX_CS_RIGHT_1	S/PDIF receiver channel status bits (right)	0x0000	R
0xF622	SPDIF_RX_CS_RIGHT_2	S/PDIF receiver channel status bits (right)	0x0000	R
0xF623	SPDIF_RX_CS_RIGHT_3	S/PDIF receiver channel status bits (right)	0x0000	R
0xF624	SPDIF_RX_CS_RIGHT_4	S/PDIF receiver channel status bits (right)	0x0000	R
0xF625	SPDIF_RX_CS_RIGHT_5	S/PDIF receiver channel status bits (right)	0x0000	R
0xF626	SPDIF_RX_CS_RIGHT_6	S/PDIF receiver channel status bits (right)	0x0000	R
0xF627	SPDIF_RX_CS_RIGHT_7	S/PDIF receiver channel status bits (right)	0x0000	R
0xF628	SPDIF_RX_CS_RIGHT_8	S/PDIF receiver channel status bits (right)	0x0000	R
0xF629	SPDIF_RX_CS_RIGHT_9	S/PDIF receiver channel status bits (right)	0x0000	R
0xF62A	SPDIF_RX_CS_RIGHT_10	S/PDIF receiver channel status bits (right)	0x0000	R
0xF62B	SPDIF_RX_CS_RIGHT_11	S/PDIF receiver channel status bits (right)	0x0000	R

Address	Register Name	Description	Reset	RW
0xF676	SPDIF_RX_PB_LEFT_6	S/PDIF receiver parity bits (left)	0x0000	R
0xF677	SPDIF_RX_PB_LEFT_7	S/PDIF receiver parity bits (left)	0x0000	R
0xF678	SPDIF_RX_PB_LEFT_8	S/PDIF receiver parity bits (left)	0x0000	R
0xF679	SPDIF_RX_PB_LEFT_9	S/PDIF receiver parity bits (left)	0x0000	R
0xF67A	SPDIF_RX_PB_LEFT_10	S/PDIF receiver parity bits (left)	0x0000	R
0xF67B	SPDIF_RX_PB_LEFT_11	S/PDIF receiver parity bits (left)	0x0000	R
0xF680	SPDIF_RX_PB_RIGHT_0	S/PDIF receiver parity bits (right)	0x0000	R
0xF681	SPDIF_RX_PB_RIGHT_1	S/PDIF receiver parity bits (right)	0x0000	R
0xF682	SPDIF_RX_PB_RIGHT_2	S/PDIF receiver parity bits (right)	0x0000	R
0xF683	SPDIF_RX_PB_RIGHT_3	S/PDIF receiver parity bits (right)	0x0000	R
0xF684	SPDIF_RX_PB_RIGHT_4	S/PDIF receiver parity bits (right)	0x0000	R
0xF685	SPDIF_RX_PB_RIGHT_5	S/PDIF receiver parity bits (right)	0x0000	R
0xF686	SPDIF_RX_PB_RIGHT_6	S/PDIF receiver parity bits (right)	0x0000	R
0xF687	SPDIF_RX_PB_RIGHT_7	S/PDIF receiver parity bits (right)	0x0000	R
0xF688	SPDIF_RX_PB_RIGHT_8	S/PDIF receiver parity bits (right)	0x0000	R
0xF689	SPDIF_RX_PB_RIGHT_9	S/PDIF receiver parity bits (right)	0x0000	R
0xF68A	SPDIF_RX_PB_RIGHT_10	S/PDIF receiver parity bits (right)	0x0000	R
0xF68B	SPDIF_RX_PB_RIGHT_11	S/PDIF receiver parity bits (right)	0x0000	R
0xF690	SPDIF_TX_EN	S/PDIF transmitter enable	0x0000	RW
0xF691	SPDIF_TX_CTRL	S/PDIF transmitter control	0x0000	RW
0xF69F	SPDIF_TX_AUXBIT_SOURCE	S/PDIF transmitter auxiliary bits source select	0x0000	RW
0xF6A0	SPDIF_TX_CS_LEFT_0	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6A1	SPDIF_TX_CS_LEFT_1	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6A2	SPDIF_TX_CS_LEFT_2	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6A3	SPDIF_TX_CS_LEFT_3	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6A4	SPDIF_TX_CS_LEFT_4	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6A5	SPDIF_TX_CS_LEFT_5	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6A6	SPDIF_TX_CS_LEFT_6	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6A7	SPDIF_TX_CS_LEFT_7	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6A8	SPDIF_TX_CS_LEFT_8	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6A9	SPDIF_TX_CS_LEFT_9	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6AA	SPDIF_TX_CS_LEFT_10	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6AB	SPDIF_TX_CS_LEFT_11	S/PDIF transmitter channel status bits (left)	0x0000	RW
0xF6B0	SPDIF_TX_CS_RIGHT_0	S/PDIF transmitter channel status bits (right)	0x0000	RW
0xF6B1	SPDIF_TX_CS_RIGHT_1	S/PDIF transmitter channel status bits (right)	0x0000	RW
0xF6B2	SPDIF_TX_CS_RIGHT_2	S/PDIF transmitter channel status bits (right)	0x0000	RW
0xF6B3	SPDIF_TX_CS_RIGHT_3	S/PDIF transmitter channel status bits (right)	0x0000	RW
0xF6B4	SPDIF_TX_CS_RIGHT_4	S/PDIF transmitter channel status bits (right)	0x0000	RW
0xF6B5	SPDIF_TX_CS_RIGHT_5	S/PDIF transmitter channel status bits (right))	0x0000	RW
0xF6B6	SPDIF_TX_CS_RIGHT_6	S/PDIF transmitter channel status bits (right))	0x0000	RW
0xF6B7	SPDIF_TX_CS_RIGHT_7	S/PDIF transmitter channel status bits (right)	0x0000	RW
0xF6B8	SPDIF_TX_CS_RIGHT_8	S/PDIF transmitter channel status bits (right)	0x0000	RW
0xF6B9	SPDIF_TX_CS_RIGHT_9	S/PDIF transmitter channel status bits (right)	0x0000	RW
0xF6BA	SPDIF_TX_CS_RIGHT_10	S/PDIF transmitter channel status bits (right)	0x0000	RW
0xF6BB	SPDIF_TX_CS_RIGHT_11	S/PDIF transmitter channel status bits (right)	0x0000	RW
0xF6C0	SPDIF_TX_UD_LEFT_0	S/PDIF transmitter user data bits (left)	0x0000	RW
0xF6C1	SPDIF_TX_UD_LEFT_1	S/PDIF transmitter user data bits (left)	0x0000	RW
0xF6C2	SPDIF_TX_UD_LEFT_2	S/PDIF transmitter user data bits (left)	0x0000	RW
0xF6C3	SPDIF_TX_UD_LEFT_3	S/PDIF transmitter user data bits (left)	0x0000	RW
0xF6C4	SPDIF_TX_UD_LEFT_4	S/PDIF transmitter user data bits (left)	0x0000	RW
0xF6C5	SPDIF_TX_UD_LEFT_5	S/PDIF transmitter user data bits (left)	0x0000	RW
0xF6C6	SPDIF_TX_UD_LEFT_6	S/PDIF transmitter user data bits (left)	0x0000	RW
0xF6C7	SPDIF_TX_UD_LEFT_7	S/PDIF transmitter user data bits (left)	0x0000	RW
0xF6C8	SPDIF_TX_UD_LEFT_8	S/PDIF transmitter user data bits (left)	0x0000	RW

CONTROL REGISTER DETAILS

PLL CONFIGURATION REGISTERS

PLL Feedback Divider Register

Address: 0xF000, Reset: 0x0060, Name: PLL_CTRL0

This register is the value of the feedback divider in the PLL. This value effectively multiplies the frequency of the input clock to the PLL, creating the output system clock, which clocks the DSP core and other digital circuit blocks. The format of the value stored in this register is binary integer in 7.0 format. For example, the default feedback divider value of 96 is stored as 0x60. The value written to this register does not take effect until Register 0xF003 (PLL_ENABLE), Bit 0 (PLL_ENABLE) changes state from 0b0 to 0b1.

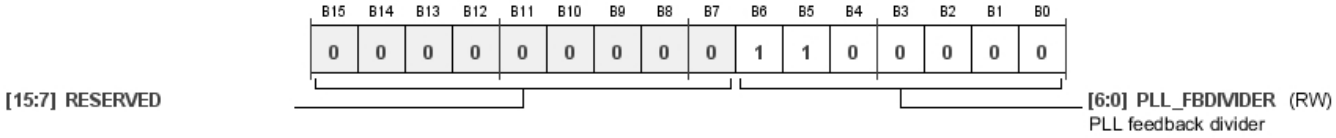

Table 65. Bit Descriptions for PLL_CTRL0

Bits	Bit Name	Settings	Description	Reset	Access
[15:7]	RESERVED			0x0	RW
[6:0]	PLL_FBDIVIDER		PLL feedback divider. This is the value of the feedback divider in the PLL, which effectively multiplies the frequency of the input clock to the PLL, creating the output system clock, which clocks the DSP core and other digital circuit blocks. The format of the value stored in this register is binary integer in 7.0 format. For example, the default feedback divider value of 96 is stored as 0x60.	0x60	RW

PLL Prescale Divider Register

Address: 0xF001, Reset: 0x0000, Name: PLL_CTRL1

This register sets the input prescale divider for the PLL. The value written to this register does not take effect until Register 0xF003 (PLL_ENABLE), Bit 0 (PLL_ENABLE) changes state from 0b0 to 0b1.

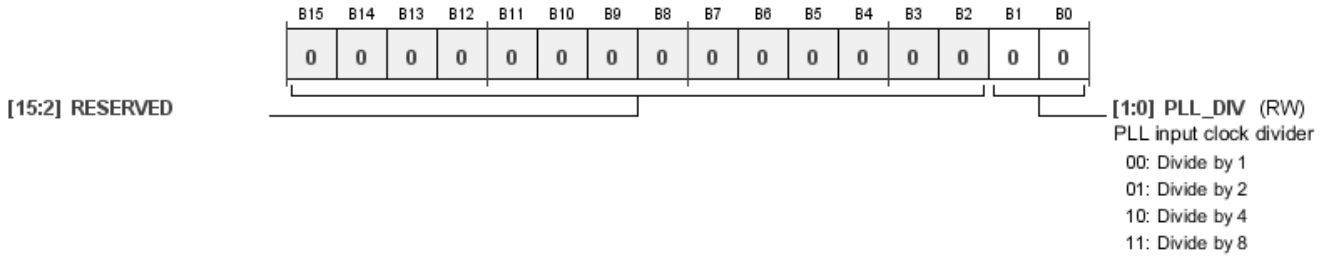

Table 66. Bit Descriptions for PLL_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[15:2]	RESERVED			0x0	RW
[1:0]	PLL_DIV		PLL input clock divider. This prescale clock divider creates the PLL input clock from the externally input master clock. The nominal frequency of the PLL input is 3.072 MHz. Therefore, if the input master clock frequency is 3.072 MHz, set the prescale clock divider to divide by 1. If the input clock is 12.288 MHz, set the prescale clock divider to divide by 4. The goal is to make the input to the PLL as close to 3.072 MHz as possible.	0x0	RW
		00	Divide by 1		
		01	Divide by 2		
		10	Divide by 4		
		11	Divide by 8		

Input Reference for Clock Generator 3 Register

Address: 0xF026, Reset: 0x000E, Name: CLK_GEN3_SRC

Clock Generator 3 can generate audio clocks using the PLL output (system clock) as a reference, or it can optionally use a reference clock entering the device from an external source either on a multipurpose pin (MPx) or the S/PDIF receiver. This register determines the source of the reference signal.

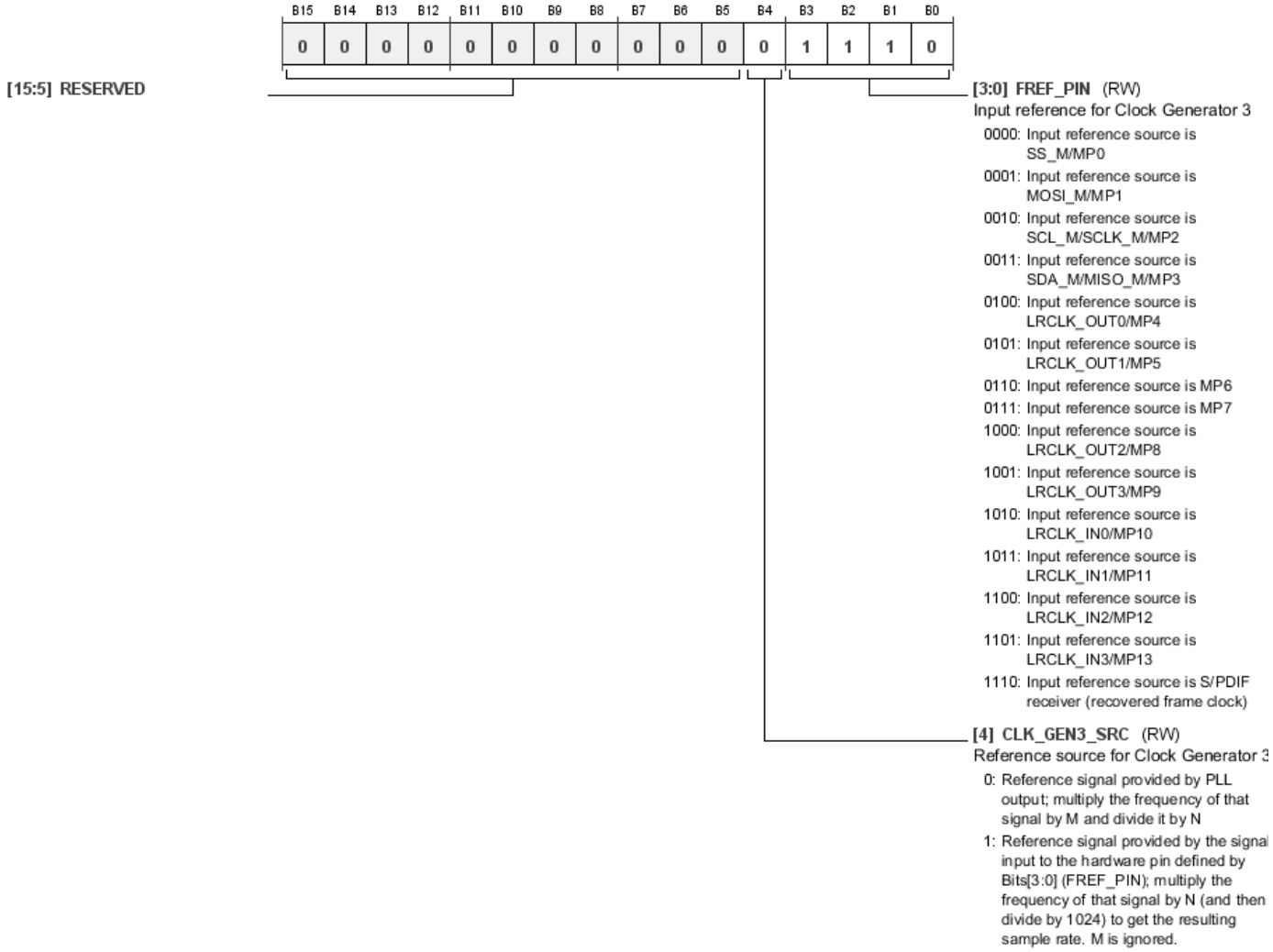

Table 78. Bit Descriptions for CLK_GEN3_SRC

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW

Core Status Register

Address: 0xF405, Reset: 0x0000, Name: CORE_STATUS

This read only register allows the user to check the status of the DSP core. To manually modify the core status, use Register 0xF400 (HIBERNATE), Register 0xF402 (START_CORE), and Register 0xF403 (KILL_CORE).

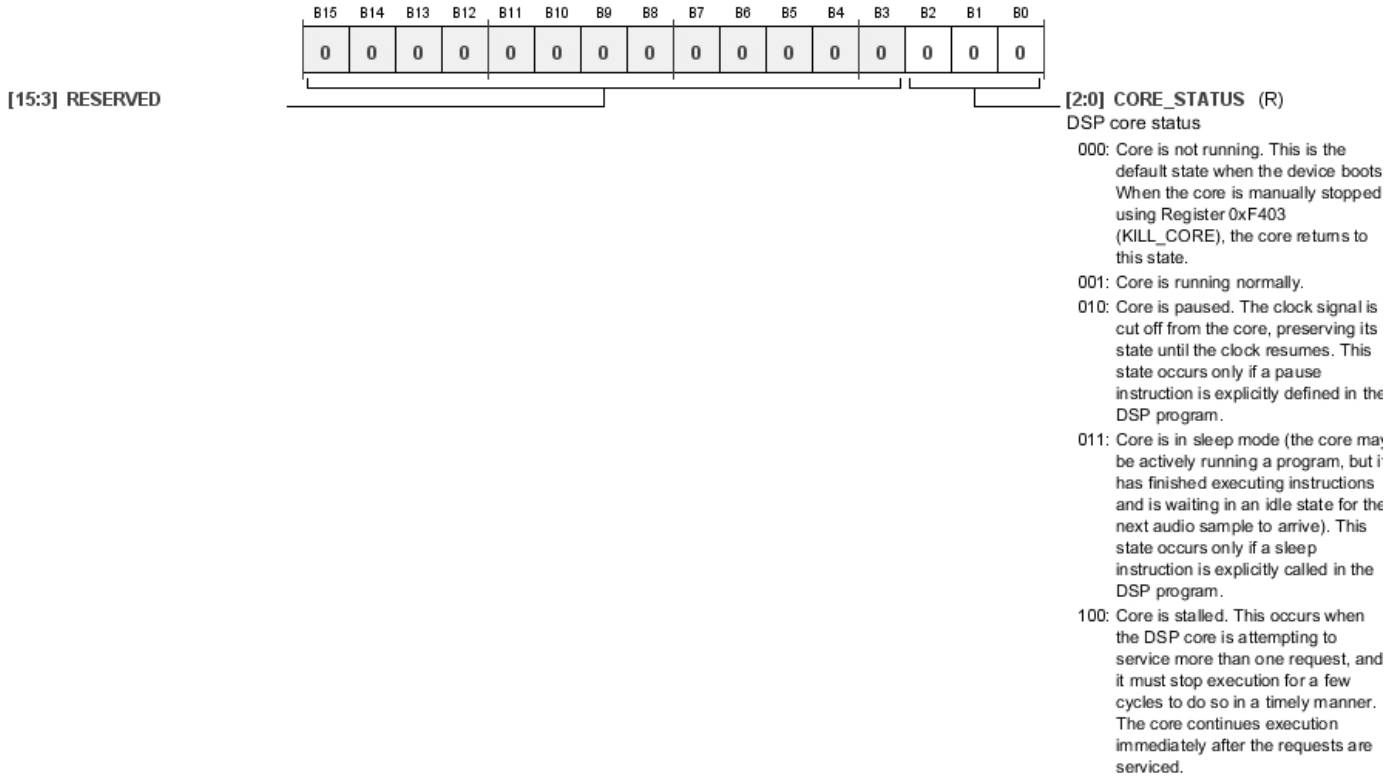

Table 95. Bit Descriptions for CORE_STATUS

Bits	Bit Name	Settings	Description	Reset	Access
[15:3]	RESERVED			0x0	RW
[2:0]	CORE_STATUS		DSP core status. These bits display the status of the DSP core at the moment the value is read.	0x0	RW
		000	Core is not running. This is the default state when the device boots. When the core is manually stopped using Register 0xF403 (KILL_CORE), the core returns to this state.		
		001	Core is running normally.		
		010	Core is paused. The clock signal is cut off from the core, preserving its state until the clock resumes. This state occurs only if a pause instruction is explicitly defined in the DSP program.		
		011	Core is in sleep mode (the core may be actively running a program, but it has finished executing instructions and is waiting in an idle state for the next audio sample to arrive). This state occurs only if a sleep instruction is explicitly called in the DSP program.		
		100	Core is stalled. This occurs when the DSP core is attempting to service more than one request, and it must stop execution for a few cycles to do so in a timely manner. The core continues execution immediately after the requests are serviced.		

Value for the Block Interrupt Counter Register

Address: 0xF451, Reset: 0x0000, Name: BLOCKINT_VALUE

This 16-bit register controls the duration in audio frames of a block. A counter increments each time a new frame start pulse is received by the DSP core. When the counter reaches the value determined by this register, a block interrupt is generated and the counter is reset. If block processing algorithms are used in SigmaStudio, SigmaStudio automatically sets this register accordingly. The user does not need to manually change the value of this register after SigmaStudio has configured it.

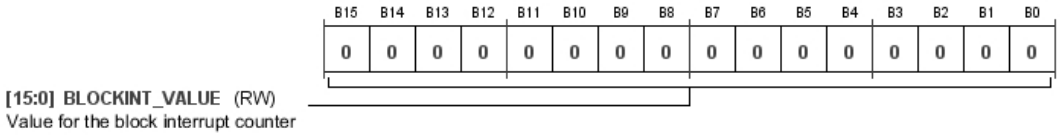

Table 108. Bit Descriptions for BLOCKINT_VALUE

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	BLOCKINT_VALUE		Value for the block interrupt counter.	0x0000	RW

Program Counter, Bits[23:16] Register

Address: 0xF460, Reset: 0x0000, Name: PROG_CNTR0

This register, in combination with Register 0xF461 (PROG_CNTR1), stores the current value of the program counter.

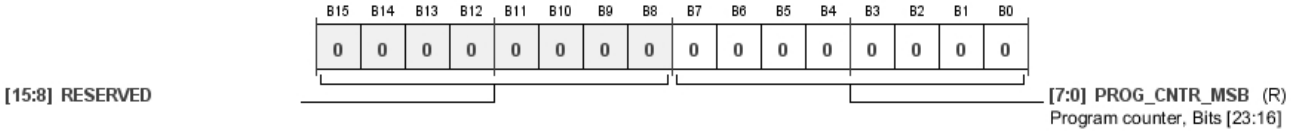

Table 109. Bit Descriptions for PROG_CNTR0

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x0	RW
[7:0]	PROG_CNTR_MSB		Program counter, Bits[23:16].	0x00	R

Program Counter, Bits[15:0] Register

Address: 0xF461, Reset: 0x0000, Name: PROG_CNTR1

This register, in combination with Register 0xF460 (PROG_CNTR0), stores the current value of the program counter.

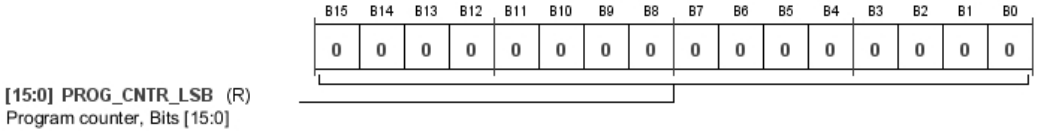

Table 110. Bit Descriptions for PROG_CNTR1

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	PROG_CNTR_LSB		Program counter, Bits[15:0].	0x0000	R

MULTIPURPOSE PIN CONFIGURATION REGISTERS

Multipurpose Pin Mode Register

Address: 0xF510 to 0xF51D (Increments of 0x1), Reset: 0x0000, Name: MPx_MODE

These 14 registers configure the multipurpose pins. Certain multipurpose pins can function as audio clock pins, control bus pins, or general-purpose input or output (GPIO) pins.

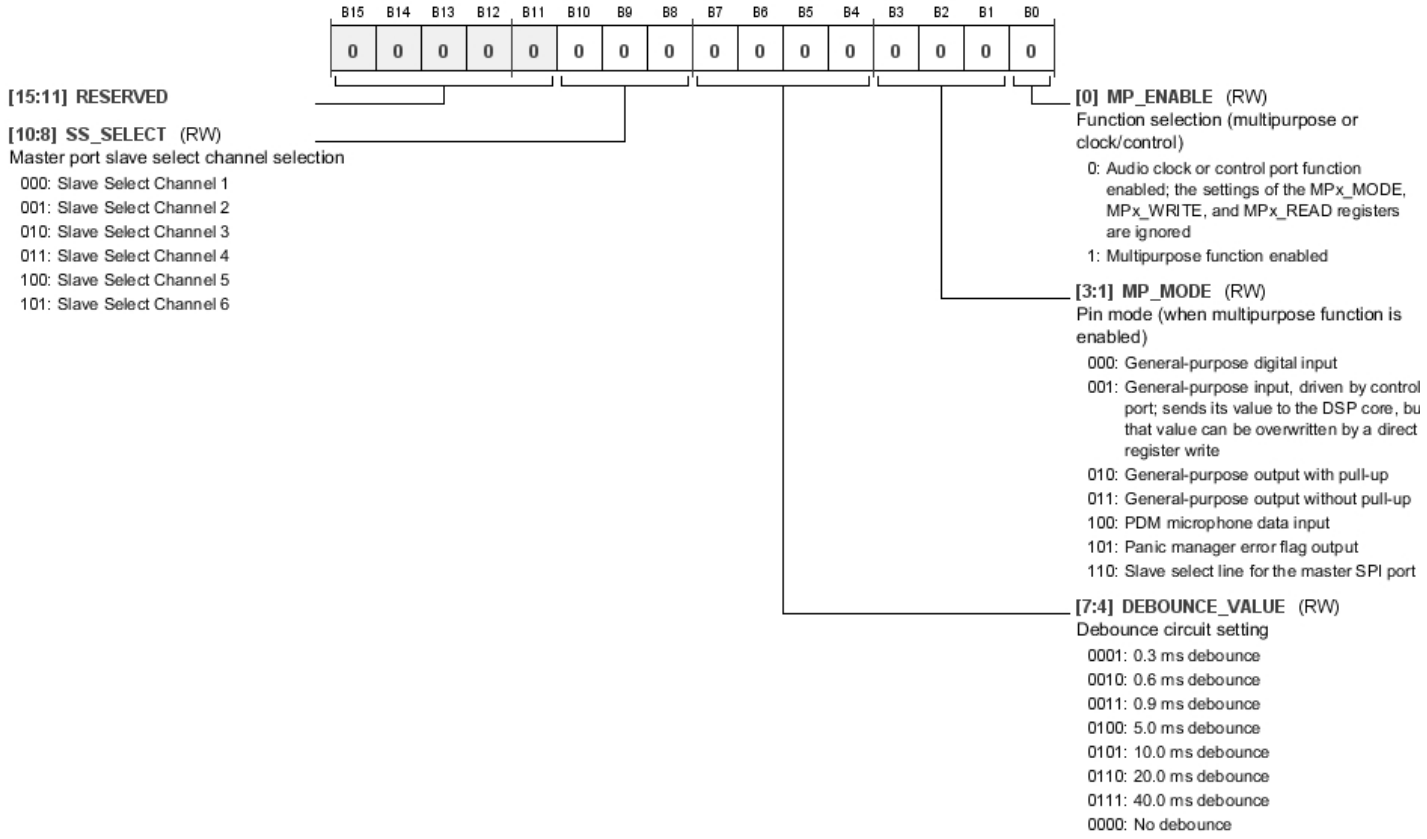

Table 116. Bit Descriptions for MPx_MODE

Bits	Bit Name	Settings	Description	Reset	Access
[15:11]	RESERVED			0x0	RW
[10:8]	SS_SELECT		Master port slave select channel selection. If the pin is configured as a slave select line (Bits[3:1] (MP_MODE) = 0b110), these bits configure which slave select channel the pin corresponds to. This allows multiple slave devices to be connected to the SPI master port, all using different slave select lines. The first slave select signal (Slave Select 0) is always routed to the SS_M/MP0 pin. The remaining six slave select lines can be routed to any multipurpose pin that has been configured as a slave select output.	0x0	RW
		000	Slave Select Channel 1		
		001	Slave Select Channel 2		
		010	Slave Select Channel 3		
		011	Slave Select Channel 4		
		100	Slave Select Channel 5		
		101	Slave Select Channel 6		

Bits	Bit Name	Settings	Description	Reset	Access
1	ASRC1L		ASRC 1 lock status.	0x0	R
		0	Locked		
		1	Unlocked		
0	ASRC0L		ASRC 0 lock status.	0x0	R
		0	Locked		
		1	Unlocked		

ASRC Mute Register

Address: 0xF581, Reset: 0x0000, Name: ASRC_MUTE

This register contains controls related to the muting of audio on ASRC channels. Bits[7:0] (ASRCxM) are individual mute controls for each stereo ASRC on the ADAU1452 and ADAU1451. Bit 8 (ASRC_RAMP0) and Bit 9 (ASRC_RAMP1) enable or disable an optional volume ramp-up and ramp-down to smoothly transition between muted and unmuted states. The mute and unmute ramps are linear. The duration of the ramp is determined by the sample rate of the DSP core, which is set by Register 0xF401 (START_PULSE). The ramp takes exactly 2048 input samples to complete. For example, if the sample rate of audio entering an ASRC channel is 48 kHz, the duration of the ramp is 2048/48,000 = 42.7 ms. If the sample rate of audio entering an ASRC channel is 6 kHz, the duration of the ramp is 2048/6000 = 341.3 ms. Bit 10 (LOCKMUTE) allows the ASRCs to automatically mute themselves in the event that lock status is lost or not attained.

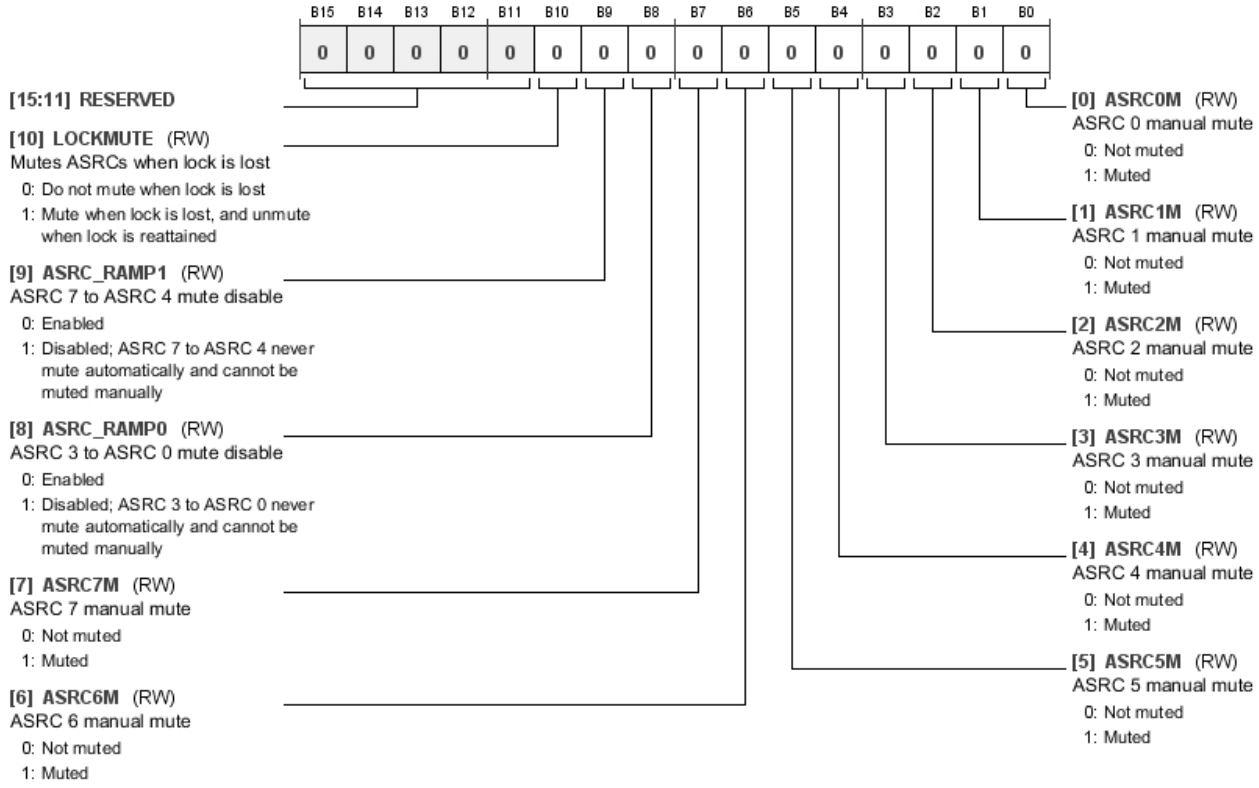

Table 121. Bit Descriptions for ASRC_MUTE

Bits	Bit Name	Settings	Description	Reset	Access
[15:11]	RESERVED			0x0	RW

S/PDIF Receiver Loss of Lock Detection Register

Address: 0xF605, Reset: 0x0000, Name: SPDIF_LOSS_OF_LOCK

This bit monitors the S/PDIF lock status and checks to see if the lock is lost during operation of the S/PDIF receiver on the ADAU1452 and ADAU1451. This condition can arise when, for example, a valid S/PDIF input signal was present for an extended period of time, but signal integrity worsened for a brief period, causing the receiver to then lose its lock to the input signal. In this case, Bit 0 (LOSS_OF_LOCK) transitions from 0b0 to 0b1 and remains set at 0b1 indefinitely. This indicates that, at some point during the operation of the device, lock to the input stream was lost. Bit 0 (LOSS_OF_LOCK) stays high at 0b1 until Register 0xF604 (SPDIF_RESTART), Bit 0 (RESTART_AUDIO), is set to 0b1, which clears Bit 0 (LOSS_OF_LOCK) back to 0b0. At that point, Register 0xF604 (SPDIF_RESTART), Bit 0 (RESTART_AUDIO), can be reset to 0b0 if required.

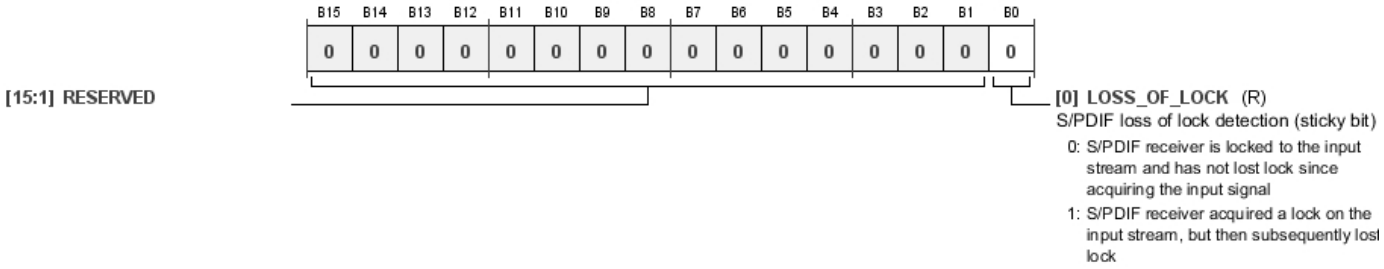

Table 129. Bit Descriptions for SPDIF_LOSS_OF_LOCK

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	LOSS_OF_LOCK		S/PDIF loss of lock detection (sticky bit).	0x0	R
		0	S/PDIF receiver is locked to the input stream and has not lost lock since acquiring the input signal		
		1	S/PDIF receiver acquired a lock on the input stream but then, subsequently, lost lock		

S/PDIF Transmitter Validity Bits (Right) Register

Address: 0xF6F0 to 0xF6FB (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_VB_RIGHT_x

These 12 registers allow the 192 validity bits encoded on the right channel of the output data stream of the S/PDIF transmitter on the ADAU1452 and ADAU1451 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

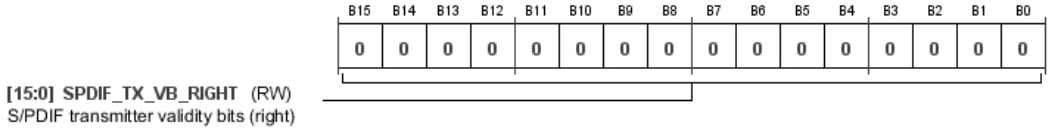

Table 148. Bit Descriptions for SPDIF_TX_VB_RIGHT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_VB_RIGHT		S/PDIF transmitter validity bits (right).	0x0000	RW

S/PDIF Transmitter Parity Bits (Left) Register

Address: 0xF700 to Address 0xF70B (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_PB_LEFT_x

These 12 registers allow the 192 parity bits encoded on the left channel of the output data stream of the S/PDIF transmitter on the ADAU1452 and ADAU1451 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

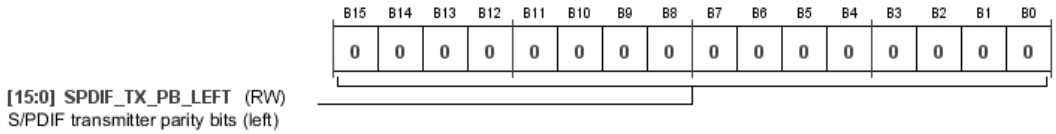

Table 149. Bit Descriptions for SPDIF_TX_PB_LEFT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_PB_LEFT		S/PDIF transmitter parity bits (left).	0x0000	RW

S/PDIF Transmitter Parity Bits (Right) Register

Address: 0xF710 to Address 0xF71B (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_PB_RIGHT_x

These 12 registers allow the 192 parity bits encoded on the right channel of the output data stream of the S/PDIF transmitter on the ADAU1452 and ADAU1451 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

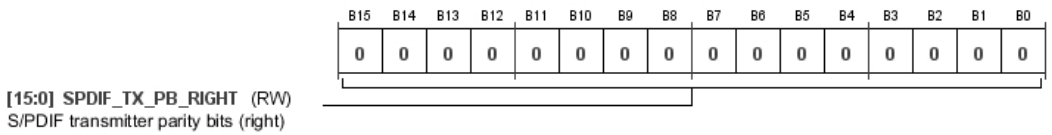

Table 150. Bit Descriptions for SPDIF_TX_PB_RIGHT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_PB_RIGHT		S/PDIF transmitter parity bits (right).	0x0000	RW

SS_M/MP0 Pin Drive Strength and Slew Rate Register

Address: 0xF79F, Reset: 0x0018, Name: SS_M_PIN

This register configures the drive strength, slew rate, and pull resistors for the SS_M/MP0 pin.

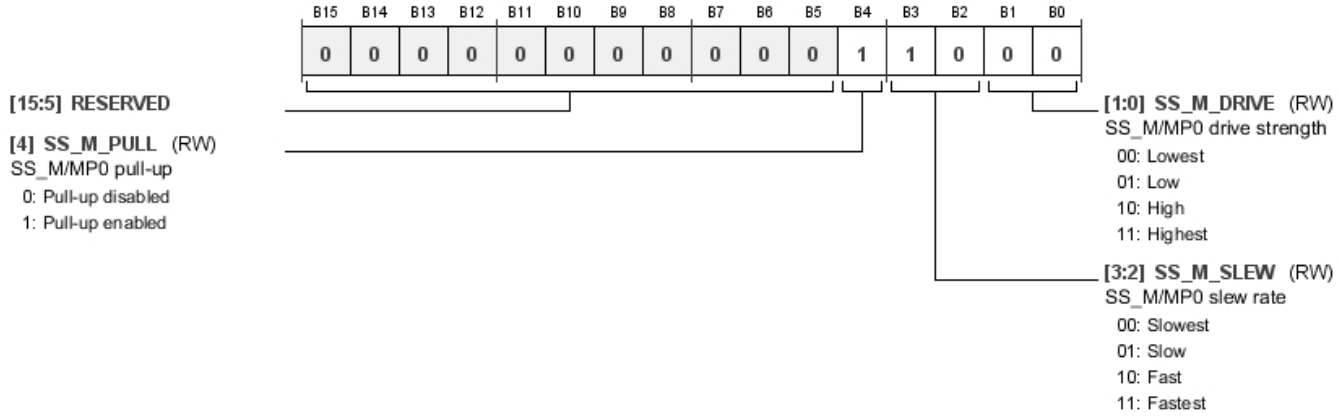

Table 164. Bit Descriptions for SS_M_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	SS_M_PULL		SS_M/MP0 pull-up.	0x1	RW
		0	Pull-up disabled		
		1	Pull-up enabled		
[3:2]	SS_M_SLEW		SS_M/MP0 slew rate.	0x2	RW
		00	Slowest		
		01	Slow		
		10	Fast		
		11	Fastest		
[1:0]	SS_M_DRIVE		SS_M/MP0 drive strength.	0x0	RW
		00	Lowest		
		01	Low		
		10	High		
		11	Highest		

MOSI_M/MP1 Pin Drive Strength and Slew Rate Register

Address: 0xF7A0, Reset: 0x0018, Name: MOSI_M_PIN

This register configures the drive strength, slew rate, and pull resistors for the MOSI_M/MP1 pin.

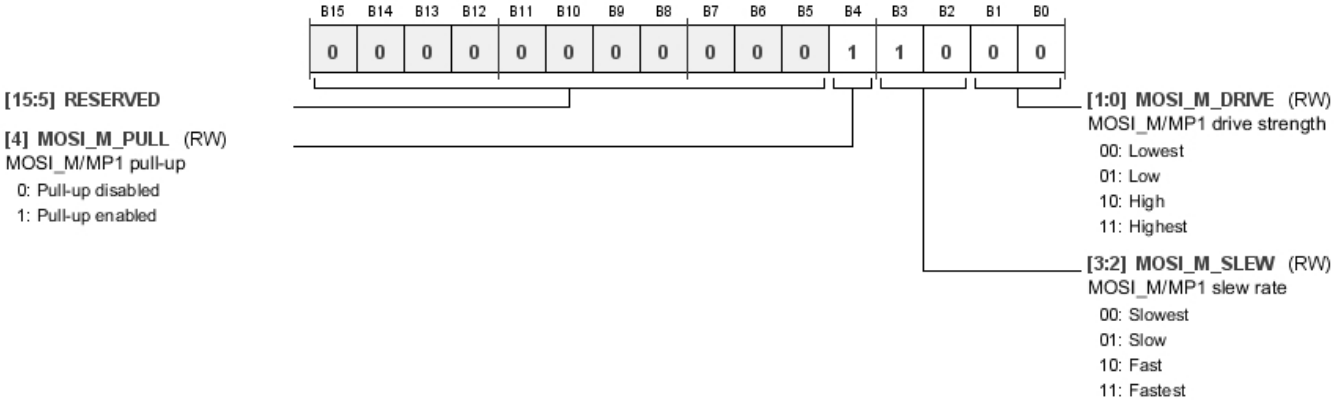

Table 165. Bit Descriptions for MOSI_M_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	MOSI_M_PULL		MOSI_M/MP1 pull-up.	0x1	RW
		0	Pull-up disabled		
		1	Pull-up enabled		
[3:2]	MOSI_M_SLEW		MOSI_M/MP1 slew rate.	0x2	RW
		00	Slowest		
		01	Slow		
		10	Fast		
		11	Fastest		
[1:0]	MOSI_M_DRIVE		MOSI_M/MP1 drive strength.	0x0	RW
		00	Lowest		
		01	Low		
		10	High		
		11	Highest		