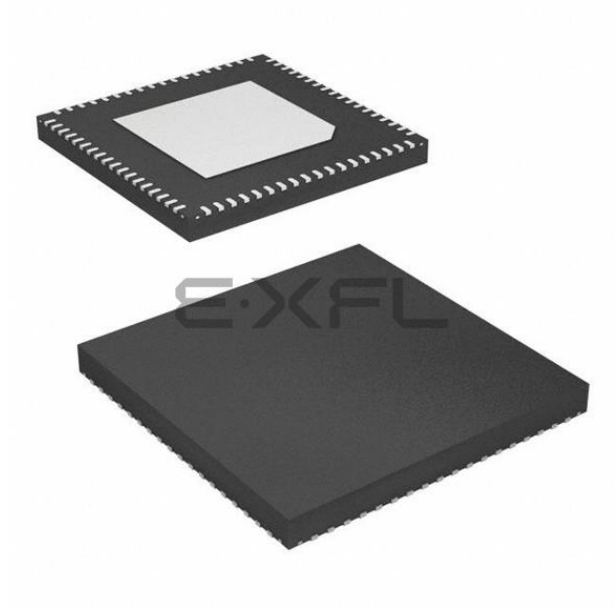

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	294.912MHz
Non-Volatile Memory	ROM (32kB)
On-Chip RAM	64kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	72-VFQFN Exposed Pad, CSP
Supplier Device Package	72-LFCSP-VQ (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1451wbcpz

GENERAL DESCRIPTION

The ADAU1452/ADAU1451/ADAU1450 are automotive qualified audio processors that far exceed the digital signal processing capabilities of earlier SigmaDSP® devices. The restructured hardware architecture is optimized for efficient audio processing. The audio processing algorithms are realized in sample-by-sample and block-by-block paradigms that can both be executed simultaneously in a signal processing flow created using the graphical programming tool, SigmaStudio™. The restructured digital signal processor (DSP) core architecture enables some types of audio processing algorithms to be executed using significantly fewer instructions than were required on previous SigmaDSP generations, leading to vastly improved code efficiency.

The 1.2 V, 32-bit DSP core can run at frequencies of up to 294.912 MHz and execute up to 6144 instructions per sample at the standard sample rate of 48 kHz. However, in addition to industry standard rates, a wide range of sample rates are available. The integer PLL and flexible clock generator hardware can generate up to 15 audio sample rates simultaneously. These clock generators, along with the on board asynchronous sample rate converters (ASRCs) and a flexible hardware audio routing matrix, make the ADAU1452/ADAU1451/ADAU1450 ideal audio hubs that greatly simplify the design of complex multirate audio systems.

The ADAU1452/ADAU1451/ADAU1450 interface with a wide range of ADCs, DACs, digital audio devices, amplifiers, and control circuitry, due to their highly configurable serial ports, S/PDIF interfaces (on the ADAU1452 and ADAU1451), and multipurpose input/output pins. They can also directly interface with PDM output MEMS microphones, thanks to integrated decimation filters specifically designed for that purpose.

Independent slave and master I²C/SPI control ports allow the ADAU1452/ADAU1451/ADAU1450 not only to be programmed and configured by an external master device, but also to act as masters that can program and configure external slave devices directly. This flexibility, combined with self boot functionality, enables the design of standalone systems that do not require any external input to operate.

The power efficient DSP core executes full programs while consuming only a few hundred milliwatts (mW) of power and can run at a maximum program load while consuming less than a watt, even in worst case temperatures exceeding 100°C. This relatively low power consumption and small footprint make the ADAU1452/ADAU1451/ADAU1450 ideal replacements for large, general-purpose DSPs that consume more power at the same processing load.

DIFFERENCES BETWEEN THE ADAU1452, ADAU1451, AND ADAU1450

The three variants of this device are differentiated by memory, DSP core frequency, availability of S/PDIF interfaces, and ASRC configuration. A detailed summary of the differences is listed in Table 1.

Because the ADAU1450 does not contain an S/PDIF receiver or transmitter, the SPDIFIN and SPDIFOUT pins are nonfunctional. Also, the settings of any registers related to the S/PDIF input or output in the ADAU1450 do not have any effect on the operation of the device.

Likewise, because the ADAU1450 does not contain ASRCs, the settings of any registers related to the ASRCs in the ADAU1450 do not have any effect on the operation of the device.

Table 1. Product Selection Table

Device Number	Data Memory (kWords)	Program Memory (kWords)	DSP Core Frequency	S/PDIF Input and Output	ASRC Configuration
ADAU1452	40	8	294.912 MHz	Available	16 channels (8 rates × 2 channels per rate)
ADAU1451	16	8	294.912 MHz	Available	16 channels (8 rates × 2 channels per rate)
ADAU1450	8	8	147.456 MHz	Not available	No ASRCs included

PDM Inputs

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 10% to 3.3 V + 10%. PDM data is latched on both edges of the clock (see Figure 11).

Table 16.

Parameter	t_{MIN}	t_{MAX}	Unit	Description
Timing Requirements				
t_{SETUP}	10		ns	Data setup time
t_{HOLD}	5		ns	Data hold time

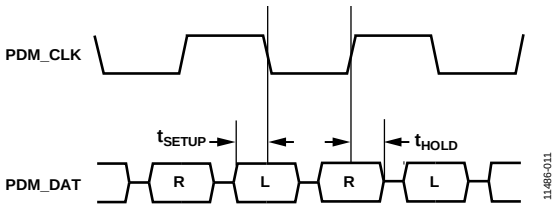
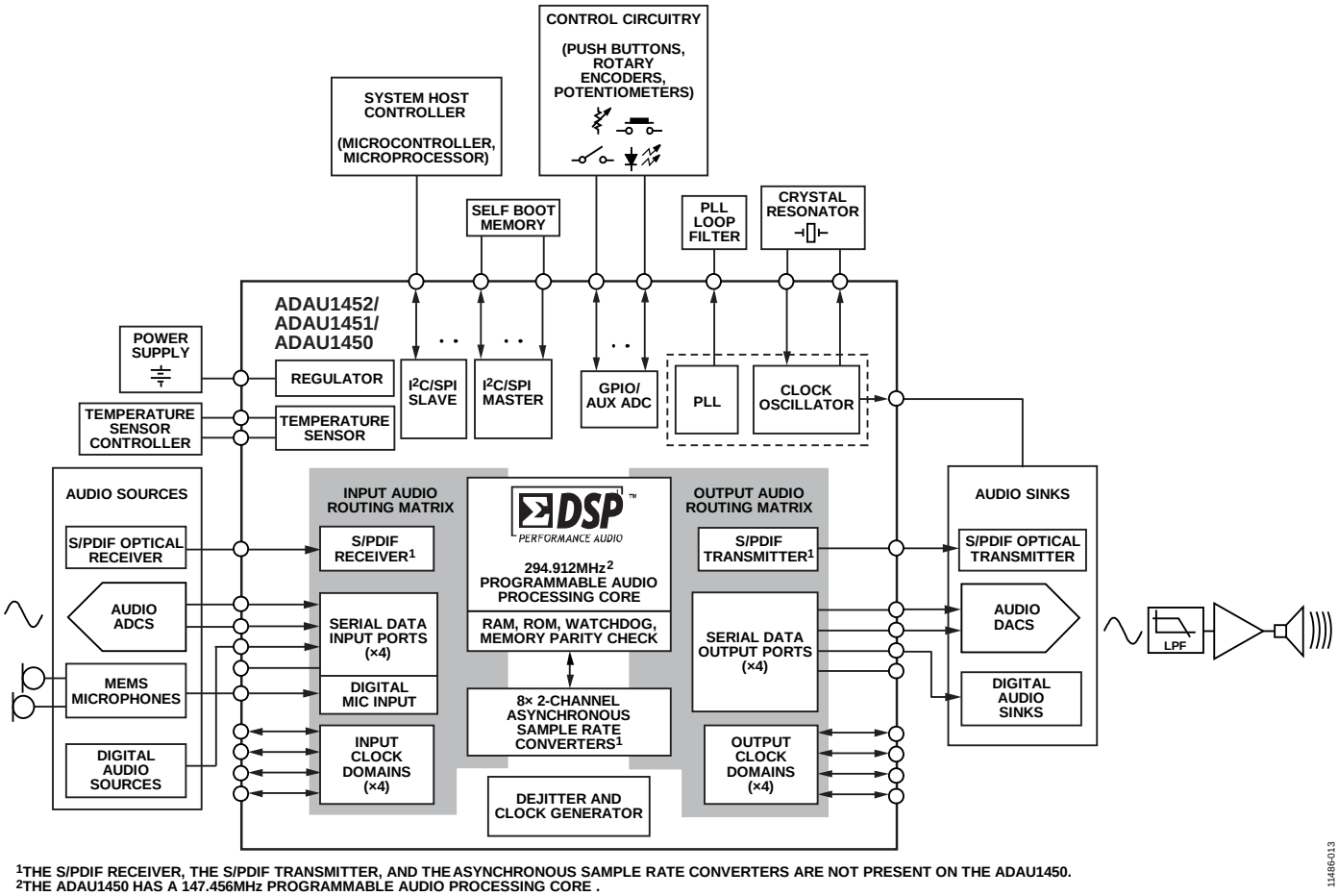


Figure 11. PDM Timing Diagram

THEORY OF OPERATION

SYSTEM BLOCK DIAGRAM



1THE S/PDIF RECEIVER, THE S/PDIF TRANSMITTER, AND THE ASYNCHRONOUS SAMPLE RATE CONVERTERS ARE NOT PRESENT ON THE ADAU1450.
2THE ADAU1450 HAS A 147.456MHz PROGRAMMABLE AUDIO PROCESSING CORE .

Figure 13. System Block Diagram with Example Connections to External Components

OVERVIEW

The ADAU1452/ADAU1451/ADAU1450 are enhanced audio processors with 48 channels of input and output. They include options for the hardware routing of audio signals between the various inputs, outputs, SigmaDSP core, and integrated sample rate converters. The SigmaDSP core features full 32-bit processing (that is, 64-bit processing in double precision mode) with an 80-bit arithmetic logic unit (ALU). By using a quadruple multiply accumulator (MAC) data path, the ADAU1452/ADAU1451 can execute more than 1.2 billion MAC operations per second, which allows for processing power that far exceeds the predecessors in the SigmaDSP family of products. The powerful DSP core can process over 3000 double precision biquad filters or 24,000 FIR filter taps per sample at the standard 48 kHz audio sampling rate. The ADAU1450 features half the processing power of the ADAU1452/ADAU1451. Other features, including synchronous parameter loading for ensuring filter stability and 100% code efficiency with the SigmaStudio tools, reduce complexity in audio system development. The SigmaStudio library of audio processing algorithms allows system designers to compensate for real-world limitations of speakers, amplifiers, and listening environments, through speaker equalization, multiband compression, limiting, and third party branded algorithms.

The input audio routing matrix and output audio routing matrix allow the user to multiplex inputs from multiple sources that are running at various sample rates to or from the SigmaDSP core, and then to pass them on to the desired hardware outputs. This drastically reduces the complexity of signal routing and clocking issues in the audio system. The audio subsystem includes up to eight stereo asynchronous sample rate converters (ASRCs), depending on the device model; Sony/Philips Digital Interconnect Format (S/PDIF) input and output (available on the ADAU1452/ADAU1451); and serial (I^2S) and time division multiplexing (TDM) I/Os. Any of these inputs can be routed to the SigmaDSP core or to any of the ASRCs (except on the ADAU1450, which does not have ASRCs). Similarly, the output signals can be taken from the SigmaDSP core, any of the ASRC outputs, the serial inputs, the PDM microphones, or the S/PDIF receiver. This routing scheme, which can be modified at any time using control registers, allows for maximum system flexibility without requiring hardware design changes.

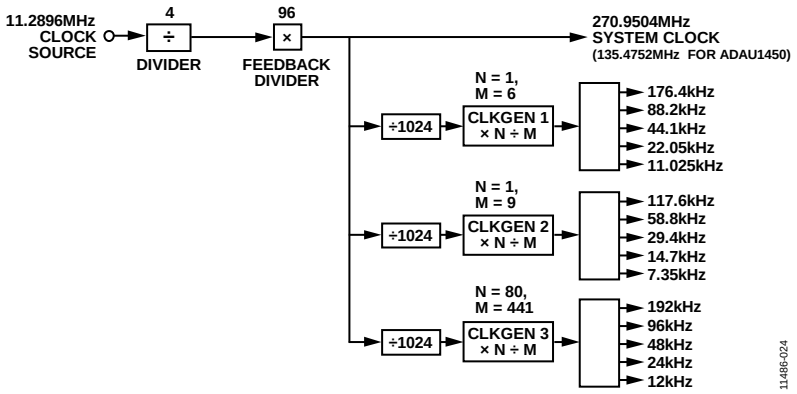


Figure 20. PLL and Audio Clock Generators with Default Settings and Resulting Clock Frequencies Labeled, XTALIN/MCLK = 11.2896 MHz

Figure 20 shows an example where the master clock input has a frequency of 11.2896 MHz, and the default settings are used for the PLL predivider, feedback divider, and Clock Generator 1 and Clock Generator 2. The resulting system clock is

$$11.2896 \text{ MHz} \div 4 \times 96 = 270.9504 \text{ MHz}$$

The base output of Clock Generator 1 is

$$270.9504 \text{ MHz} \div 1024 \times 1 \div 6 = 44.1 \text{ kHz}$$

The base output of Clock Generator 2 is

$$270.9504 \text{ MHz} \div 1024 \times 1 \div 9 = 29.4 \text{ kHz}$$

In this example, Clock Generator 3 is configured with N = 80 and M = 441; therefore, the resulting base output of Clock Generator 3 is

$$270.9504 \text{ MHz} \div 1024 \times 80 \div 441 = 48 \text{ kHz}$$

Master Clock Output

The master clock output pin (CLKOUT) is useful in cases where a master clock must be fed to other ICs in the system, such as audio codecs. The master clock output frequency is determined by the setting of the MCLK_OUT register (Address 0xF005). Four frequencies are possible: 1×, 2×, 4×, or 8× the frequency of the predivider output.

- The predivider output × 1 generates a 3.072 MHz output for a nominal system clock of 294.912 MHz.
- The predivider output × 2 generates a 6.144 MHz output for a nominal system clock of 294.912 MHz.
- The predivider output × 4 generates a 12.288 MHz output for a nominal system clock of 294.912 MHz.
- The predivider output × 8 generates a 24.576 MHz output for a nominal system clock of 294.912 MHz.

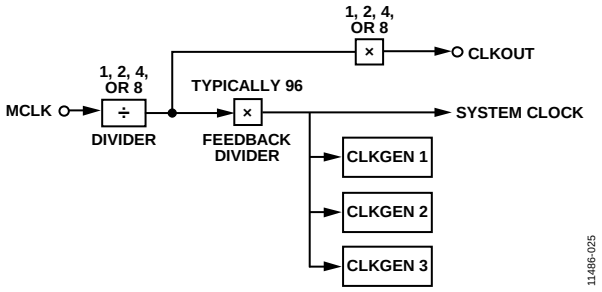


Figure 21. Clock Output Generator

The CLKOUT pin can drive more than one external slave IC if the drive strength is sufficient to drive the traces and external receiver circuitry. The ability to drive external ICs varies greatly, depending on the application and the characteristics of the PCB and the slave ICs. The drive strength and slew rate of the CLKOUT pin is configurable in the CLKOUT_PIN register (Address 0xF7A3); thus, its performance can be tuned to match the specific application. The CLKOUT pin is not designed to drive long cables or other high impedance transmission lines. Use the CLKOUT pin only to drive signals to other integrated circuits on the same PCB. When changing the settings for the predivider, disable and then reenable the PLL using Register 0xF003 (PLL_ENABLE), allowing the frequency of the CLKOUT signal to update.

Dejitter Circuitry

To account for jitter between ICs in the system and to handle interfacing safely between internal and external clocks, de-jitter circuits are included to guarantee that jitter related clocking errors are avoided. The dejitter circuitry is automated and does not require interaction or control from the user.

Auxiliary Output Mode

The received data on the S/PDIF receiver can be converted to a TDM8 stream, bypass the SigmaDSP core, and be output directly on a serial data output pin. This mode of operation is called auxiliary output mode. Configure this mode using Register 0xF608 (SPDIF_AUX_EN). The TDM8 output from the S/PDIF receiver regroups the recovered data in a TDM-like format, as shown in Table 52.

The S/PDIF receiver, when operating in auxiliary output mode, also recovers the embedded BCLK_OUTx and LRCLK_OUTx signals in the S/PDIF stream and outputs them on the corresponding BCLK_OUTx and LRCLK_OUTx pins in master mode when Register 0xF608 (SPDIF_AUX_EN), Bits[3:0] (TDMOUT), are configured to enable auxiliary output mode. The selected BCLK_OUTx signal has a frequency of 256× the recovered sample rate, and the LRCLK_OUTx signal is a 50-50 duty cycle square wave that has the same frequency as the audio sample rate (see Table 130).

Table 52. S/PDIF Auxiliary Output Mode, TDM8 Data Format

TDM8 Channel	Description of Data Format
0	8 zero bits followed by 24 audio bits, recovered from the left audio channel of the S/PDIF stream
1	28 zero bits followed by the left parity bit, left validity bit, left user data, and left channel status
2	30 zero bits followed by the compression type bit (0b0 = AC3, 0b1 = DTS) and the audio type bit (0 = PCM, 1 = compressed)
3	No data
4	8 zero bits followed by 24 audio bits, recovered from the right audio channel of the S/PDIF stream
5	28 zero bits followed by the right parity bit, right validity bit, right user data, and right channel status
6	No data
7	31 zero bits followed by the block start signal

S/PDIF Interface Registers

An overview of the registers related to the S/PDIF interface is shown in Table 53. For a more detailed description, refer to the S/PDIF Interface Registers section.

Table 53. S/PDIF Interface Registers

Address	Register	Description
0xF600	SPDIF_LOCK_DET	S/PDIF receiver lock bit detection
0xF601	SPDIF_RX_CTRL	S/PDIF receiver control
0xF602	SPDIF_RX_DECODE	Decoded signals from the S/PDIF receiver
0xF603	SPDIF_RX_COMPRMODE	Compression mode from the S/PDIF receiver
0xF604	SPDIF_RESTART	Automatically resume S/PDIF receiver audio input
0xF605	SPDIF_LOSS_OF_LOCK	S/PDIF receiver loss of lock detection
0xF608	SPDIF_AUX_EN	S/PDIF receiver auxiliary outputs enable
0xF60F	SPDIF_RX_AUXBIT_READY	S/PDIF receiver auxiliary bits ready flag
0xF610 to 0xF61B	SPDIF_RX_CS_LEFT_x	S/PDIF receiver channel status bits (left)
0xF620 to 0xF62B	SPDIF_RX_CS_RIGHT_x	S/PDIF receiver channel status bits (right)
0xF630 to 0xF63B	SPDIF_RX_UD_LEFT_x	S/PDIF receiver user data bits (left)
0xF640 to 0xF64B	SPDIF_RX_UD_RIGHT_x	S/PDIF receiver user data bits (right)
0xF650 to 0xF65B	SPDIF_RX_VB_LEFT_x	S/PDIF receiver validity bits (left)
0xF660 to 0xF66B	SPDIF_RX_VB_RIGHT_x	S/PDIF receiver validity bits (right)
0xF670 to 0xF67B	SPDIF_RX_PB_LEFT_x	S/PDIF receiver parity bits (left)
0xF680 to 0xF68B	SPDIF_RX_PB_RIGHT_x	S/PDIF receiver parity bits (right)
0xF690	SPDIF_TX_EN	S/PDIF transmitter enable
0xF691	SPDIF_TX_CTRL	S/PDIF transmitter control
0xF69F	SPDIF_TX_AUXBIT_SOURCE	S/PDIF transmitter auxiliary bits source select
0xF6A0 to 0xF6AB	SPDIF_TX_CS_LEFT_x	S/PDIF transmitter channel status bits (left)
0xF6B0 to 0xF6BB	SPDIF_TX_CS_RIGHT_x	S/PDIF transmitter channel status bits (right)
0xF6C0 to 0xF6CB	SPDIF_TX_UD_LEFT_x	S/PDIF transmitter user data bits (left)
0xF6D0 to 0xF6DB	SPDIF_TX_UD_RIGHT_x	S/PDIF transmitter user data bits (right)
0xF6E0 to 0xF6EB	SPDIF_TX_VB_LEFT_x	S/PDIF transmitter validity bits (left)
0xF6F0 to 0xF6FB	SPDIF_TX_VB_RIGHT_x	S/PDIF transmitter validity bits (right)
0xF700 to 0xF70B	SPDIF_TX_PB_LEFT_x	S/PDIF transmitter parity bits (left)
0xF710 to 0xF71B	SPDIF_TX_PB_RIGHT_x	S/PDIF transmitter parity bits (right)

Address	Register Name	Description	Reset	RW
0xF6C9	SPDIF_TX_UD_LEFT_9	S/PDIF transmitter user data bits (left)	0x0000	RW
0xF6CA	SPDIF_TX_UD_LEFT_10	S/PDIF transmitter user data bits (left))	0x0000	RW
0xF6CB	SPDIF_TX_UD_LEFT_11	S/PDIF transmitter user data bits (left)	0x0000	RW
0xF6D0	SPDIF_TX_UD_RIGHT_0	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6D1	SPDIF_TX_UD_RIGHT_1	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6D2	SPDIF_TX_UD_RIGHT_2	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6D3	SPDIF_TX_UD_RIGHT_3	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6D4	SPDIF_TX_UD_RIGHT_4	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6D5	SPDIF_TX_UD_RIGHT_5	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6D6	SPDIF_TX_UD_RIGHT_6	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6D7	SPDIF_TX_UD_RIGHT_7	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6D8	SPDIF_TX_UD_RIGHT_8	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6D9	SPDIF_TX_UD_RIGHT_9	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6DA	SPDIF_TX_UD_RIGHT_10	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6DB	SPDIF_TX_UD_RIGHT_11	S/PDIF transmitter user data bits (right)	0x0000	RW
0xF6E0	SPDIF_TX_VB_LEFT_0	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6E1	SPDIF_TX_VB_LEFT_1	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6E2	SPDIF_TX_VB_LEFT_2	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6E3	SPDIF_TX_VB_LEFT_3	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6E4	SPDIF_TX_VB_LEFT_4	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6E5	SPDIF_TX_VB_LEFT_5	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6E6	SPDIF_TX_VB_LEFT_6	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6E7	SPDIF_TX_VB_LEFT_7	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6E8	SPDIF_TX_VB_LEFT_8	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6E9	SPDIF_TX_VB_LEFT_9	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6EA	SPDIF_TX_VB_LEFT_10	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6EB	SPDIF_TX_VB_LEFT_11	S/PDIF transmitter validity bits (left)	0x0000	RW
0xF6F0	SPDIF_TX_VB_RIGHT_0	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF6F1	SPDIF_TX_VB_RIGHT_1	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF6F2	SPDIF_TX_VB_RIGHT_2	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF6F3	SPDIF_TX_VB_RIGHT_3	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF6F4	SPDIF_TX_VB_RIGHT_4	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF6F5	SPDIF_TX_VB_RIGHT_5	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF6F6	SPDIF_TX_VB_RIGHT_6	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF6F7	SPDIF_TX_VB_RIGHT_7	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF6F8	SPDIF_TX_VB_RIGHT_8	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF6F9	SPDIF_TX_VB_RIGHT_9	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF6FA	SPDIF_TX_VB_RIGHT_10	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF6FB	SPDIF_TX_VB_RIGHT_11	S/PDIF transmitter validity bits (right)	0x0000	RW
0xF700	SPDIF_TX_PB_LEFT_0	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF701	SPDIF_TX_PB_LEFT_1	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF702	SPDIF_TX_PB_LEFT_2	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF703	SPDIF_TX_PB_LEFT_3	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF704	SPDIF_TX_PB_LEFT_4	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF705	SPDIF_TX_PB_LEFT_5	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF706	SPDIF_TX_PB_LEFT_6	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF707	SPDIF_TX_PB_LEFT_7	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF708	SPDIF_TX_PB_LEFT_8	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF709	SPDIF_TX_PB_LEFT_9	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF70A	SPDIF_TX_PB_LEFT_10	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF70B	SPDIF_TX_PB_LEFT_11	S/PDIF transmitter parity bits (left)	0x0000	RW
0xF710	SPDIF_TX_PB_RIGHT_0	S/PDIF transmitter parity bits (right)	0x0000	RW
0xF711	SPDIF_TX_PB_RIGHT_1	S/PDIF transmitter parity bits (right)	0x0000	RW
0xF712	SPDIF_TX_PB_RIGHT_2	S/PDIF transmitter parity bits (right)	0x0000	RW

CONTROL REGISTER DETAILS

PLL CONFIGURATION REGISTERS

PLL Feedback Divider Register

Address: 0xF000, Reset: 0x0060, Name: PLL_CTRL0

This register is the value of the feedback divider in the PLL. This value effectively multiplies the frequency of the input clock to the PLL, creating the output system clock, which clocks the DSP core and other digital circuit blocks. The format of the value stored in this register is binary integer in 7.0 format. For example, the default feedback divider value of 96 is stored as 0x60. The value written to this register does not take effect until Register 0xF003 (PLL_ENABLE), Bit 0 (PLL_ENABLE) changes state from 0b0 to 0b1.

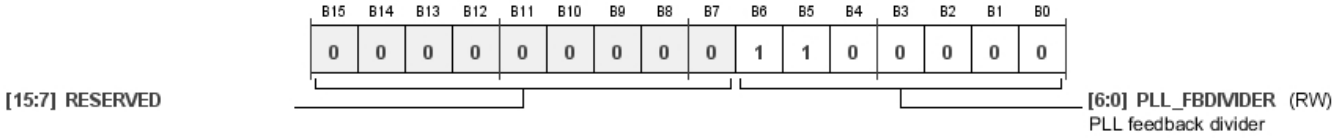


Table 65. Bit Descriptions for PLL_CTRL0

Bits	Bit Name	Settings	Description	Reset	Access
[15:7]	RESERVED			0x0	RW
[6:0]	PLL_FBDIVIDER		PLL feedback divider. This is the value of the feedback divider in the PLL, which effectively multiplies the frequency of the input clock to the PLL, creating the output system clock, which clocks the DSP core and other digital circuit blocks. The format of the value stored in this register is binary integer in 7.0 format. For example, the default feedback divider value of 96 is stored as 0x60.	0x60	RW

PLL Prescale Divider Register

Address: 0xF001, Reset: 0x0000, Name: PLL_CTRL1

This register sets the input prescale divider for the PLL. The value written to this register does not take effect until Register 0xF003 (PLL_ENABLE), Bit 0 (PLL_ENABLE) changes state from 0b0 to 0b1.

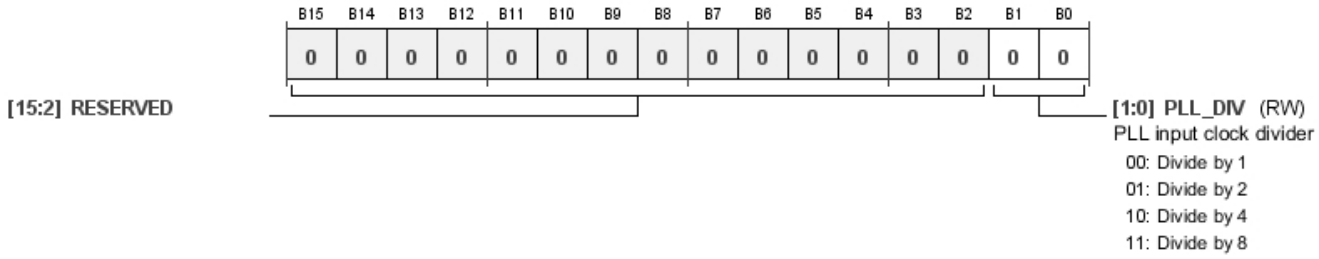


Table 66. Bit Descriptions for PLL_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[15:2]	RESERVED			0x0	RW
[1:0]	PLL_DIV		PLL input clock divider. This prescale clock divider creates the PLL input clock from the externally input master clock. The nominal frequency of the PLL input is 3.072 MHz. Therefore, if the input master clock frequency is 3.072 MHz, set the prescale clock divider to divide by 1. If the input clock is 12.288 MHz, set the prescale clock divider to divide by 4. The goal is to make the input to the PLL as close to 3.072 MHz as possible.	0x0	RW
		00	Divide by 1		
		01	Divide by 2		
		10	Divide by 4		
		11	Divide by 8		

Bits	Bit Name	Settings	Description	Reset	Access
4	CLK_GEN3_SRC		Reference source for Clock Generator 3. This bit selects the reference of Clock Generator 3. If set to use an external reference clock, Bits[3:0] define the source pin. Otherwise, the PLL output is used as the reference clock. When an external reference clock is used for Clock Generator 3, the resulting base output frequency of Clock Generator 3 is the frequency of the input reference clock multiplied by the Clock Generator 3 numerator, divided by 1024. For example: if Bit 4 (CLK_GEN3_SRC) = 0b1 (an external reference clock is used); Bits[3:0] (FREF_PIN) = 0b1110 (the input signal of the S/PDIF receiver is used as the reference source); the sample rate of the S/PDIF input signal = 48 kHz; and the numerator of Clock Generator 3 = 2048; the resulting base output sample rate of Clock Generator 3 is 48 kHz × 2048/1024 = 96 kHz.	0x0	RW
		0	Reference signal provided by PLL output; multiply the frequency of that signal by M and divide it by N		
		1	Reference signal provided by the signal input to the hardware pin defined by Bits[3:0] (FREF_PIN); multiply the frequency of that signal by N (and then divide by 1024) to get the resulting sample rate; M is ignored		
[3:0]	FREF_PIN		Input reference for Clock Generator 3. If Clock Generator 3 is set up to lock to an external reference clock (Bit 4 (CLK_GEN3_SRC) = 0b1), these bits allow the user to specify which pin is receiving the reference clock. The signal input to the corresponding pin should be a 50% duty cycle square wave clock representing the reference sample rate.	0xE	RW
		0000	Input reference source is SS_M/MP0		
		0001	Input reference source is MOSI_M/MP1		
		0010	Input reference source is SCL_M/SCLK_M/MP2		
		0011	Input reference source is SDA_M/MISO_M/MP3		
		0100	Input reference source is LRCLK_OUT0/MP4		
		0101	Input reference source is LRCLK_OUT1/MP5		
		0110	Input reference source is MP6		
		0111	Input reference source is MP7		
		1000	Input reference source is LRCLK_OUT2/MP8		
		1001	Input reference source is LRCLK_OUT3/MP9		
		1010	Input reference source is LRCLK_IN0/MP10		
		1011	Input reference source is LRCLK_IN1/MP11		
		1100	Input reference source is LRCLK_IN2/MP12		
		1101	Input reference source is LRCLK_IN3/MP13		
		1110	Input reference source is S/PDIF receiver (recovered frame clock)		

Lock Bit for Clock Generator 3 Input Reference Register

Address: 0xF027, Reset: 0x0000, Name: CLK_GEN3_LOCK

This register monitors whether or not Clock Generator 3 has locked to its reference clock source, regardless of whether it is coming from the PLL output or from an external reference signal, which is configured in Register 0xF026, Bit 4 (CLK_GEN3_SRC).

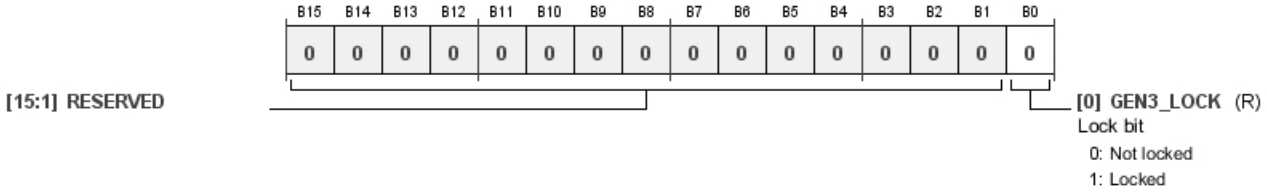


Table 79. Bit Descriptions for CLK_GEN3_LOCK

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	GEN3_LOCK		Lock bit.	0x0	R
		0	Not locked		
		1	Locked		

Bits	Bit Name	Settings	Description	Reset	Access
10	CLK_GEN1_PWR		Clock Generator 1 power enable. When this bit is disabled, Clock Generator 1 is disabled and ceases to output audio clocks. Any LRCLK_OUTx, LRCLK_INx or BCLK_OUTx, BCLK_INx pins that are configured to output clocks generated by Clock Generator 1 output a logic low signal while Clock Generator 1 is disabled. Any functional block in hardware, including the DSP core, that is configured to be clocked by Clock Generator 1 ceases to function when this bit is disabled.	0x0	RW
		0	Power disabled		
		1	Power enabled		
9	ASRCBANK1_PWR		ASRC 4, ASRC 5, ASRC 6, ASRC 7 power enable. When this bit is disabled, ASRC Channel 8 to Channel 15 are disabled, and their output data streams cease.	0x0	RW
		0	Power disabled		
		1	Power enabled		
8	ASRCBANK0_PWR		ASRC 0, ASRC 1, ASRC 2, ASRC 3 power enable. When this bit is disabled, ASRC Channel 0 to Channel 7 are disabled, and their output data streams cease.	0x0	RW
		0	Power disabled		
		1	Power enabled		
7	SOUT3_PWR		SDATA_OUT3 power enable. When this bit is disabled, the SDATA_OUT3 pin and associated serial port circuitry are also disabled. LRCLK_OUT3 and BCLK_OUT3 are not affected.	0x0	RW
		0	Power disabled		
		1	Power enabled		
6	SOUT2_PWR		SDATA_OUT2 power enable. When this bit is disabled, the SDATA_OUT2 pin and associated serial port circuitry is disabled. LRCLK_OUT2 and BCLK_OUT2 are not affected.	0x0	RW
		0	Power disabled		
		1	Power enabled		
5	SOUT1_PWR		SDATA_OUT1 power enable. When this bit is disabled, the SDATA_OUT1 pin and associated serial port circuitry are also disabled. LRCLK_OUT1 and BCLK_OUT1 are not affected.	0x0	RW
		0	Power disabled		
		1	Power enabled		
4	SOUT0_PWR		SDATA_OUT0 power enable. When this bit is disabled, the SDATA_OUT0 pin and associated serial port circuitry are disabled. LRCLK_OUT0 and BCLK_OUT0 are not affected.	0x0	RW
		0	Power disabled		
		1	Power enabled		
3	SIN3_PWR		SDATA_IN3 power enable. When this bit is disabled, the SDATA_IN3 pin and associated serial port circuitry are disabled. LRCLK_IN3 and BCLK_IN3 are not affected.	0x0	RW
		0	Power disabled		
		1	Power enabled		
2	SIN2_PWR		SDATA_IN2 power enable. When this bit is disabled, the SDATA_IN2 pin and associated serial port circuitry are disabled. LRCLK_IN2 and BCLK_IN2 are not affected.	0x0	RW
		0	Power disabled		
		1	Power enabled		
1	SIN1_PWR		SDATA_IN1 power enable. When this bit is disabled, the SDATA_IN1 pin and associated serial port circuitry are disabled. The LRCLK_IN1 and BCLK_IN1 pins are not affected.	0x0	RW
		0	Power disabled		
		1	Power enabled		
0	SIN0_PWR		SDATA_IN0 power enable. When this bit is disabled, the SDATA_IN0 pin and associated serial port circuitry are disabled. The LRCLK_IN0 and BCLK_IN0 pins are not affected.	0x0	RW
		0	Power disabled		
		1	Power enabled		

SERIAL PORT CONFIGURATION REGISTERS

Serial Port Control 0 Register

Address: 0xF200 to 0xF21C (Increments of 0x4), Reset: 0x0000, Name: SERIAL_BYTE_x_0

These eight registers configure several settings for the corresponding serial input and serial output ports. Channel count, MSB position, data-word length, clock polarity, clock sources, and clock type are configured using these registers. On the input side, Register 0xF200 (SERIAL_BYTE_0_0) corresponds to SDATA_IN0; Register 0xF204 (SERIAL_BYTE_1_0) corresponds to SDATA_IN1; Register 0xF208 (SERIAL_BYTE_2_0) corresponds to SDATA_IN2; and Register 0xF20C (SERIAL_BYTE_3_0) corresponds to SDATA_IN3. On the output side, Register 0xF210 (SERIAL_BYTE_4_0) corresponds to SDATA_OUT0; Register 0xF214 (SERIAL_BYTE_5_0) corresponds to SDATA_OUT1; Register 0xF218 (SERIAL_BYTE_6_0) corresponds to SDATA_OUT2; and Register 0xF21C (SERIAL_BYTE_7_0) corresponds to SDATA_OUT3.

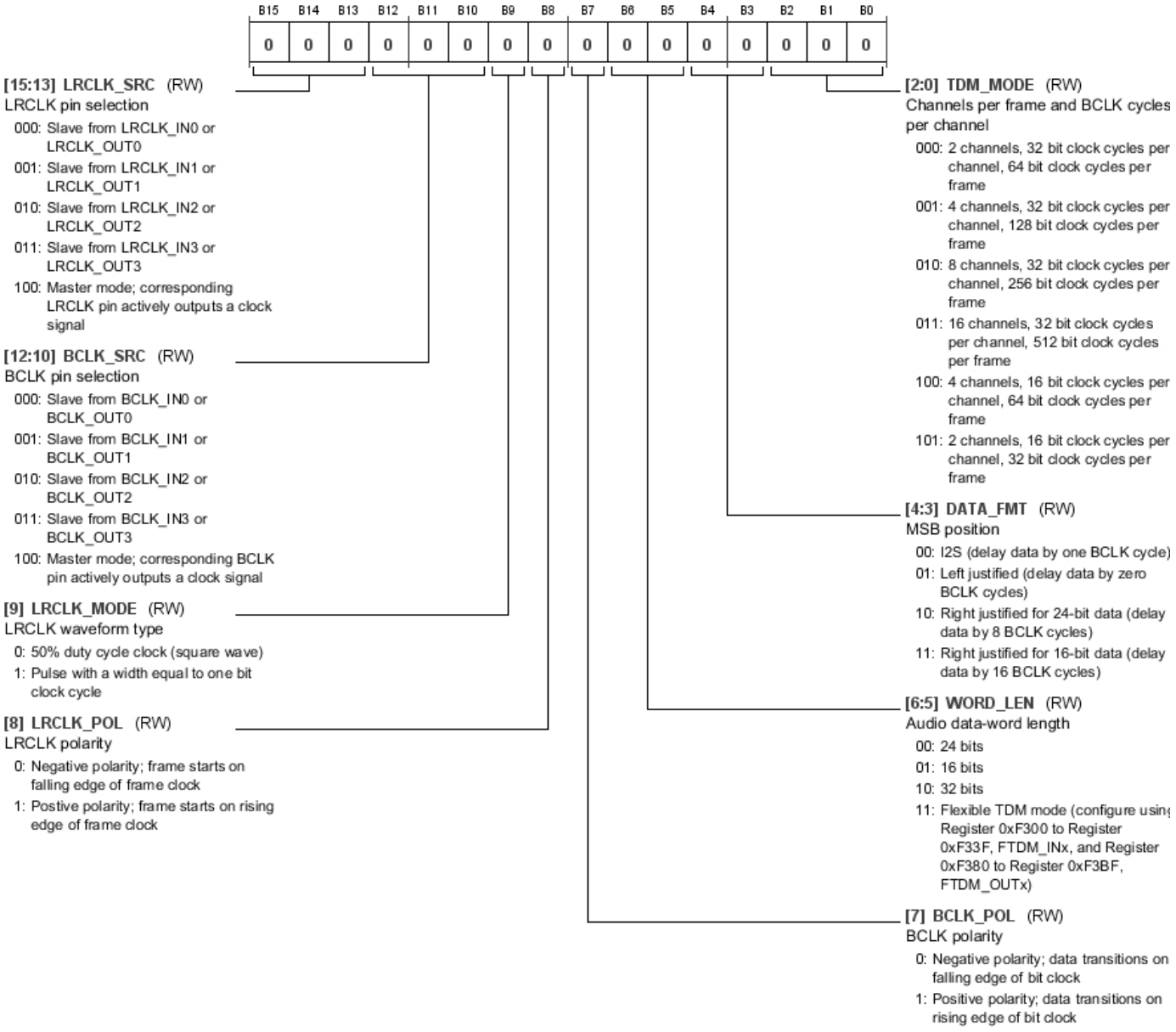


Table 86. Bit Descriptions for SERIAL_BYTE_x_0

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	LRCLK_SRC		LRCLK pin selection. These bits configure whether the corresponding serial port is a frame clock master or slave. When configured as a master, the corresponding LRCLK pin (LRCLK_INx for SDATA_IN pins and LRCLK_OUTx for SDATA_OUT pins) with the same number as the serial port (for example, LRCLK_OUT0 for SDATA_OUT0) actively drives out a clock signal. When configured as a slave, the serial port can receive its clock signal from any of the four corresponding LRCLK pins (LRCLK_INx pins for SDATA_INx pins or LRCLK_OUTx pins for SDATA_OUTx pins).	0x0	RW
		000	Slave from LRCLK_IN0 or LRCLK_OUT0		
		001	Slave from LRCLK_IN1 or LRCLK_OUT1		
		010	Slave from LRCLK_IN2 or LRCLK_OUT2		
		011	Slave from LRCLK_IN3 or LRCLK_OUT3		
		100	Master mode; corresponding LRCLK pin actively outputs a clock signal		
[12:10]	BCLK_SRC		BCLK pin selection. These bits configure whether the corresponding serial port is a bit clock master or slave. When configured as a master, the corresponding BCLK pin (BCLK_INx for SDATA_INx pins and BCLK_OUTx for SDATA_OUTx pins) with the same number as the serial port (for example, BCLK_OUT0 for SDATA_OUT0) actively drives out a clock signal. When configured as a slave, the serial port can receive its clock signal from any of the four corresponding BCLK pins (BCLK_INx pins for SDATA_INx pins or BCLK_OUTx pins for SDATA_OUTx pins).	0x0	RW
		000	Slave from BCLK_IN0 or BCLK_OUT0		
		001	Slave from BCLK_IN1 or BCLK_OUT1		
		010	Slave from BCLK_IN2 or BCLK_OUT2		
		011	Slave from BCLK_IN3 or BCLK_OUT3		
		100	Master mode; corresponding BCLK pin actively outputs a clock signal		
9	LRCLK_MODE		LRCLK waveform type. The frame clock can be a 50/50 duty cycle square wave or a short pulse.	0x0	RW
		0	50% duty cycle clock (square wave)		
		1	Pulse with a width equal to one bit clock cycle		
8	LRCLK_POL		LRCLK polarity. This bit sets the frame clock polarity on the corresponding serial port. Negative polarity means that the frame starts on the falling edge of the frame clock. This conforms to the I²S standard audio format.	0x0	RW
		0	Negative polarity; frame starts on falling edge of frame clock		
		1	Positive polarity; frame starts on rising edge of frame clock		
7	BCLK_POL		BCLK polarity. This bit sets the bit clock polarity on the corresponding serial port. Negative polarity means that the data signal transitions on the falling edge of the bit clock. This conforms to the I²S standard audio format.	0x0	RW
		0	Negative polarity; data transitions on falling edge of bit clock		
		1	Positive polarity; data transitions on rising edge of bit clock		
[6:5]	WORD_LEN		Audio data-word length. These bits set the word length of the audio data channels on the corresponding serial port. For serial input ports, if the input data has more words than the length as configured by these bits, the extra data bits are ignored. For output serial ports, if the word length, as configured by these bits, is shorter than the data length coming from the data source (the DSP, ASRCs, S/PDIF receiver, PDM inputs, or serial inputs), the extra data bits are truncated and output as 0s. If Bits[6:5] (WORD_LEN) are set to 0b10 for 32-bit mode, the corresponding 32-bit input or output cells are required in SigmaStudio.	0x0	RW
		00	24 bits		
		01	16 bits		
		10	32 bits		
		11	Flexible TDM mode (configure using Register 0xF300 to Register 0xF33F, FTDM_INx, and Register 0xF380 to Register 0xF3BF, FTDM_OUTx)		

Bits	Bit Name	Settings	Description	Reset	Access
[4:3]	DATA_FMT		MSB position. These bits set the positioning of the data in the frame on the corresponding serial port.	0x0	RW
		00	I²S (delay data by one BCLK cycle)		
		01	Left justified (delay data by zero BCLK cycles)		
		10	Right justified for 24-bit data (delay data by 8 BCLK cycles)		
		11	Right justified for 16-bit data (delay data by 16 BCLK cycles)		
[2:0]	TDM_MODE		Channels per frame and BCLK cycles per channel. These bits set the number of channels per frame and the number of bit clock cycles per frame on the corresponding serial port.	0x0	RW
		000	2 channels, 32 bit clock cycles per channel, 64 bit clock cycles per frame		
		001	4 channels, 32 bit clock cycles per channel, 128 bit clock cycles per frame		
		010	8 channels, 32 bit clock cycles per channel, 256 bit clock cycles per frame		
		011	16 channels, 32 bit clock cycles per channel, 512 bit clock cycles per frame		
		100	4 channels, 16 bit clock cycles per channel, 64 bit clock cycles per frame		
		101	2 channels, 16 bit clock cycles per channel, 32 bit clock cycles per frame		

Serial Port Control 1 Register

Address: 0xF201 to 0xF21D (Increments of 0x4), Reset: 0x0002, Name: SERIAL_BYTE_x_1

These eight registers configure several settings for the corresponding serial input and serial output ports. Clock generator, sample rate, and behavior during inactive channels are configured with these registers. On the input side, Register 0xF201 (SERIAL_BYTE_0_1) corresponds to SDATA_IN0; Register 0xF205 (SERIAL_BYTE_1_1) corresponds to SDATA_IN1; Register 0xF209 (SERIAL_BYTE_2_1) corresponds to SDATA_IN2; and Register 0xF20D (SERIAL_BYTE_3_1) corresponds to SDATA_IN3. On the output side, Register 0xF211 (SERIAL_BYTE_4_1) corresponds to SDATA_OUT0; Register 0xF215 (SERIAL_BYTE_5_1) corresponds to SDATA_OUT1; Register 0xF219 (SERIAL_BYTE_6_1) corresponds to SDATA_OUT2; and Register 0xF21D (SERIAL_BYTE_7_1) corresponds to SDATA_OUT3.

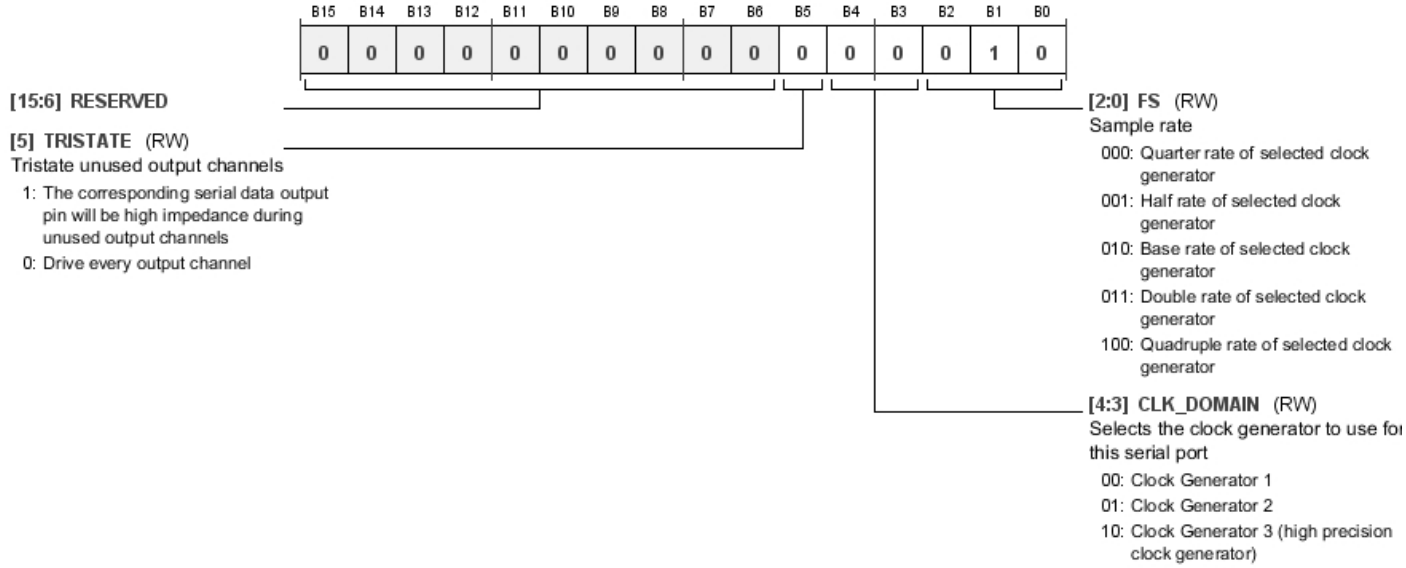


Table 87. Bit Descriptions for SERIAL_BYTE_x_1

Bits	Bit Name	Settings	Description	Reset	Access
[15:6]	RESERVED			0x000	RW
5	TRISTATE		Tristate unused output channels. This bit has no effect on serial input ports.	0x0	RW
		1	The corresponding serial data output pin is high impedance during unused output channels		
		0	Drive every output channel		

DSP CORE CONTROL REGISTERS

Hibernate Setting Register

Address: 0xF400, Reset: 0x0000, Name: HIBERNATE

When hibernation mode is activated, the DSP core continues processing the current audio sample or block, and then enters a low power hibernation state. If Bit 0 (HIBERNATE) is set to 0b1 when the DSP core is processing audio, wait at least the duration of one sample before attempting to modify any other control registers. If Bit 0 (HIBERNATE) is set to 0b1 when the DSP core is processing audio, and block processing is used in the signal flow, wait at least the duration of one block plus the duration of one sample before attempting to modify any other control registers. During hibernation, interrupts to the core are disabled. This prevents audio from flowing into or out of the DSP core. Because DSP processing ceases when hibernation is active, there is a significant drop in the current consumption on the DVDD supply.

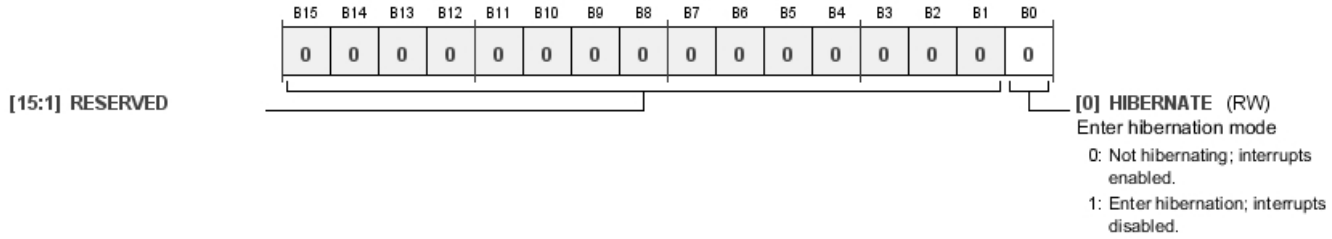


Table 90. Bit Descriptions for Hibernate

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	HIBERNATE		Enter hibernation mode. This bit disables incoming interrupts and tells the DSP core to go to a low power sleep mode after the next audio sample or block has finished processing. It causes the DSP to enter hibernation mode by masking all interrupts.	0x0	RW
		0	Not hibernating; interrupts enabled.		
		1	Enter hibernation; interrupts disabled.		

Panic Mask 3 Register

Address: 0xF426, Reset: 0x0000, Name: PANIC_LOOP_MASK

The panic manager checks and reports software errors related to looping code sections. Register 0xF426 (PANIC_LOOP_MASK) allows the user to configure whether loop errors are reported to the panic manager or ignored.

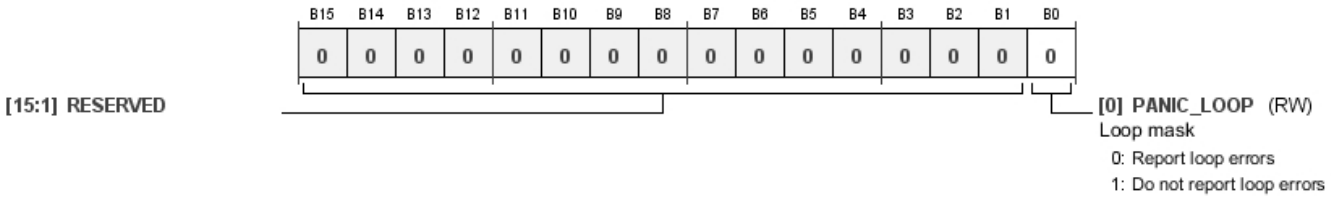


Table 101. Bit Descriptions for PANIC_LOOP_MASK

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	PANIC_LOOP		Loop mask.	0x0	RW
		0	Report loop errors		
		1	Do not report loop errors		

Panic Flag Register

Address: 0xF427, Reset: 0x0000, Name: PANIC_FLAG

This register acts as the master error flag for the panic manager. If any error is encountered in any functional block whose panic manager mask is disabled, this register logs that an error has occurred. Individual functional block masks are configured using Register 0xF422 (PANIC_PARITY_MASK), Register 0xF423 (PANIC_SOFTWARE_MASK), Register 0xF424 (PANIC_WD_MASK), Register 0xF425 (PANIC_STACK_MASK), and Register 0xF426 (PANIC_LOOP_MASK).

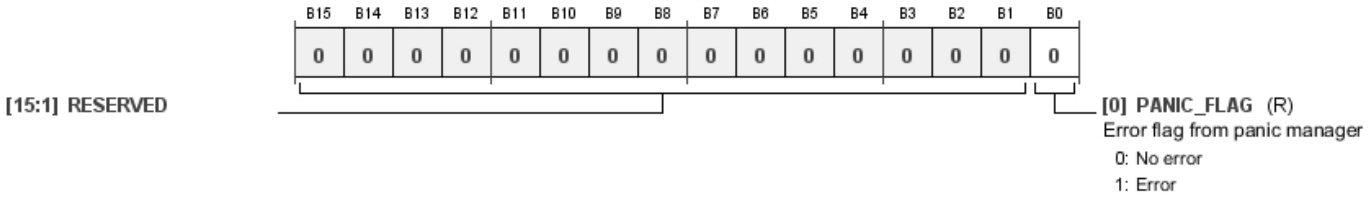


Table 102. Bit Descriptions for PANIC_FLAG

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	PANIC_FLAG		Error flag from panic manager. This error flag bit is sticky. When an error is reported, this bit goes high, and it stays high until the user resets it using Register 0xF421 (PANIC_CLEAR).	0x0	R
		0	No error		
		1	Error		

Watchdog Maximum Count Register

Address: 0xF443, Reset: 0x0000, Name: WATCHDOG_MAXCOUNT

This register is designed to start counting at a specified number and decrement by 1 for each clock cycle of the system clock in the core. The counter is reset to the maximum value each time the program counter jumps to the beginning of the program to begin processing another audio frame (this is implemented in the DSP program code generated by SigmaStudio). If the counter reaches 0, a watchdog error flag is raised in the panic manager. The watchdog is typically set to begin counting from a number slightly larger than the maximum number of instructions expected to execute in the program, such that an error occurs if the program does not finish in time for the next incoming sample.

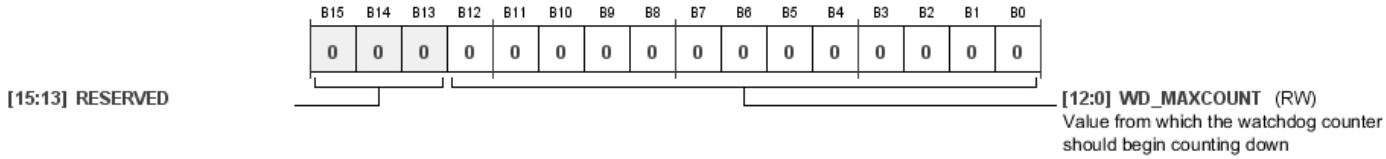


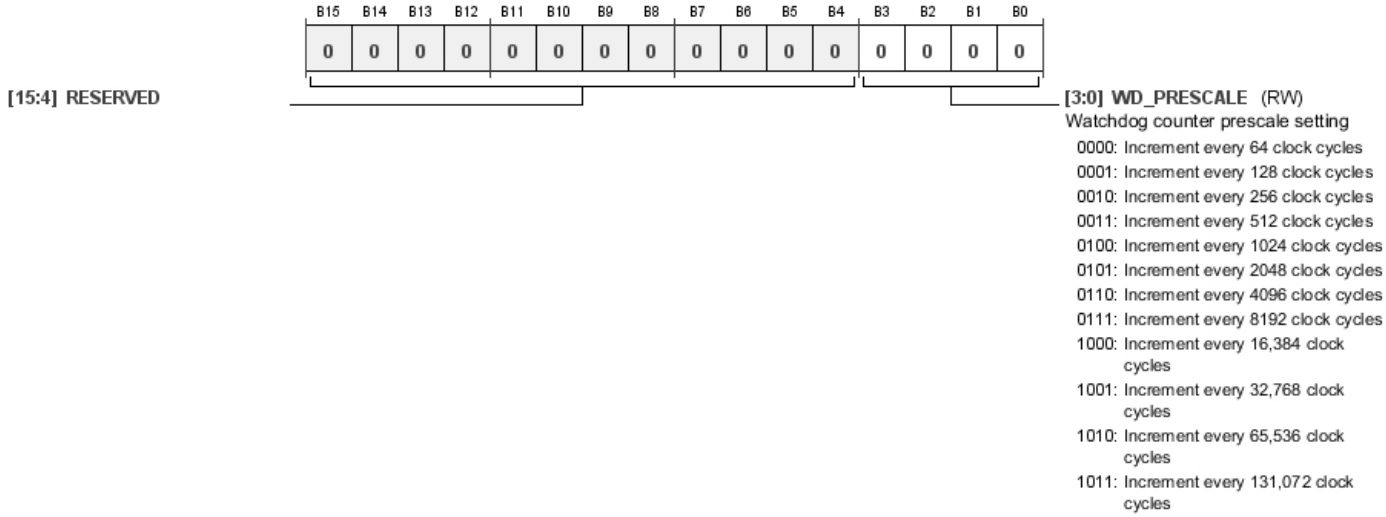
Table 105. Bit Descriptions for WATCHDOG_MAXCOUNT

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED			0x0	RW
[12:0]	WD_MAXCOUNT		Value from which the watchdog counter should begin counting down.	0x0000	RW

Watchdog Prescale Register

Address: 0xF444, Reset: 0x0000, Name: WATCHDOG_PRESCALE

The watchdog prescaler is a number that is multiplied by the setting in Register 0xF443 (WATCHDOG_MAXCOUNT) to achieve very large counts for the watchdog, if necessary. Using the largest prescale factor of 128 × 1024 and the largest watchdog maximum count of 64 × 1024, a very large watchdog counter, on the order of 8.5 billion clock cycles, can be achieved.



Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DEBOUNCE_VALUE		Debounce circuit setting. These bits configure the duration of the debounce circuitry when the corresponding pin is configured as an input (Bits[3:1] (MP_MODE) = 0b000).	0x0	RW
		0001	0.3 ms debounce		
		0010	0.6 ms debounce		
		0011	0.9 ms debounce		
		0100	5.0 ms debounce		
		0101	10.0 ms debounce		
		0110	20.0 ms debounce		
		0111	40.0 ms debounce		
		0000	No debounce		
[3:1]	MP_MODE		Pin mode (when multipurpose function is enabled). These bits select the function of the corresponding pin if it is enabled in multipurpose mode (Bit 0 (MP_ENABLE) = 0b1).	0x0	RW
		000	General-purpose digital input		
		001	General-purpose input, driven by control port; sends its value to the DSP core, but that value can be overwritten by a direct register write		
		010	General-purpose output with pull-up		
		011	General-purpose output without pull-up		
		100	PDM microphone data input		
		101	Panic manager error flag output		
		110	Slave select line for the master SPI port		
0	MP_ENABLE		Function selection (multipurpose or clock/control). This bit selects whether the corresponding pin is used as a multipurpose pin or as its primary function (which could be either an audio clock or control bus pin).	0x0	RW
		0	Audio clock or control port function enabled; the settings of the MPx_MODE, MPx_WRITE, and MPx_READ registers are ignored		
		1	Multipurpose function enabled		

Multipurpose Pin Write Value Register

Address: 0xF520 to 0xF52D (Increments of 0x1), Reset: 0x0000, Name: MPx_WRITE

If a multipurpose pin is configured as an output driven by the control port (the corresponding Bits[3:1] (MP_MODE) = 0b001), the value that is output from the DSP core can be configured by directly writing to these registers.

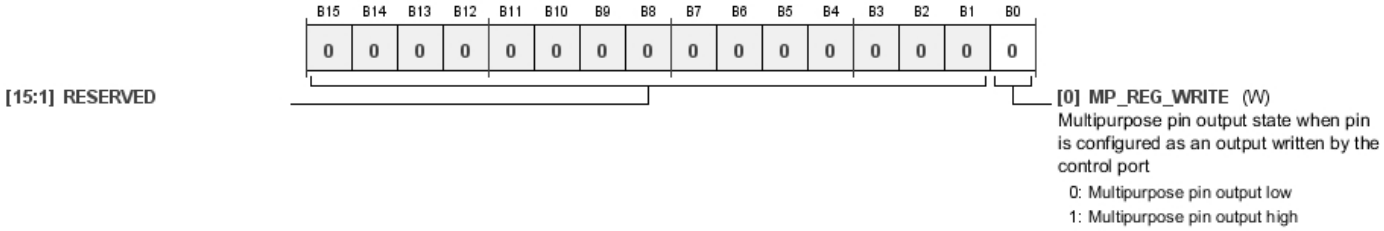


Table 117. Bit Descriptions for MPx_WRITE

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	W
0	MP_REG_WRITE		Multipurpose pin output state when pin is configured as an output written by the control port. This register configures the value seen by the DSP core for the corresponding multipurpose pin input. The pin can have two states: logic low (off) or logic high (on).	0x0	W
		0	Multipurpose pin output low		
		1	Multipurpose pin output high		

Bits	Bit Name	Settings	Description	Reset	Access
10	LOCKMUTE		Mutes ASRCs when lock is lost. When this bit is enabled, individual stereo ASRCs automatically mute on the event that lock status is lost (for example, if the sample rate of the input suddenly changes and the ASRC needs to reattain lock), provided that the corresponding ASRC_RAMPx bit is set to 0b0 (enabled). This automatic mute uses a volume ramp instead of an instantaneous mute to avoid click-and-pop noises on the output. When lock status is attained again (and the corresponding ASRC_RAMPx and ASRCxM bits are set to 0b0 (enabled) and 0b0 (unmuted), respectively), the ASRC automatically unmutes using a volume ramp. However, because there is a period of uncertainty when the ASRC is attaining lock, there still may be noise on the ASRC outputs when the input signal returns. Measures must be taken in the DSP program to delay the unmuting of the ASRC output signals if this noise is not desired. The individual ASRCxM mute bits override the automatic LOCKMUTE behavior.	0x0	RW
		0	Do not mute when lock is lost		
		1	Mute when lock is lost, and unmute when lock is reattained		
9	ASRC_RAMP1		ASRC 7 to ASRC 4 mute disable. ASRC 7 to ASRC 4 (Channel 15 to Channel 8) are defined as ASRC Block 1. This bit enables or disables mute ramping for all ASRCs in Block 1. If this bit is 0b1, Bit 7 (ASRC7M), Bit 6 (ASRC6M), Bit 5 (ASRC5M), and Bit 4 (ASRC4M) are ignored, and the outputs of ASRC 7 to ASRC 4 are active at all times.	0x0	RW
		0	Enabled		
		1	Disabled; ASRC 7 to ASRC 4 never mute automatically and cannot be muted manually		
8	ASRC_RAMP0		ASRC 3 to ASRC 0 mute disable. ASRC 3 to ASRC 0 (Channel 7 to Channel 0) are defined as ASRC Block 0. This bit enables or disables mute ramping for all ASRCs in Block 0. If this bit is 0b1, Bit 3 (ASRC3M), Bit 2 (ASRC2M), Bit 1 (ASRC1M), and Bit 0 (ASRC0M) are ignored, and the outputs of ASRC 3 to ASRC 0 are active at all times.	0x0	RW
		0	Enabled		
		1	Disabled; ASRC 3 to ASRC 0 never mute automatically and cannot be muted manually		
7	ASRC7M		ASRC 7 manual mute.	0x0	RW
		0	Not muted		
		1	Muted		
6	ASRC6M		ASRC 6 manual mute.	0x0	RW
		0	Not muted		
		1	Muted		
5	ASRC5M		ASRC 5 manual mute.	0x0	RW
		0	Not muted		
		1	Muted		
4	ASRC4M		ASRC 4 manual mute.	0x0	RW
		0	Not muted		
		1	Muted		
3	ASRC3M		ASRC 3 manual mute.	0x0	RW
		0	Not muted		
		1	Muted		
2	ASRC2M		ASRC 2 manual mute.	0x0	RW
		0	Not muted		
		1	Muted		
1	ASRC1M		ASRC 1 manual mute.	0x0	RW
		0	Not muted		
		1	Muted		
0	ASRC0M		ASRC 0 manual mute.	0x0	RW
		0	Not muted		
		1	Muted		

S/PDIF Transmitter Validity Bits (Right) Register

Address: 0xF6F0 to 0xF6FB (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_VB_RIGHT_x

These 12 registers allow the 192 validity bits encoded on the right channel of the output data stream of the S/PDIF transmitter on the ADAU1452 and ADAU1451 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

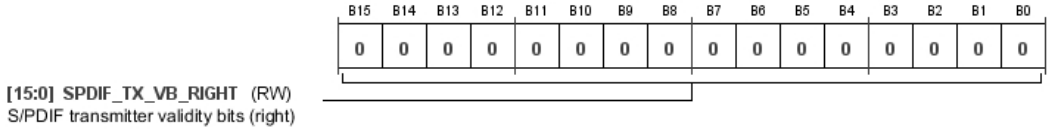


Table 148. Bit Descriptions for SPDIF_TX_VB_RIGHT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_VB_RIGHT		S/PDIF transmitter validity bits (right).	0x0000	RW

S/PDIF Transmitter Parity Bits (Left) Register

Address: 0xF700 to Address 0xF70B (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_PB_LEFT_x

These 12 registers allow the 192 parity bits encoded on the left channel of the output data stream of the S/PDIF transmitter on the ADAU1452 and ADAU1451 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

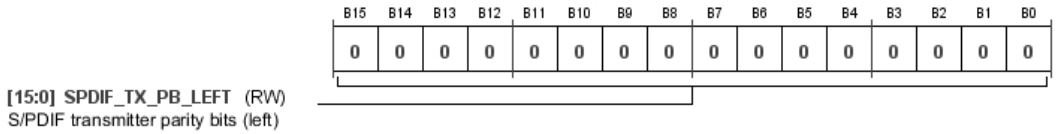


Table 149. Bit Descriptions for SPDIF_TX_PB_LEFT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_PB_LEFT		S/PDIF transmitter parity bits (left).	0x0000	RW

S/PDIF Transmitter Parity Bits (Right) Register

Address: 0xF710 to Address 0xF71B (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_PB_RIGHT_x

These 12 registers allow the 192 parity bits encoded on the right channel of the output data stream of the S/PDIF transmitter on the ADAU1452 and ADAU1451 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

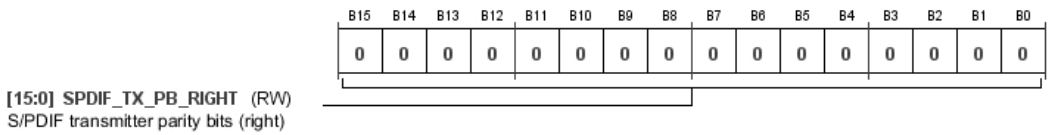


Table 150. Bit Descriptions for SPDIF_TX_PB_RIGHT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_PB_RIGHT		S/PDIF transmitter parity bits (right).	0x0000	RW

MP7 Pin Drive Strength and Slew Rate Register

Address: 0xF7A2, Reset: 0x0018, Name: MP7_PIN

This register configures the drive strength, slew rate, and pull resistors for the MP7 pin.

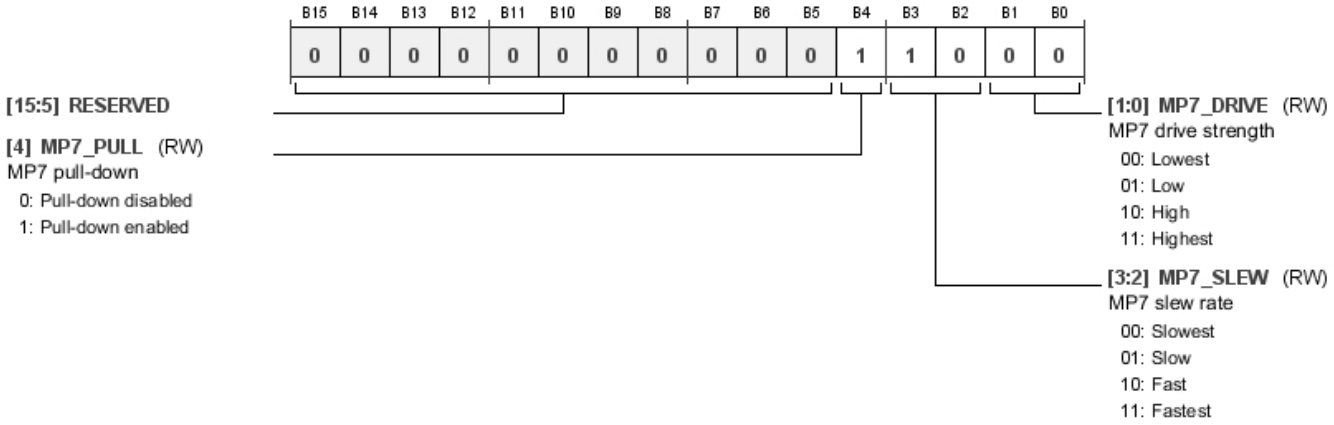
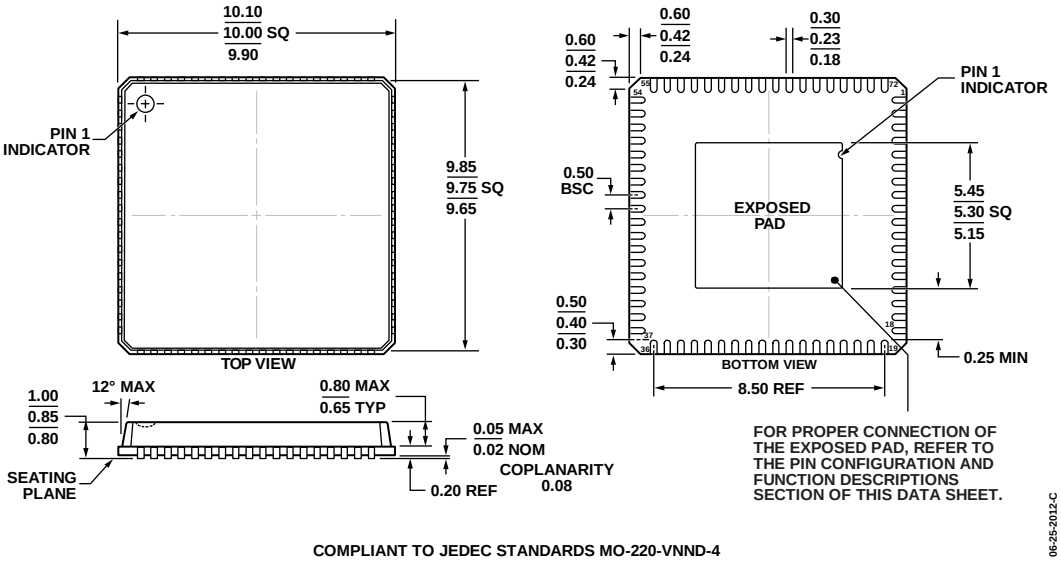


Table 167. Bit Descriptions for MP7_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	MP7_PULL		MP7 pull-down.	0x1	RW
		0	Pull-down disabled		
		1	Pull-down enabled		
[3:2]	MP7_SLEW		MP7 slew rate.	0x2	RW
		00	Slowest		
		01	Slow		
		10	Fast		
		11	Fastest		
[1:0]	MP7_DRIVE		MP7 drive strength.	0x0	RW
		00	Lowest		
		01	Low		
		10	High		
		11	Highest		

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VNND-4

Figure 91. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-72-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADAU1452WBCPZ	−40°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-6
ADAU1452WBCPZ-RL	−40°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 13" Tape and Reel	CP-72-6
ADAU1451WBCPZ	−40°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-6
ADAU1451WBCPZ-RL	−40°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 13" Tape and Reel	CP-72-6
ADAU1450WBCPZ	−40°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-6
ADAU1450WBCPZ-RL	−40°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 13" Tape and Reel	CP-72-6
EVAL-ADAU1452Z		Evaluation Board	
EVAL-ADAU1452MINIZ		Evaluation Board	

[1] Z = RoHS compliant part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADAU1452W/ADAU1451W/ADAU1450W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).