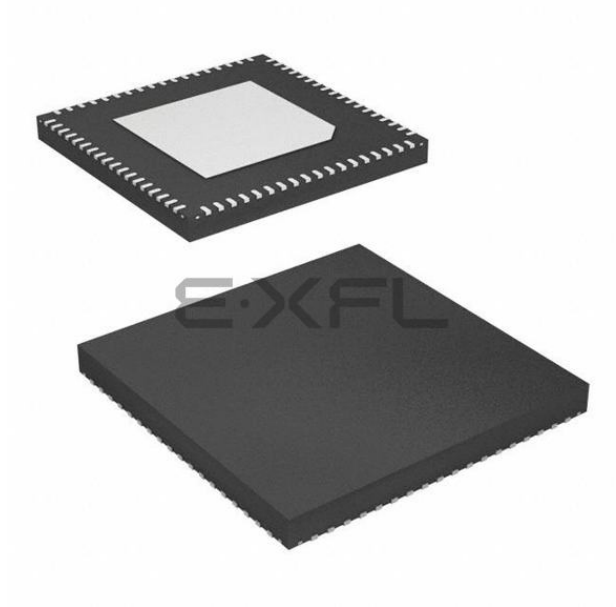

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	294.912MHz
Non-Volatile Memory	ROM (32kB)
On-Chip RAM	160kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	72-VFQFN Exposed Pad, CSP
Supplier Device Package	72-LFCSP-VQ (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1452wbcpz

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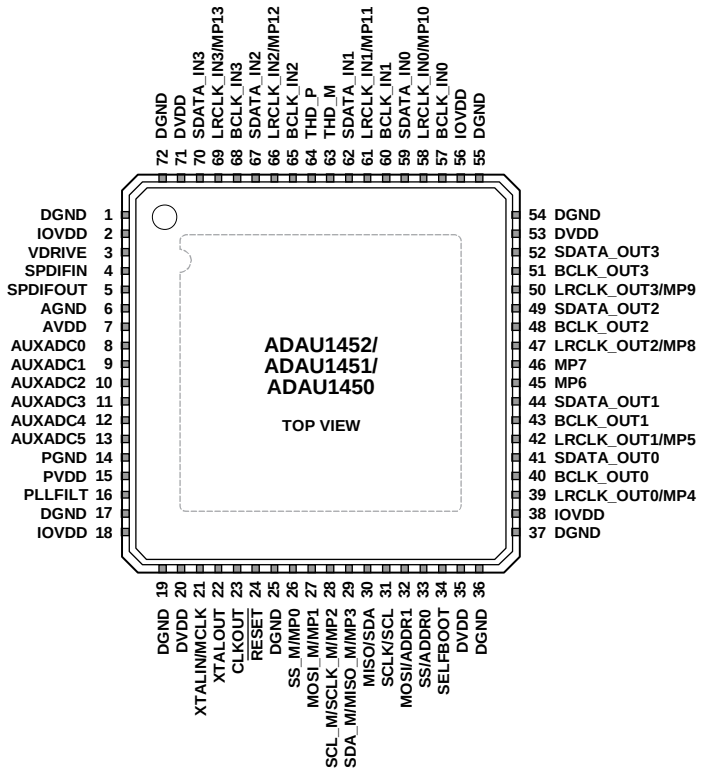
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE GROUNDED BY SOLDERING IT TO A COPPER SQUARE OF EQUIVALENT SIZE ON THE PCB. IDENTICAL COPPER SQUARES MUST EXIST ON ALL LAYERS OF THE BOARD, CONNECTED BY VIAS, AND THEY MUST BE CONNECTED TO A DEDICATED COPPER GROUND LAYER WITHIN THE PCB.

11486-002

Figure 12. Pin Configuration

Table 23. Pin Function Descriptions

Pin No.	Mnemonic	Internal Pull Resistor	Description
1	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane.
2	IOVDD	None	Input/Output Supply, 1.8 V – 10% to 3.3 V + 10%. Bypass this pin with decoupling capacitors to Pin 1 (DGND).
3	VDRIVE	None	PNP Bipolar Junction Transistor-Base Drive Bias Pin for the Digital Supply Regulator. Connect VDRIVE to the base of an external PNP pass transistor (STD2805 is recommended). If an external supply is provided directly to DVDD, connect the VDRIVE pin to ground.
4	SPDIFIN	None	Input to the Integrated Sony/Philips Digital Interface Format Receiver. Disconnect this pin when not in use. This pin is internally biased to IOVDD/2. This pin is nonfunctional on the ADAU1450 and should be left disconnected.
5	SPDIFOUT	Configurable	Output from the Integrated Sony/Philips Digital Interface Format Transmitter. Disconnect this pin when not in use. This pin is internally biased to IOVDD/2. This pin is nonfunctional on the ADAU1450 and should be left disconnected.
6	AGND	None	Analog Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane.
7	AVDD	None	Analog (Auxiliary ADC) Supply. Must be 3.3 V ± 10%. Bypass this pin with decoupling capacitors to Pin 6 (AGND).
8	AUXADC0	None	Auxiliary ADC Input Channel 0. This pin reads an analog input signal and uses its value in the DSP program. Disconnect this pin when not in use.
9	AUXADC1	None	Auxiliary ADC Input Channel 1. This pin reads an analog input signal and uses its value in the DSP program. Disconnect this pin when not in use.

Header Format

The self boot EEPROM header consists of 16 bytes of data, starting at the beginning of the internal memory of the slave EEPROM (Address 0). The header format (see Figure 39) consists of the following:

- 8-bit Sentinel 0xAA (shown in Figure 39 as 0b10101010)
- 24-bit address indicating the byte address of the header of the first block (normally this is 0x000010, which is the address immediately following the header)
- 64-bit PLL configuration (PLL_CHECKSUM = PLL_FB_DIV + MCLK_OUT + PLL_DIV)

Data Block Format

Following the header, several data blocks are stored in the EEPROM memory (see Figure 40).

Each data block consists of eight bytes that configure the length and address of the data, followed by a series of 4-byte data packets.

Each block consists of the following:

- One LST bit, which signals the last block before the footer. LST = 0b1 indicates the last block; LST = 0b0 indicates that additional blocks are still to follow.
- 13 bits that are reserved for future use. Set these bits to 0b0.
- Two MEM bits that select the target data memory bank (0x0 = Data Memory 0, 0x1 = Data Memory 1, 0x2 = program memory).
- 16-bit base address that sets the memory address at which the master port starts writing when loading data from the block into memory.
- 16-bit data length that defines the number of 4-byte data-words to be written.
- 16-bit jump address that tells the DSP core at which address in program memory it should begin execution when the self boot operation is complete. The jump address bits are ignored unless the LST bit is set to 0b1.
- Arbitrary number of packets of 32-bit data. The number of packets is defined by the 16-bit data length.

Footer Format

After all the data blocks, a footer signifies the end of the self boot EEPROM memory (see Figure 41). The footer consists of a 64-bit checksum, which is the sum of the header and all blocks and all data as 32-bit words.

After the self boot operation completes, the checksum of the downloaded data is calculated and the panic manager signals if it does not match the checksum in the EEPROM. If the checksum is set to 0 dec, the checksum checking is disabled.

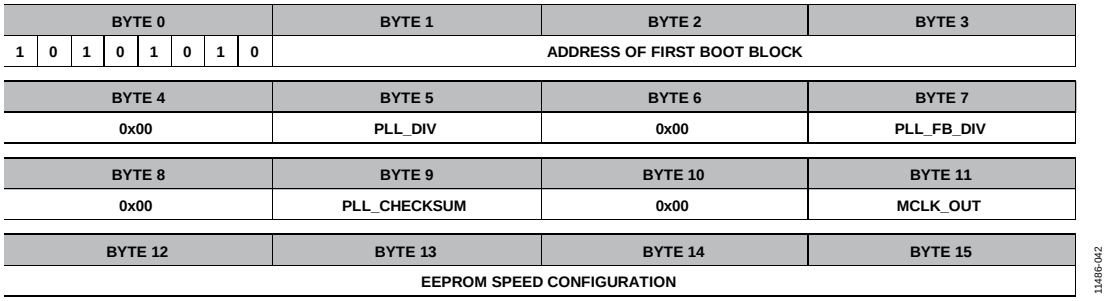


Figure 39. Self Boot EEPROM Header Format

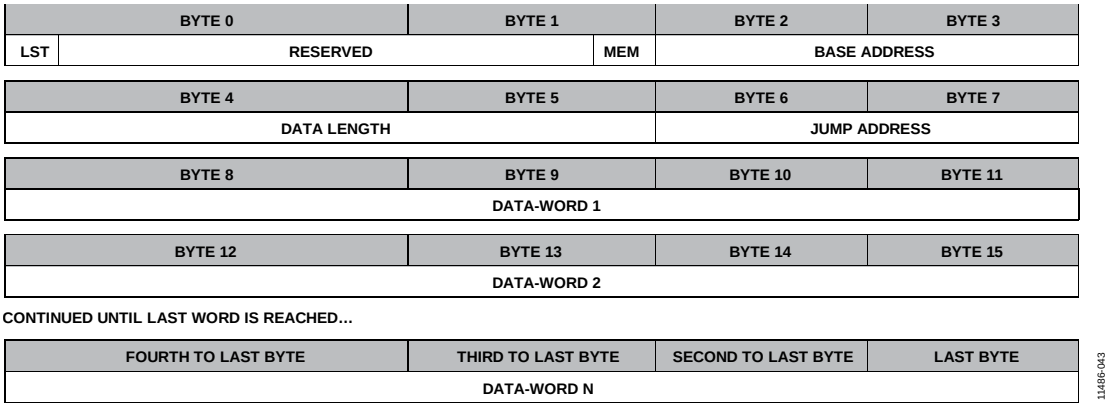


Figure 40. Self Boot EEPROM Data Block Format

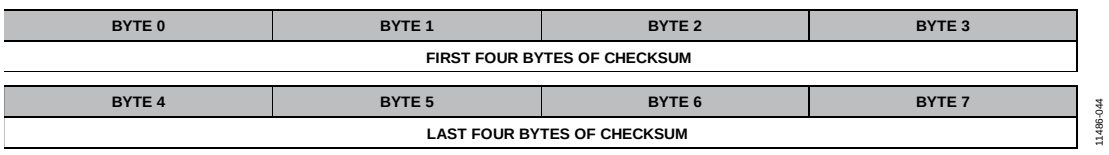


Figure 41. Self Boot EEPROM Footer Format

Serial Audio Inputs to DSP Core

The 48 serial input channels are mapped to four audio input cells in SigmaStudio. Each input cell corresponds to one of the serial input pins (see Table 37).

Depending on whether the serial port is configured in 2-channel, 4-channel, 8-channel, or 16-channel mode, the available channels in SigmaStudio change. The channel count for each serial port is configured in the SERIAL_BYTE_x_0 registers, Bits[2:0] (TDM_MODE), at Address 0xF200 to Address 0xF21C (in increments of 0x4).

Figure 43 shows how the input pins map to the input cells in SigmaStudio, including their graphical appearance in the software.

Table 37. Serial Input Pin Mapping to SigmaStudio Input Cells

Serial Input Pin	Channels in SigmaStudio
SDATA_IN0	0 to 15
SDATA_IN1	16 to 31
SDATA_IN2	32 to 39
SDATA_IN3	40 to 47

Table 38. Detailed Serial Input Mapping to SigmaStudio Input Channels[1]

Serial Input Pin	Position in I²S Stream (2-Channel)	Position in TDM4 Stream	Position in TDM8 Stream	Position in TDM16 Stream	Input Channel in SigmaStudio
SDATA_IN0	Left	0	0	0	0
SDATA_IN0	Right	1	1	1	1
SDATA_IN0	N/A	2	2	2	2
SDATA_IN0	N/A	3	3	3	3
SDATA_IN0	N/A	N/A	4	4	4
SDATA_IN0	N/A	N/A	5	5	5
SDATA_IN0	N/A	N/A	6	6	6
SDATA_IN0	N/A	N/A	7	7	7
SDATA_IN0	N/A	N/A	N/A	8	8
SDATA_IN0	N/A	N/A	N/A	9	9
SDATA_IN0	N/A	N/A	N/A	10	10
SDATA_IN0	N/A	N/A	N/A	11	11
SDATA_IN0	N/A	N/A	N/A	12	12
SDATA_IN0	N/A	N/A	N/A	13	13
SDATA_IN0	N/A	N/A	N/A	14	14
SDATA_IN0	N/A	N/A	N/A	15	15
SDATA_IN1	Left	0	0	0	16
SDATA_IN1	Right	1	1	1	17
SDATA_IN1	N/A	2	2	2	18
SDATA_IN1	N/A	3	3	3	19
SDATA_IN1	N/A	N/A	4	4	20
SDATA_IN1	N/A	N/A	5	5	21
SDATA_IN1	N/A	N/A	6	6	22
SDATA_IN1	N/A	N/A	7	7	23
SDATA_IN1	N/A	N/A	N/A	8	24
SDATA_IN1	N/A	N/A	N/A	9	25
SDATA_IN1	N/A	N/A	N/A	10	26
SDATA_IN1	N/A	N/A	N/A	11	27
SDATA_IN1	N/A	N/A	N/A	12	28
SDATA_IN1	N/A	N/A	N/A	13	29
SDATA_IN1	N/A	N/A	N/A	14	30
SDATA_IN1	N/A	N/A	N/A	15	31
SDATA_IN2	Left	0	0	0	32
SDATA_IN2	Right	1	1	1	33
SDATA_IN2	N/A	2	2	2	34
SDATA_IN2	N/A	3	3	3	35
SDATA_IN2	N/A	N/A	4	4	36
SDATA_IN2	N/A	N/A	5	5	37
SDATA_IN2	N/A	N/A	6	6	38
SDATA_IN2	N/A	N/A	7	7	39

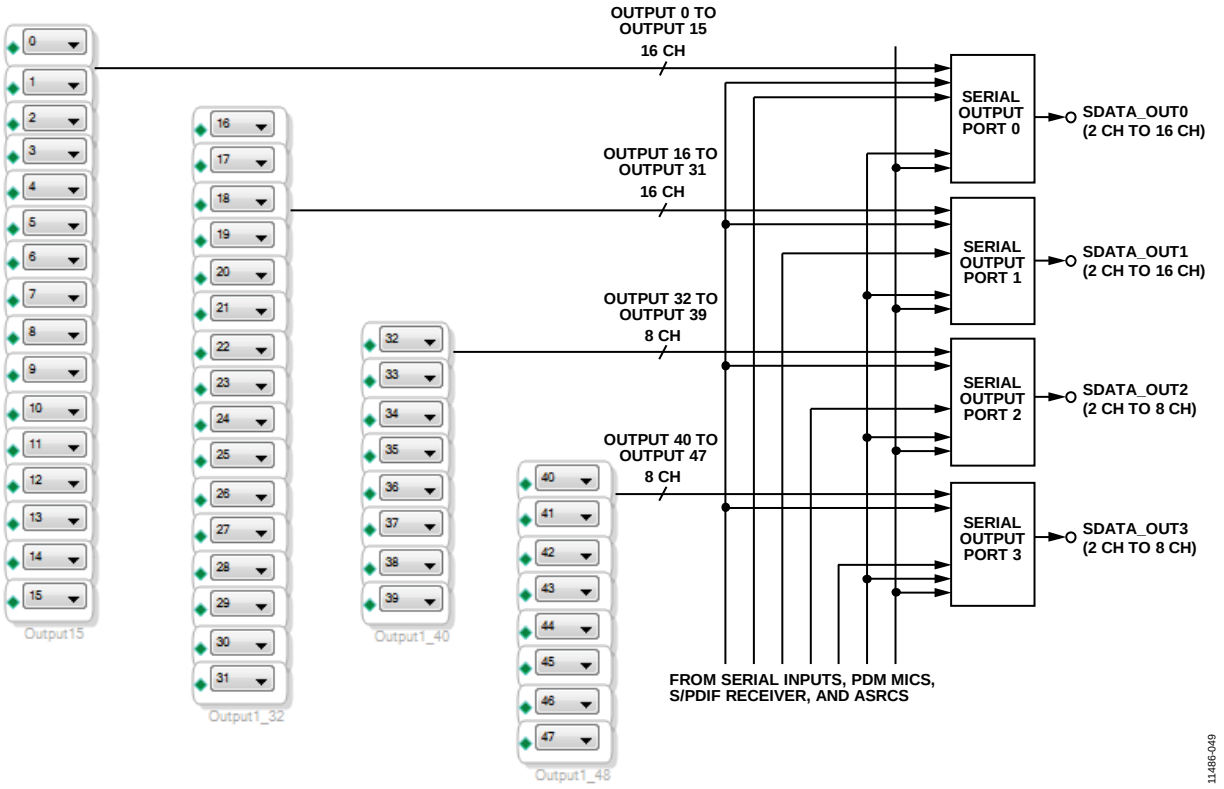


Figure 46. DSP to Serial Output Mapping in SigmaStudio

The data that is output from each serial output pin is also configurable, via the SOUT_SOURCEx registers, to originate from one of the following sources: the DSP, the serial inputs, the PDM microphone inputs, the S/PDIF receiver, or the ASRCs. These registers can be configured graphically in SigmaStudio, as shown in Figure 47.

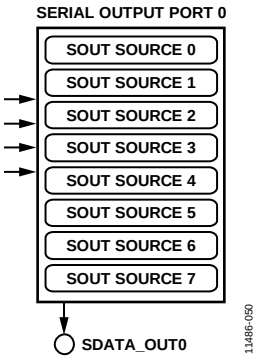


Figure 47. Configuring the Serial Output Data Channels (SOUT_SOURCEx Registers) Graphically in SigmaStudio

S/PDIF Audio Outputs from DSP Core to S/PDIF Transmitter

The output signal of the S/PDIF transmitter can come from the DSP core or directly from the S/PDIF receiver. The selection is controlled by Register 0xF1C0 (SPDIFTX_INPUT).

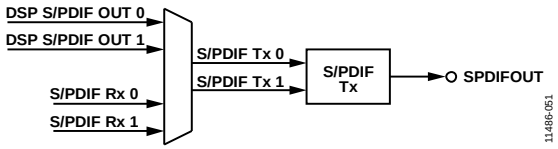


Figure 48. S/PDIF Transmitter Source Selection

When the signal comes from the DSP core, use the S/PDIF output cells in SigmaStudio.

Table 42. S/PDIF Output Mapping from SigmaStudio Channels

S/PDIF Output Channel in SigmaStudio	Channel in S/PDIF Transmitter Data Stream
0	Left
1	Right

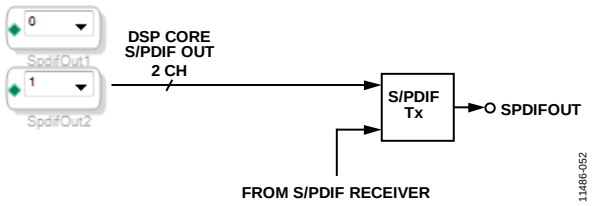


Figure 49. DSP to S/PDIF Transmitter Output Mapping in SigmaStudio

When the outputs of the ASRCs are required for processing in the SigmaDSP core, the ASRC input block must be selected in SigmaStudio (see Figure 52 and Figure 53). In the case of the ADAU1450, which has no ASRCs, the ASRC input cell does not generate any data.

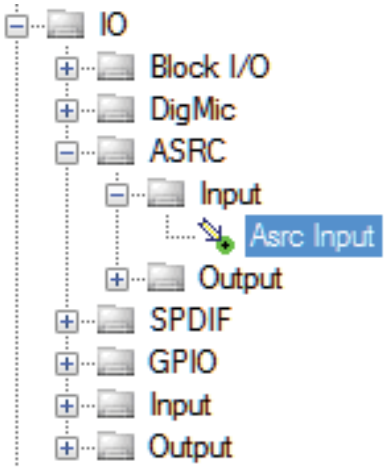


Figure 52. Location of ASRC-to-DSP Input Cell in SigmaStudio Toolbox

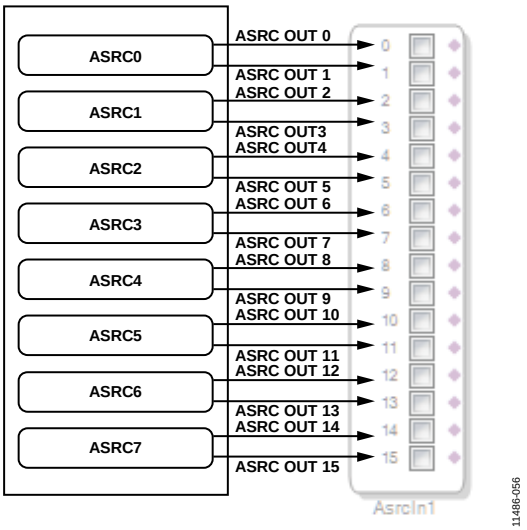


Figure 53. Routing of ASRC Outputs to ASRC-to-DSP Input Cell in SigmaStudio

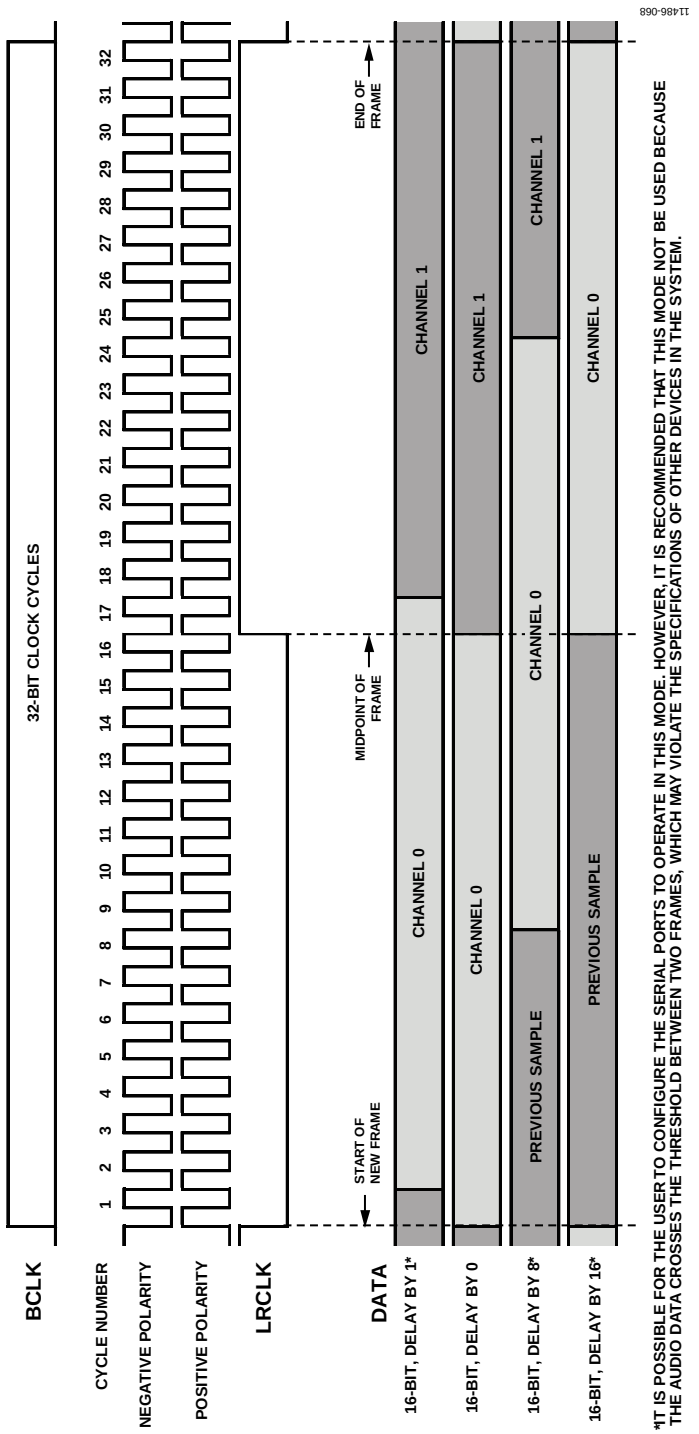


Figure 65. Serial Audio Data Formats; Two Channels, 16 Bits per Channel

Figure 65 shows some timing diagrams for possible serial port configurations in two channel mode, with 16 bit clock cycles per channel, for a total of 32 bit clock cycles per frame (refer to the SERIAL_BYTE_x_0 registers, Register 0xF200 to Register 0xF21C, Bits[2:0] (TDM_MODE) = 0b101).

Different bit clock polarities are illustrated (SERIAL_BYTE_x_0, Bit 7 (BCLK_POL)). The audio word length is fixed at 16 bits (SERIAL_BYTE_x_0, Bits[6:5] (WORD_LEN) = 0b01), and there are four possible configurations for MSB position (SERIAL_BYTE_x_0, Bits[4:3] (DATA_FMT)), all of which are shown in Figure 65.

The four multipliers are 64-bit double precision, capable of multiplying an 8.56 format number by an 8.24 number. The multiply accumulators consist of 16 registers, with a depth of 80 bits. The core can access RAM with a load/store width of 256 bits (eight 32-bit words per frame). The two ALUs have an 80-bit width and operate on numbers in 24.56 format. The 24.56-bit format provides more than 42 dB of headroom.

It is possible to create combinations of time domain and frequency domain processing, using block and sample frame interrupts. Sixteen data address generator (DAG) registers are available, and circular buffer addressing is possible.

Many of the signal processing functions are coded using full, 64-bit, double precision arithmetic. The serial port input and output word lengths are 24 bits, but eight extra headroom bits are used in the processor to allow internal gains of up to 48 dB without clipping. Additional gains can be achieved by initially scaling down the input signal in the DSP signal flow.

Numeric Formats

DSP systems commonly use a standard numeric format. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The same numeric format is used for both the parameter and data values.

A digital clipper circuit is used within the DSP core before outputting to the serial port outputs, ASRCs, and S/PDIF. This clips the top seven bits (and the least significant bit) of the signal to produce a 24-bit output with a range of +1.0 (minus 1 LSB) to −1.0. Figure 79 shows the maximum signal levels at each point in the data flow in both binary and decibel levels.

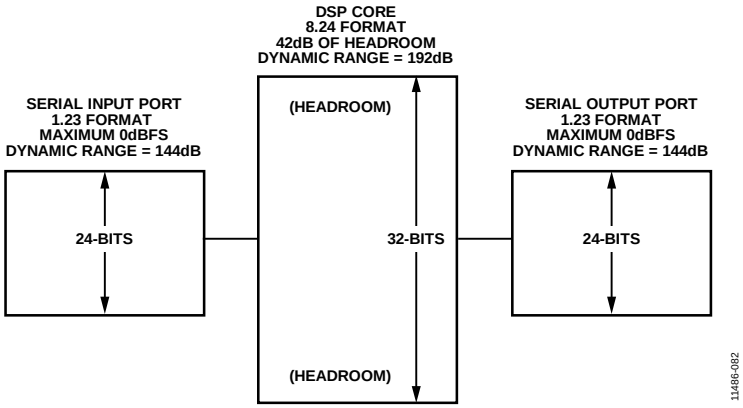


Figure 79. Signal Range for 1.23 Format (Serial Ports, ASRCs) and 8.24 Format (DSP Core)

Numerical Format: 8.24

Linear range: −128.0 to (+128.0 − 1 LSB)

Dynamic range (ratio of the largest possible signal level to the smallest possible non-zero signal level): 192 dB

```
Examples:
0b 1000 0000 0000 0000 0000 0000 0000 0000 = 0x80000000 = -128.0
0b 1110 0000 0000 0000 0000 0000 0000 0000 = 0xE0000000 = -32.0
0b 1111 1000 0000 0000 0000 0000 0000 0000 = 0xF8000000 = -8.0
0b 1111 1110 0000 0000 0000 0000 0000 0000 = 0xFE000000 = -2
0b 1111 1111 0000 0000 0000 0000 0000 0000 = 0xFF000000 = -1
0b 1111 1111 1000 0000 0000 0000 0000 0000 = 0xFF800000 = -0.5
0b 1111 1111 1110 0110 0110 0110 0110 0110 = 0xFFE66666 = -0.1
0b 1111 1111 1111 1111 1111 1111 1111 1111 = 0xFFFFFFFF = -0.00000005 (1 LSB below 0.0)
0b 0000 0000 0000 0000 0000 0000 0000 0000 = 0x00000000 = 0.0
0b 0000 0000 0000 0000 0000 0000 0000 0001 = 0x00000001 = 0.00000005 (1 LSB above 0.0)
0b 0000 0000 0001 1001 1001 1001 1001 1001 = 0x00199999 = 0.1
0b 0000 0000 0100 0000 0000 0000 0000 0000 = 0x00400000 = 0.25
0b 0000 0000 1000 0000 0000 0000 0000 0000 = 0x00800000 = 0.5
0b 0000 0001 0000 0000 0000 0000 0000 0000 = 0x01000000 = 1.0
0b 0000 0010 0000 0000 0000 0000 0000 0000 = 0x02000000 = 2.0
0b 0111 1111 1111 1111 1111 1111 1111 1111 = 0x7FFFFFFF = 127.99999994 (1 LSB below 128.0)
```

Reliability Features

Several reliability features are controlled by a panic manager subsystem that monitors the state of the SigmaDSP core and memories and generates alerts if error conditions are encountered. The panic manager indicates error conditions to the user via register flags and GPIO outputs. The origin of the error can be traced to different functional blocks such as the watchdog, memory, stack, software program, and core op codes.

Although designed mostly as an aid for software development, the panic manager is also useful in monitoring the state of the memories over long periods of time, such as in applications where the system operates unattended for an extended period, and resets are infrequent. The memories in the device have a built-in self test feature that runs automatically while the device is in operation. If a memory corruption is detected, the appropriate flag is signaled in the panic manager. The program running in the DSP core can monitor the state of the panic manager and can mute the audio outputs if an error is encountered, and external devices, such as microcontrollers, can poll the panic manager registers or monitor the multipurpose pins to perform some preprogrammed action, if necessary.

DSP Core and Reliability Registers

An overview of the registers related to the DSP core is shown in Table 57. For a more detailed description, see the DSP Core Control Registers section and Debug and Reliability Registers section.

Table 57. DSP Core and Reliability Registers

Address	Register	Description
0xF400	HIBERNATE	Hibernate setting
0xF401	START_PULSE	Start pulse selection
0xF402	START_CORE	Instruction to start the core
0xF403	KILL_CORE	Instruction to stop the core
0xF404	START_ADDRESS	Start address of the program
0xF405	CORE_STATUS	Core status
0xF421	PANIC_CLEAR	Clear the panic manager
0xF422	PANIC_PARITY_MASK	Panic parity
0xF423	PANIC_SOFTWARE_MASK	Panic Mask 0
0xF424	PANIC_WD_MASK	Panic Mask 1
0xF425	PANIC_STACK_MASK	Panic Mask 2
0xF426	PANIC_LOOP_MASK	Panic Mask 3
0xF427	PANIC_FLAG	Panic flag
0xF428	PANIC_CODE	Panic code
0xF432	EXECUTE_COUNT	Execute stage error program count
0xF443	WATCHDOG_MAXCOUNT	Watchdog maximum count
0xF444	WATCHDOG_PRESCALE	Watchdog prescale
0xF450	BLOCKINT_EN	Enable block interrupts
0xF451	BLOCKINT_VALUE	Value for the block interrupt counter
0xF460	PROG_CNTR0	Program counter, Bits[23:16]
0xF461	PROG_CNTR1	Program counter, Bits[15:0]
0xF462	PROG_CNTR_CLEAR	Program counter clear
0xF463	PROG_CNTR_LENGTH0	Program counter length, Bits[23:16]
0xF464	PROG_CNTR_LENGTH1	Program counter length, Bits[15:0]
0xF465	PROG_CNTR_MAXLENGTH0	Program counter maximum length, Bits[23:16]

Table 70. Bit Descriptions for MCLK_OUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:3]	RESERVED			0x0	RW
[2:1]	CLKOUT_RATE		Frequency of CLKOUT. Frequency of the signal output from the CLKOUT pin. These bits set the frequency of the signal on the CLKOUT pin. The frequencies documented in Table 70 are examples that are valid for a master clock input that is a binary multiple of 3.072 MHz. In this case, the options for output rates are 3.072 MHz, 6.144 MHz, 12.288 MHz, or 24.576 MHz. If the input master clock is scaled down (for example, to a binary multiple of 2.8224 MHz), the possible output rates are 2.8224 MHz, 5.6448 MHz, 11.2896 MHz, or 22.5792 MHz).	0x0	RW
		00	Predivider output. This is 3.072 MHz for a nominal system clock of 294.912 MHz.		
		01	Double the predivider output. This is 6.144 MHz for a nominal system clock of 294.912 MHz.		
		10	Four times the predivider output. This is 12.288 MHz for a nominal system clock of 294.912 MHz.		
		11	Eight times the predivider output. This is 24.576 MHz for a nominal system clock of 294.912 MHz.		
0	CLKOUT_ENABLE		CLKOUT enable. When this bit is enabled, a clock signal is output from the CLKOUT pin of the device. When disabled, the CLKOUT pin is high impedance.	0x0	RW
		0	CLKOUT pin disabled		
		1	CLKOUT pin enabled		

Analog PLL Watchdog Control Register

Address: 0xF006, Reset: 0x0001, Name: PLL_WATCHDOG

The PLL watchdog is a feature that monitors the PLL and automatically resets it in the event that it reaches an unstable condition. The PLL resets itself and automatically attempts to lock to the incoming clock signal again, with the same settings as before. This functionality requires no interaction on the part of the user. Ensure that the PLL watchdog is enabled at all times.

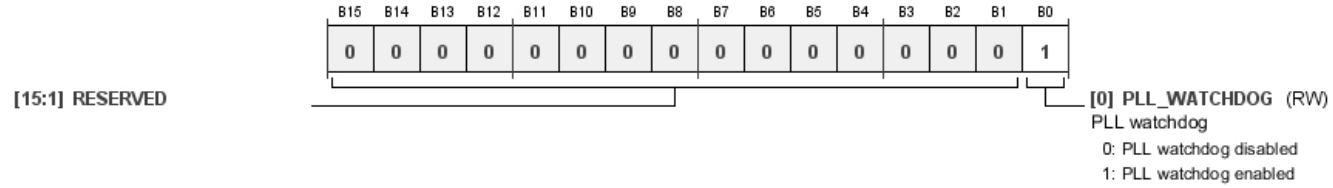


Table 71. Bit Descriptions for PLL_WATCHDOG

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	PLL_WATCHDOG		PLL watchdog.	0x1	RW
		0	PLL watchdog disabled		
		1	PLL watchdog enabled		

Bits	Bit Name	Settings	Description	Reset	Access
[2:0]	SOUT_SOURCE		Audio data source for these serial audio output channels. If these bits are set to 0b001, the corresponding output channels output a copy of the data from the corresponding input channels. For example, if Address 0xF180, Bits[2:0] are set to 0b001, Serial Input Channel 0 and Serial Input Channel 1 copy to Serial Output Channel 0 and Serial Output Channel 1, respectively. If these bits are set to 0b010, DSP Output Channel 0 and DSP Output Channel 1 copy to Serial Output Channel 0 and Serial Output Channel 1, respectively. If these bits are set to 0b011, Bits[5:3] (SOUT_ASRC_SELECT) must be configured to select the desired ASRC output.	0x0	RW
		000	Disabled; these output channels are not used		
		001	Direct copy of data from corresponding serial input channels		
		010	Data from corresponding DSP core output channels		
		011	From ASRC (select channel using Bits[5:3], SOUT_ASRC_SELECT) on the ADAU1452 and ADAU1451		
		100	Digital PDM Microphone Input Channel 0 and Digital PDM Microphone Input Channel 1		
		101	Digital PDM Microphone Input Channel 2 and Digital PDM Microphone Input Channel 3		

S/PDIF Transmitter Data Selector Register

Address: 0xF1C0, Reset: 0x0000, Name: SPDIFTX_INPUT

This register configures which data source feeds the S/PDIF transmitter on the ADAU1452 and ADAU1451. Data can originate from the S/PDIF outputs of the DSP core or directly from the S/PDIF receiver.

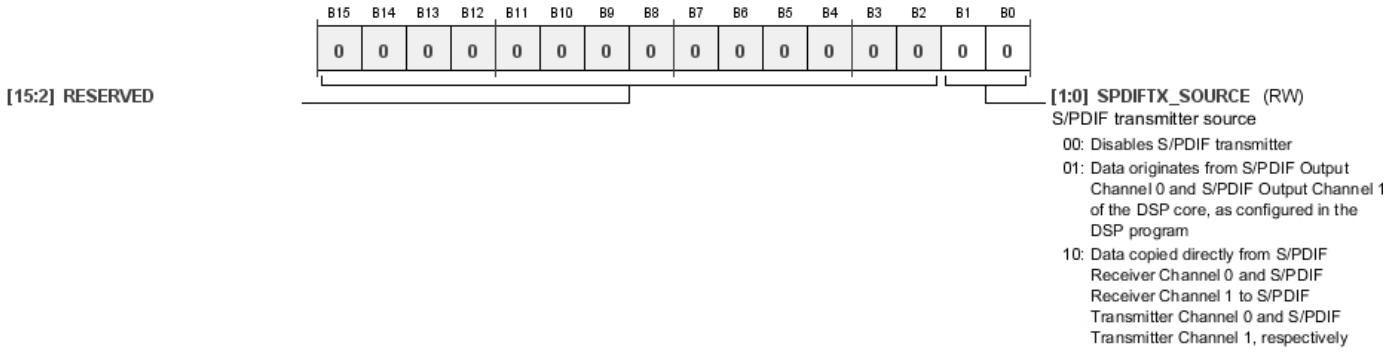


Table 85. Bit Descriptions for SPDIFTX_INPUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:2]	RESERVED			0x0	RW
[1:0]	SPDIFTX_SOURCE		S/PDIF transmitter source.	0x0	RW
		00	Disables S/PDIF transmitter		
		01	Data originates from S/PDIF Output Channel 0 and S/PDIF Output Channel 1 of the DSP core, as configured in the DSP program		
		10	Data copied directly from S/PDIF Receiver Channel 0 and S/PDIF Receiver Channel 1 to S/PDIF Transmitter Channel 0 and S/PDIF Transmitter Channel 1, respectively		

Bits	Bit Name	Settings	Description	Reset	Access
[4:3]	DATA_FMT		MSB position. These bits set the positioning of the data in the frame on the corresponding serial port.	0x0	RW
		00	I²S (delay data by one BCLK cycle)		
		01	Left justified (delay data by zero BCLK cycles)		
		10	Right justified for 24-bit data (delay data by 8 BCLK cycles)		
		11	Right justified for 16-bit data (delay data by 16 BCLK cycles)		
[2:0]	TDM_MODE		Channels per frame and BCLK cycles per channel. These bits set the number of channels per frame and the number of bit clock cycles per frame on the corresponding serial port.	0x0	RW
		000	2 channels, 32 bit clock cycles per channel, 64 bit clock cycles per frame		
		001	4 channels, 32 bit clock cycles per channel, 128 bit clock cycles per frame		
		010	8 channels, 32 bit clock cycles per channel, 256 bit clock cycles per frame		
		011	16 channels, 32 bit clock cycles per channel, 512 bit clock cycles per frame		
		100	4 channels, 16 bit clock cycles per channel, 64 bit clock cycles per frame		
		101	2 channels, 16 bit clock cycles per channel, 32 bit clock cycles per frame		

Serial Port Control 1 Register

Address: 0xF201 to 0xF21D (Increments of 0x4), Reset: 0x0002, Name: SERIAL_BYTE_x_1

These eight registers configure several settings for the corresponding serial input and serial output ports. Clock generator, sample rate, and behavior during inactive channels are configured with these registers. On the input side, Register 0xF201 (SERIAL_BYTE_0_1) corresponds to SDATA_IN0; Register 0xF205 (SERIAL_BYTE_1_1) corresponds to SDATA_IN1; Register 0xF209 (SERIAL_BYTE_2_1) corresponds to SDATA_IN2; and Register 0xF20D (SERIAL_BYTE_3_1) corresponds to SDATA_IN3. On the output side, Register 0xF211 (SERIAL_BYTE_4_1) corresponds to SDATA_OUT0; Register 0xF215 (SERIAL_BYTE_5_1) corresponds to SDATA_OUT1; Register 0xF219 (SERIAL_BYTE_6_1) corresponds to SDATA_OUT2; and Register 0xF21D (SERIAL_BYTE_7_1) corresponds to SDATA_OUT3.

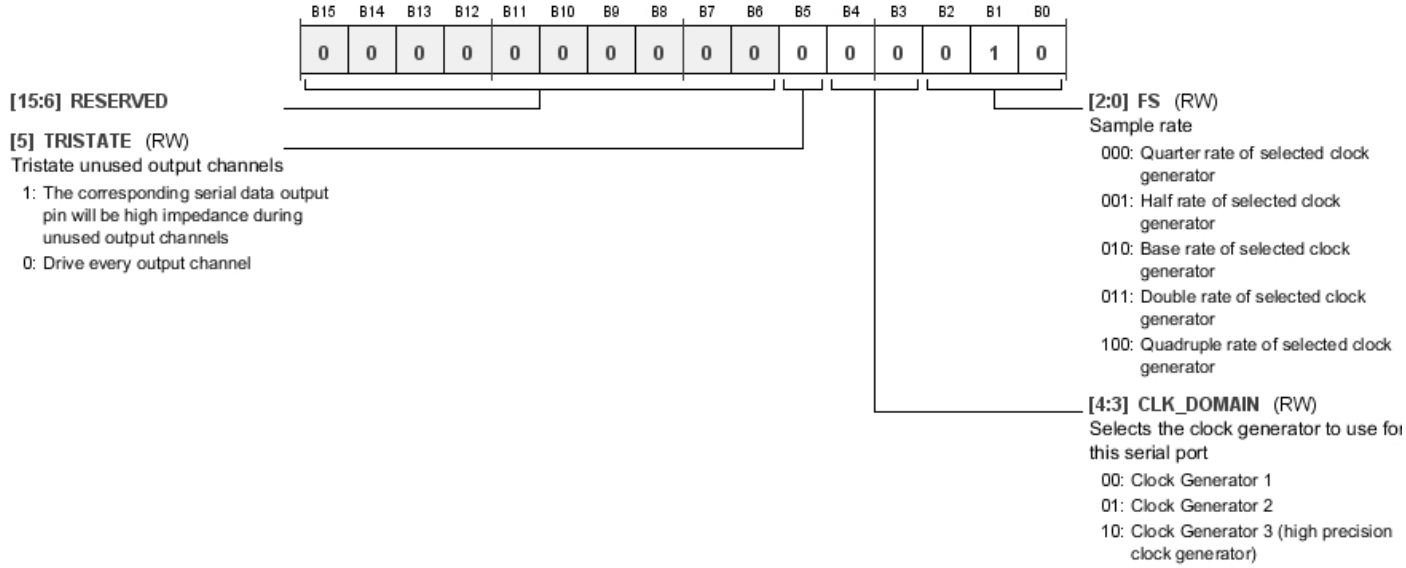


Table 87. Bit Descriptions for SERIAL_BYTE_x_1

Bits	Bit Name	Settings	Description	Reset	Access
[15:6]	RESERVED			0x000	RW
5	TRISTATE		Tristate unused output channels. This bit has no effect on serial input ports.	0x0	RW
		1	The corresponding serial data output pin is high impedance during unused output channels		
		0	Drive every output channel		

Bits	Bit Name	Settings	Description	Reset	Access
[4:2]	CHANNEL_OUT_POS		Source serial output channel. These bits, along with Bit 5 (SERIAL_OUT_SEL), select which serial output channel is the source of data for the corresponding flexible TDM output slot. If Bit 5 (SERIAL_OUT_SEL) = 0b0, Bits[4:2] (CHANNEL_OUT_POS) select serial output channels between Serial Output Channel 32 and Serial Output Channel 39. If Bit 5 (SERIAL_OUT_SEL) = 0b1, Bits[4:2] (CHANNEL_OUT_POS) selects serial output channels between Serial Output Channel 40 and Serial Output Channel 47.	0x0	RW
		000	Serial Output Channel 32 or Serial Output Channel 40		
		001	Serial Output Channel 33 or Serial Output Channel 41		
		010	Serial Output Channel 34 or Serial Output Channel 42		
		011	Serial Output Channel 35 or Serial Output Channel 43		
		100	Serial Output Channel 36 or Serial Output Channel 44		
		101	Serial Output Channel 37 or Serial Output Channel 45		
		110	Serial Output Channel 38 or Serial Output Channel 46		
		111	Serial Output Channel 39 or Serial Output Channel 47		
[1:0]	BYTE_OUT_POS		Source data byte. These bits determine which data byte is used from the corresponding serial output channel (selected by setting Bit 5 (SERIAL_OUT_SEL) and Bits[4:2] (CHANNEL_OUT_POS)). Because there can be up to 32 bits in the data-word, four bytes are available.	0x0	RW
		00	Byte 0; Bits[31:24]		
		01	Byte 1; Bits[23:16]		
		10	Byte 2; Bits[15:8]		
		11	Byte 3; Bits[7:0]		

Bits	Bit Name	Settings	Description	Reset	Access
6	DM0_BANK2_MASK		DM0 Bank 2 mask.	0x0	RW
		0	Report DM0_BANK2 parity mask errors		
		1	Do not report DM0_BANK2 parity mask errors		
5	DM0_BANK1_MASK		DM0 Bank 1 mask.	0x0	RW
		0	Report DM0_BANK1 parity mask errors		
		1	Do not report DM0_BANK1 parity mask errors		
4	DM0_BANK0_MASK		DM0 Bank 0 mask.	0x0	RW
		0	Report DM0_BANK0 parity mask errors		
		1	Do not report DM0_BANK0 parity mask errors		
3	PM1_MASK		PM1 parity mask.	0x0	RW
		0	Report PM1 parity mask errors		
		1	Do not report PM1 parity mask errors		
2	PM0_MASK		PM0 parity mask.	0x0	RW
		0	Report PM0 parity mask errors		
		1	Do not report PM0 parity mask errors		
1	ASRC1_MASK		ASRC 1 parity mask.	0x1	RW
		0	Report ASRC 1 parity mask errors		
		1	Do not report ASRC 1 parity mask errors		
0	ASRC0_MASK		ASRC 0 parity mask.	0x1	RW
		0	Report ASRC 0 parity mask errors		
		1	Do not report ASRC 0 parity mask errors		

Panic Mask 0 Register

Address: 0xF423, Reset: 0x0000, Name: PANIC_SOFTWARE_MASK

The panic manager checks and reports software errors. Register 0xF423 (PANIC_SOFTWARE_MASK) allows the user to configure whether software errors are reported to the panic manager or ignored.

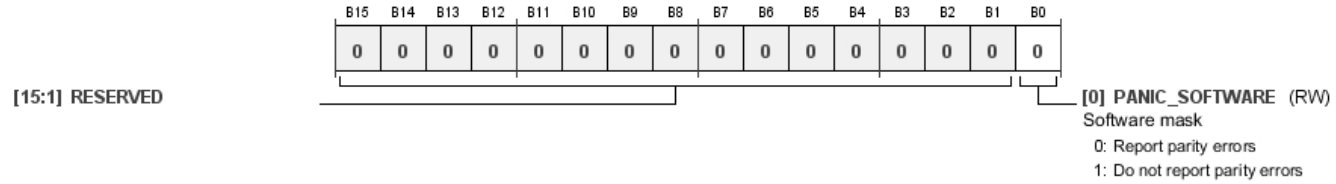


Table 98. Bit Descriptions for PANIC_SOFTWARE_MASK

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	PANIC_SOFTWARE		Software mask.	0x0	RW
		0	Report parity errors		
		1	Do not report parity errors		

MULTIPURPOSE PIN CONFIGURATION REGISTERS

Multipurpose Pin Mode Register

Address: 0xF510 to 0xF51D (Increments of 0x1), Reset: 0x0000, Name: MPx_MODE

These 14 registers configure the multipurpose pins. Certain multipurpose pins can function as audio clock pins, control bus pins, or general-purpose input or output (GPIO) pins.

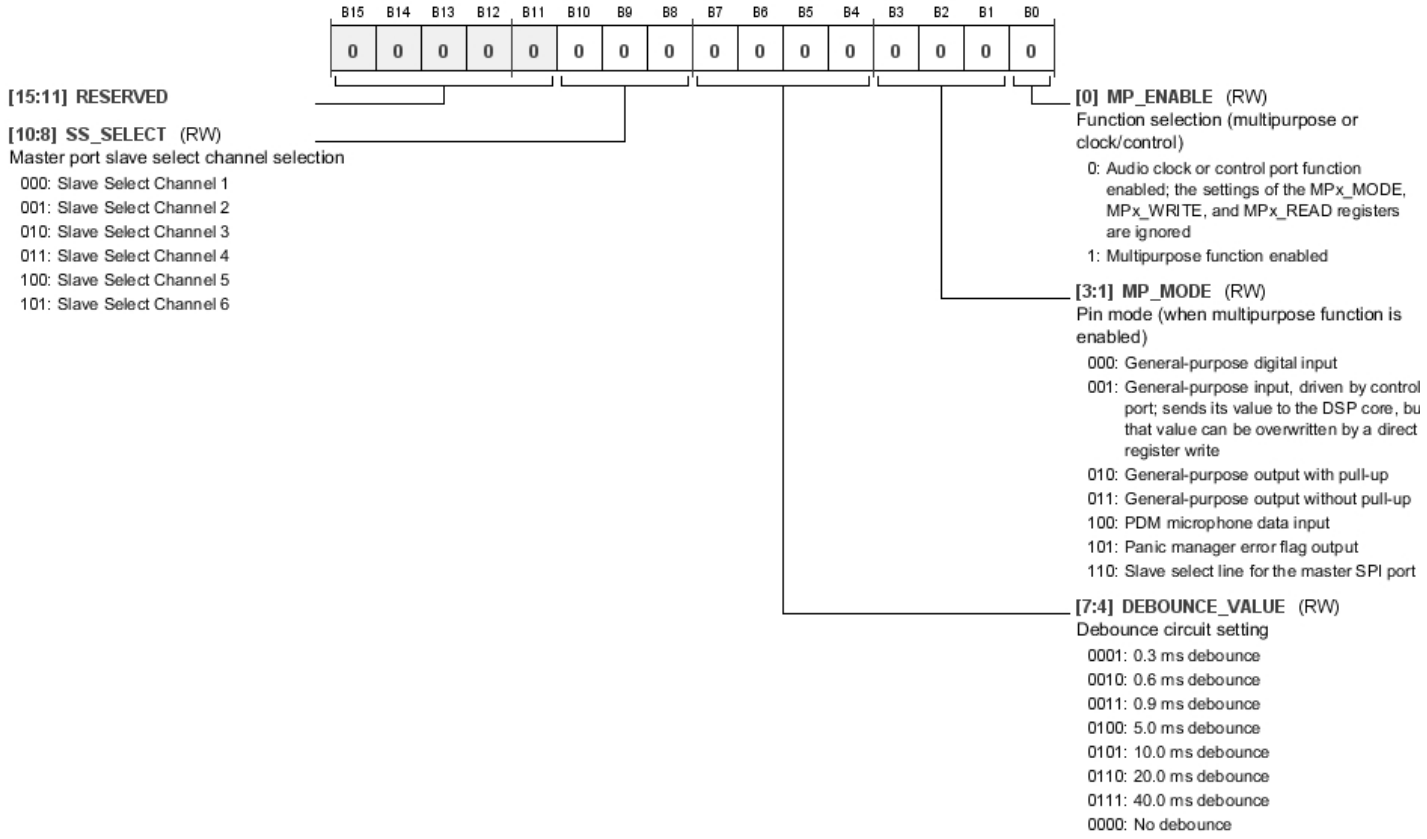


Table 116. Bit Descriptions for MPx_MODE

Bits	Bit Name	Settings	Description	Reset	Access
[15:11]	RESERVED			0x0	RW
[10:8]	SS_SELECT		Master port slave select channel selection. If the pin is configured as a slave select line (Bits[3:1] (MP_MODE) = 0b110), these bits configure which slave select channel the pin corresponds to. This allows multiple slave devices to be connected to the SPI master port, all using different slave select lines. The first slave select signal (Slave Select 0) is always routed to the SS_M/MP0 pin. The remaining six slave select lines can be routed to any multipurpose pin that has been configured as a slave select output.	0x0	RW
		000	Slave Select Channel 1		
		001	Slave Select Channel 2		
		010	Slave Select Channel 3		
		011	Slave Select Channel 4		
		100	Slave Select Channel 5		
		101	Slave Select Channel 6		

S/PDIF INTERFACE REGISTERS

S/PDIF Receiver Lock Bit Detection Register

Address: 0xF600, Reset: 0x0000, Name: SPDIF_LOCK_DET

This register contains a flag that monitors the S/PDIF receiver on the ADAU1452 and ADAU1451 and provides a way to check the validity of the input signal.

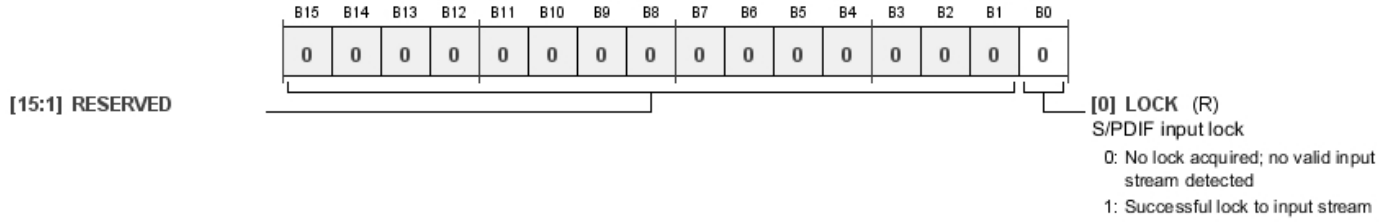


Table 124. Bit Descriptions for SPDIF_LOCK_DET

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0	RW
0	LOCK		S/PDIF input lock.	0x0	R
		0	No lock acquired; no valid input stream detected		
		1	Successful lock to input stream		

S/PDIF Receiver Control Register

Address: 0xF601, Reset: 0x0000, Name: SPDIF_RX_CTRL

This register provides controls that govern the behavior of the S/PDIF receiver on the ADAU1452 and ADAU1451.

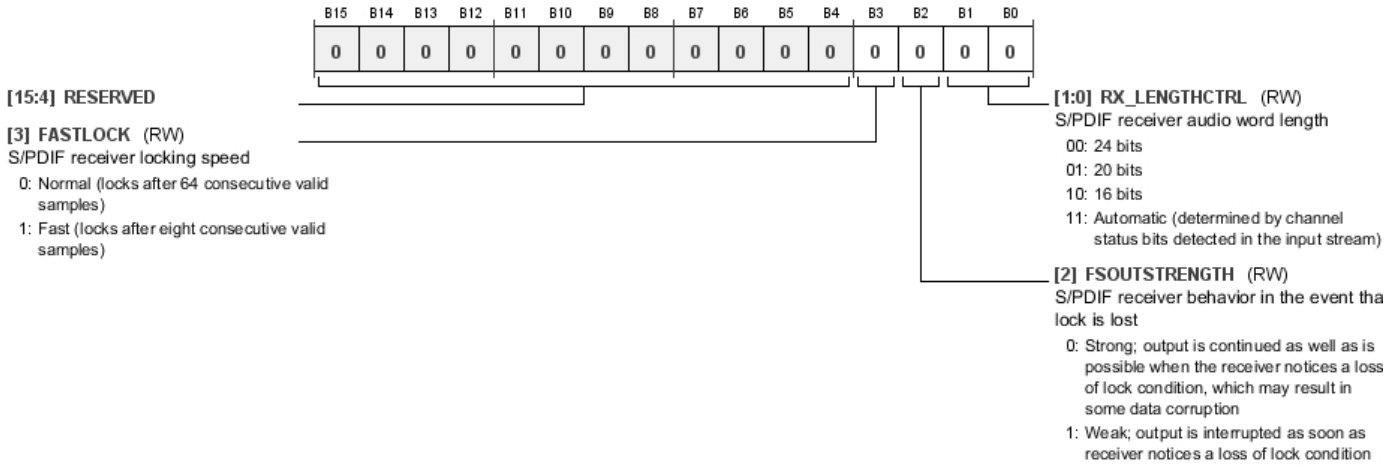


Table 125. Bit Descriptions for SPDIF_RX_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	RESERVED			0x0	RW
3	FASTLOCK		S/PDIF receiver locking speed.	0x0	RW
		0	Normal (locks after 64 consecutive valid samples)		
		1	Fast (locks after eight consecutive valid samples)		

S/PDIF Transmitter User Data Bits (Left) Register

Address: 0xF6C0 to 0xF6CB (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_UD_LEFT_x

These 12 registers allow the 192 user data bits encoded on the left channel of the output data stream of the S/PDIF transmitter on the ADAU1452 and ADAU1451 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

Table 145. Bit Descriptions for SPDIF_TX_UD_LEFT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_UD_LEFT		S/PDIF transmitter user data bits (left).	0x0000	RW

S/PDIF Transmitter User Data Bits (Right) Register

Address: 0xF6D0 to 0xF6DB (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_UD_RIGHT_x

These 12 registers allow the 192 user data bits encoded on the right channel of the output data stream of the S/PDIF transmitter on the ADAU1452 and ADAU1451 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

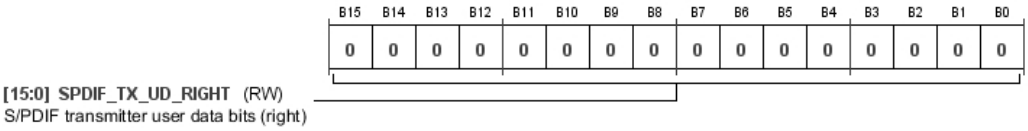


Table 146. Bit Descriptions for SPDIF_TX_UD_RIGHT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_UD_RIGHT		S/PDIF transmitter user data bits (right).	0x0000	RW

S/PDIF Transmitter Validity Bits (Left) Register

Address: 0xF6E0 to 0xF6EB (Increments of 0x1), Reset: 0x0000, Name: SPDIF_TX_VB_LEFT_x

These 12 registers allow the 192 validity bits encoded on the left channel of the output data stream of the S/PDIF transmitter on the ADAU1452 and ADAU1451 to be manually configured. For these bits to be output properly on the S/PDIF transmitter, Register 0xF69F (SPDIF_TX_AUXBIT_SOURCE), Bit 0 (TX_AUXBITS_SOURCE), must be set to 0b0.

Table 147. Bit Descriptions for SPDIF_TX_VB_LEFT_x

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SPDIF_TX_VB_LEFT		S/PDIF transmitter validity bits (left).	0x0000	RW

BCLK Output Pins Drive Strength and Slew Rate Register

Address: 0xF784 to 0xF787 (Increments of 0x1), Reset: 0x0018, Name: BCLK_OUTx_PIN

These registers configure the drive strength, slew rate, and pull resistors for the BCLK_OUTx pins. Register 0xF784 corresponds to BCLK_OUT0, Register 0xF785 corresponds to BCLK_OUT1, Register 0xF786 corresponds to BCLK_OUT2, and Register 0xF787 corresponds to BCLK_OUT3.

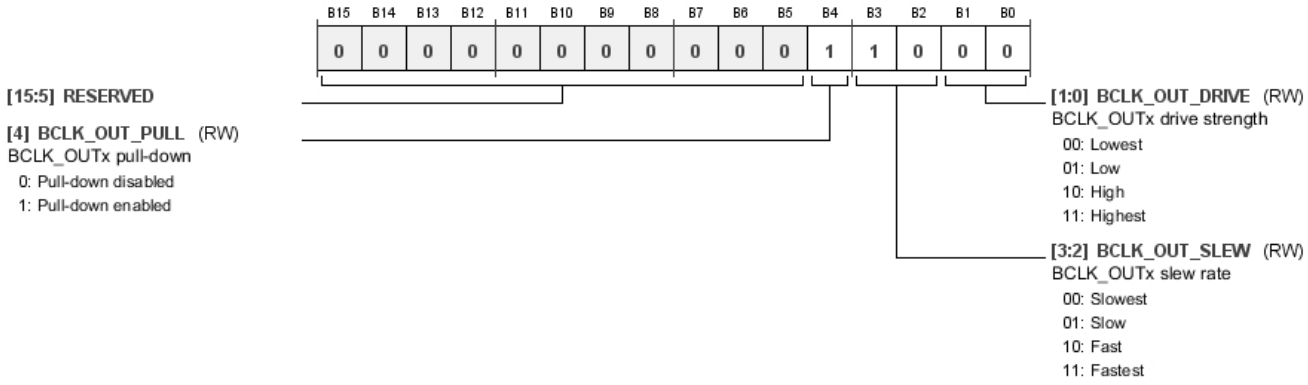


Table 152. Bit Descriptions for BCLK_OUTx_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x0	RW
4	BCLK_OUT_PULL		BCLK_OUTx pull-down.	0x1	RW
		0	Pull-down disabled		
		1	Pull-down enabled		
[3:2]	BCLK_OUT_SLEW		BCLK_OUTx slew rate.	0x2	RW
		00	Slowest		
		01	Slow		
		10	Fast		
		11	Fastest		
[1:0]	BCLK_OUT_DRIVE		BCLK_OUTx drive strength.	0x0	RW
		00	Lowest		
		01	Low		
		10	High		
		11	Highest		

APPLICATIONS INFORMATION

PCB DESIGN CONSIDERATIONS

A solid ground plane is a necessity for maintaining signal integrity and minimizing EMI radiation. If the PCB has two ground planes, they can be stitched together using vias that are spread evenly throughout the board.

Power Supply Bypass Capacitors

Bypass each power supply pin to its nearest appropriate ground pin with a single 100 nF capacitor and, optionally, with an additional 10 nF capacitor in parallel. Make the connections to each side of the capacitor as short as possible, and keep the trace on a single layer with no vias. For maximum effectiveness, place the capacitor either equidistant from the power and ground pins or, when equidistant placement is not possible, slightly nearer to the power pin (see Figure 81). Establish the thermal connections to the planes on the far side of the capacitor.

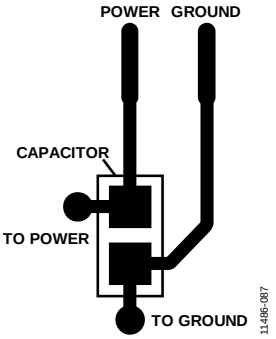


Figure 81. Recommended Power Supply Bypass Capacitor Layout

Typically, a single 100 nF capacitor for each power ground pin pair is sufficient. However, if there is excessive high frequency noise in the system, use an additional 10 nF capacitor in parallel (see Figure 82). In that case, place the 10 nF capacitor between the devices and the 100 nF capacitor, and establish the thermal connections on the far side of the 100 nF capacitor.

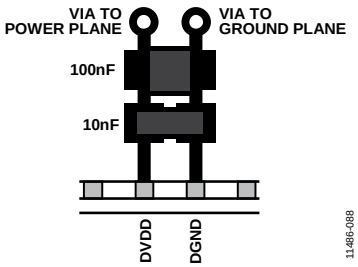


Figure 82. Layout for Multiple Power Supply Bypass Capacitors

To provide a current reservoir in case of sudden current spikes, use a 10 µF capacitor for each named supply (DVDD, AVDD, PVDD, and IOVDD) as shown in Figure 83.

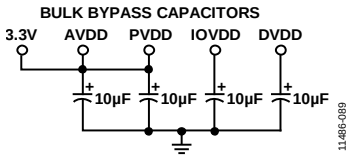


Figure 83. Bulk Capacitor Schematic

Parts Placement

Place all 100 nF bypass capacitors, which are recommended for every analog, digital, and PLL power ground pair, as near as possible to the ADAU1452/ADAU1451/ADAU1450. Bypass each of the AVDD, DVDD, PVDD, and IOVDD supply signals on the board with an additional single bulk capacitor (10 µF to 47 µF).

Keep all traces in the crystal resonator circuit (see Figure 15) as short as possible to minimize stray capacitance. Do not connect any long board traces to the crystal oscillator circuit components because such traces may affect crystal startup and operation.

Grounding

Use a single ground plane in the application layout. Place all components in an analog signal path away from digital signals.

Exposed Pad PCB Design

The device package includes an exposed pad for improved heat dissipation. When designing a board for such a package, give special consideration to the following:

- Place a copper layer, equal in size to the exposed pad, on all layers of the board, from top to bottom. Connect the copper layers to a dedicated copper board layer (see Figure 84).

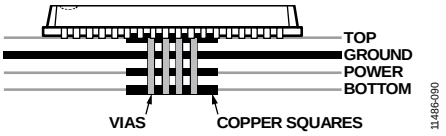


Figure 84. Exposed Pad Layout Example—Side View

- Place vias such that all layers of copper are connected, allowing for efficient heat and energy conductivity. For an example, see Figure 85, which shows 49 vias arranged in a 7 × 7 grid in the pad area.

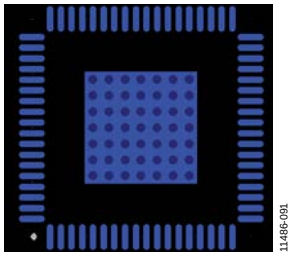


Figure 85. Exposed Pad Layout Example—Top View

PLL Filter

To minimize jitter, connect the single resistor and two capacitors in the PLL filter to the PLLFILT and PVDD pins with short traces.

Power Supply Isolation with Ferrite Beads

Ferrite beads can be used for supply isolation. When using ferrite beads, always place the beads outside the local high frequency decoupling capacitors, as shown in Figure 86. If the ferrite beads are placed between the supply pin and the decoupling capacitor, high frequency noise is reflected back into the IC because there is no suitable return path to ground. As a result, EMI increases, creating noisy supplies.

EOS/ESD Protection

Although the ADAU1452/ADAU1451/ADAU1450 has robust internal protection circuitry against overvoltages and electrostatic discharge, an external transient voltage suppressor (TVS) is recommended for all systems to prevent damage to the IC. For examples, see the AN-311 Application Note.

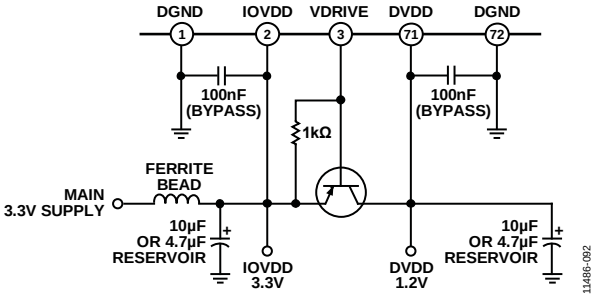


Figure 86. Ferrite Bead Power Supply Isolation Circuit Example

TYPICAL APPLICATIONS BLOCK DIAGRAM

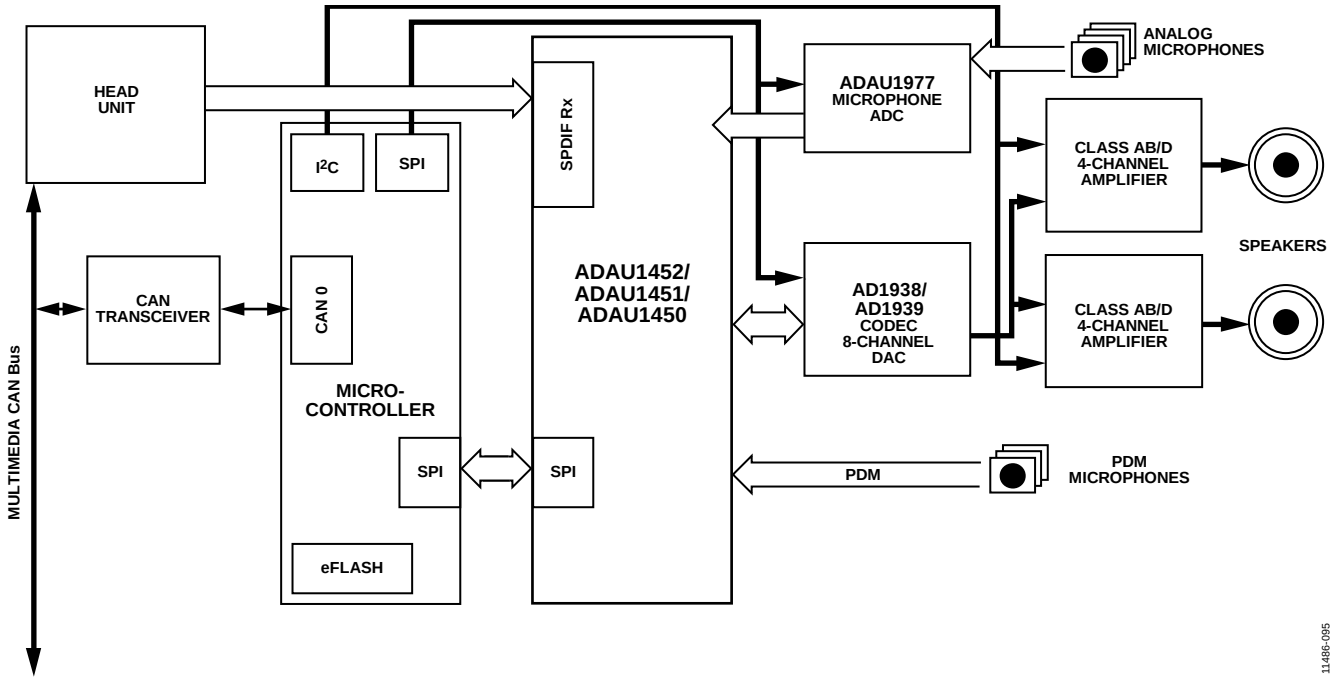


Figure 87. Automotive Infotainment Amplifier Block Diagram