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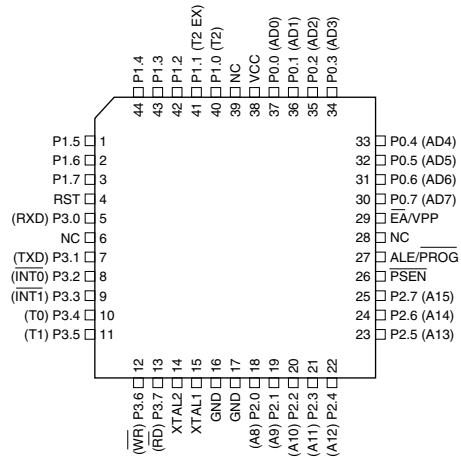
Applications of "Embedded - Microcontrollers"
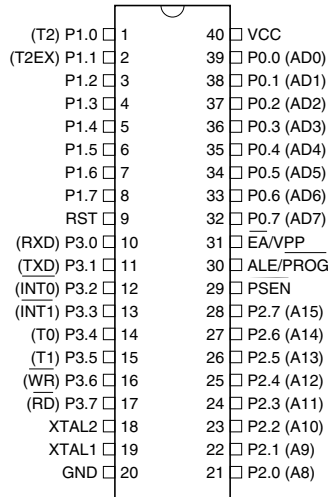
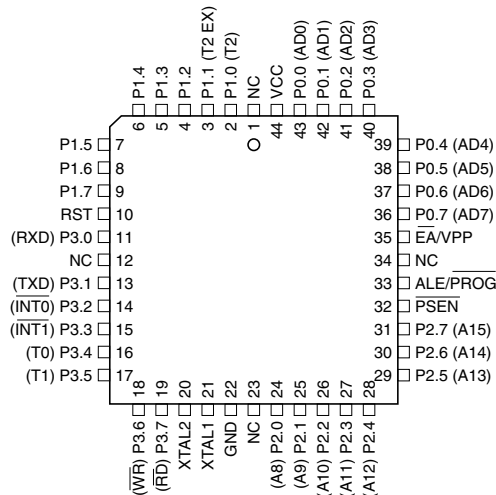| Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	WDT
Number of I/O	32
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c55wd-24pi

Pin Configurations

TQFP

```
              P1.4  44          
              P1.3  43          
              P1.2  42          
      P1.1 (T2 EX)  41          
         P1.0 (T2)  40          
               NC   39          
              VCC   38          
         P0.0 (AD0) 37          
         P0.1 (AD1) 36          
         P0.2 (AD2) 35          
         P0.3 (AD3) 34          

        P1.5  1                 33  P0.4 (AD4)
        P1.6  2                 32  P0.5 (AD5)
        P1.7  3                 31  P0.6 (AD6)
         RST  4                 30  P0.7 (AD7)
  (RXD) P3.0  5                 29  EA/VPP
          NC  6                 28  NC
  (TXD) P3.1  7                 27  ALE/PROG
 (INT0) P3.2  8                 26  PSEN
 (INT1) P3.3  9                 25  P2.7 (A15)
   (T0) P3.4 10                 24  P2.6 (A14)
   (T1) P3.5 11                 23  P2.5 (A13)

              12  13  14  15  16  17  18  19  20  21  22
     (WR) P3.6                                      P2.4 (A12)
     (RD) P3.7                                  P2.3 (A11)
              XTAL2                          P2.2 (A10)
                  XTAL1                  P2.1 (A9)
                      GND            P2.0 (A8)
                          GND
```

PDIP

```
      (T2) P1.0  ▢ 1       40 ▢  VCC
    (T2EX) P1.1  ▢ 2       39 ▢  P0.0 (AD0)
           P1.2  ▢ 3       38 ▢  P0.1 (AD1)
           P1.3  ▢ 4       37 ▢  P0.2 (AD2)
           P1.4  ▢ 5       36 ▢  P0.3 (AD3)
           P1.5  ▢ 6       35 ▢  P0.4 (AD4)
           P1.6  ▢ 7       34 ▢  P0.5 (AD5)
           P1.7  ▢ 8       33 ▢  P0.6 (AD6)
            RST  ▢ 9       32 ▢  P0.7 (AD7)
    (RXD) P3.0   ▢ 10      31 ▢  EA/VPP
    (TXD) P3.1   ▢ 11      30 ▢  ALE/PROG
   (INT0) P3.2   ▢ 12      29 ▢  PSEN
   (INT1) P3.3   ▢ 13      28 ▢  P2.7 (A15)
     (T0) P3.4   ▢ 14      27 ▢  P2.6 (A14)
     (T1) P3.5   ▢ 15      26 ▢  P2.5 (A13)
     (WR) P3.6   ▢ 16      25 ▢  P2.4 (A12)
     (RD) P3.7   ▢ 17      24 ▢  P2.3 (A11)
          XTAL2  ▢ 18      23 ▢  P2.2 (A10)
          XTAL1  ▢ 19      22 ▢  P2.1 (A9)
            GND  ▢ 20      21 ▢  P2.0 (A8)
```

PLCC

```
              P1.4   6          
              P1.3   5          
              P1.2   4          
      P1.1 (T2 EX)   3          
         P1.0 (T2)   2          
               NC    1          
              VCC   44          
         P0.0 (AD0) 43          
         P0.1 (AD1) 42          
         P0.2 (AD2) 41          
         P0.3 (AD3) 40          

        P1.5  7                 39  P0.4 (AD4)
        P1.6  8                 38  P0.5 (AD5)
        P1.7  9                 37  P0.6 (AD6)
         RST 10                 36  P0.7 (AD7)
  (RXD) P3.0 11                 35  EA/VPP
          NC 12                 34  NC
  (TXD) P3.1 13                 33  ALE/PROG
 (INT0) P3.2 14                 32  PSEN
 (INT1) P3.3 15                 31  P2.7 (A15)
   (T0) P3.4 16                 30  P2.6 (A14)
   (T1) P3.5 17                 29  P2.5 (A13)

              18  19  20  21  22  23  24  25  26  27  28
     (WR) P3.6                                      P2.4 (A12)
     (RD) P3.7                                  P2.3 (A11)
              XTAL2                          P2.2 (A10)
                  XTAL1                  P2.1 (A9)
                      GND            P2.0 (A8)
                          NC
```

Block Diagram

P0.0 - P0.7   P2.0 - P2.7

V_{CC}

GND

PORT 0 DRIVERS   PORT 2 DRIVERS

RAM ADDR. REGISTER → RAM

PORT 0 LATCH   PORT 2 LATCH   QUICK FLASH

B REGISTER   ACC   STACK POINTER   PROGRAM ADDRESS REGISTER

TMP2   TMP1   BUFFER

ALU   PC INCREMENTER

INTERRUPT, SERIAL PORT, AND TIMER BLOCKS   PROGRAM COUNTER

PSW

PSEN   TIMING AND CONTROL   INSTRUCTION REGISTER   DUAL DPTR

ALE/PROG

$\overline{EA}$ / V_{PP}

RST

WATCH DOG   PORT 1 LATCH   PORT 3 LATCH

OSC   PORT 1 DRIVERS   PORT 3 DRIVERS

P1.0 - P1.7   P3.0 - P3.7

Pin Description

VCC   Supply voltage.

GND   Ground.

Port 0   Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1   Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)

Port 2   Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3   Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89C55WD, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DIS-RTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89C55WD is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12V programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Table 4. AUXR1: Auxiliary Register 1

AUXR1	Address = A2H					Reset Value = XXXXXXX0B		
	Not Bit Addressable							
	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

–   Reserved for future expansion

DPS   Data Pointer Register Select

DPS

0   Selects DPTR Registers DP0L, DP0H

1   Selects DPTR Registers DP1L, DP1H

Timer 0 and 1

Timer 0 and Timer 1 in the AT89C55WD operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52.

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 2.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 5. Timer 2 Operating Modes

RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-Reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 5.

Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 6). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 5. Timer in Capture Mode
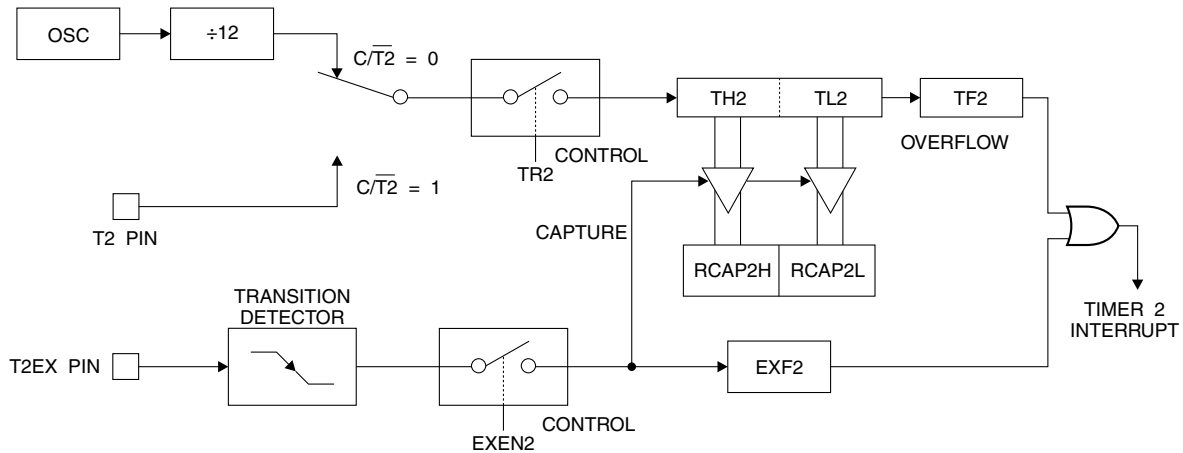
Figure 6 shows Timer 2 automatically counting up when DCEN=0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture ModeRCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 6. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 6. Timer 2 Auto Reload Mode (DCEN = 0)
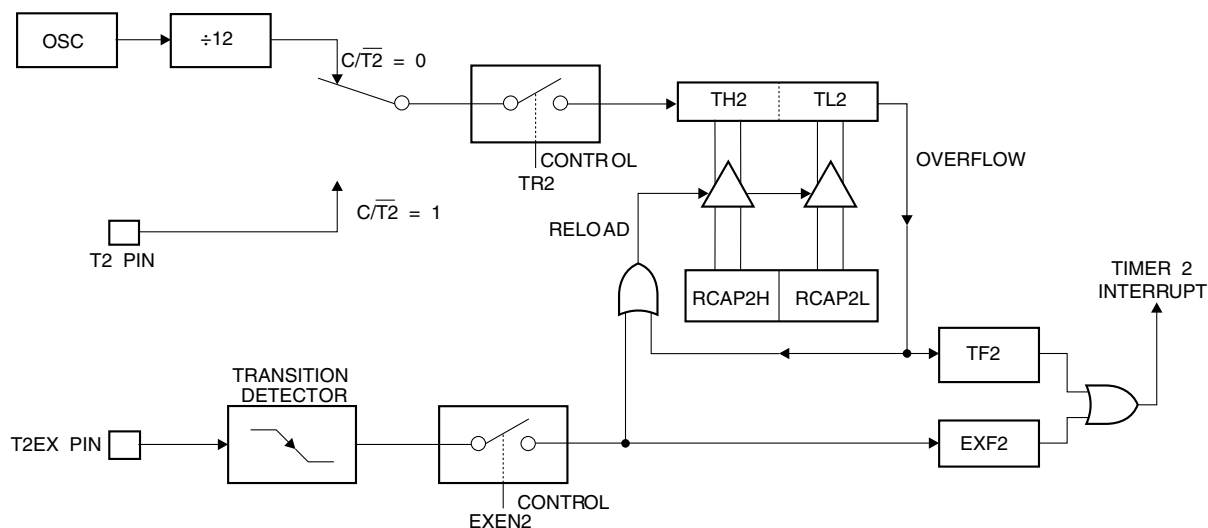
Table 6. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H						Reset Value = XXXX XX00B	
Not Bit Addressable							
–	–	–	–	–	–	T2OE	DCEN
7	6	5	4	3	2	1	0

(Bit)

Symbol	Function
–	Not implemented, reserved for future
T2OE	Timer 2 Output Enable bit
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter

Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 8.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation (CP/$\overline{\text{T2}}$ = 0). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536\text{-RCAP2H,RCAP2L)}]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 8. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

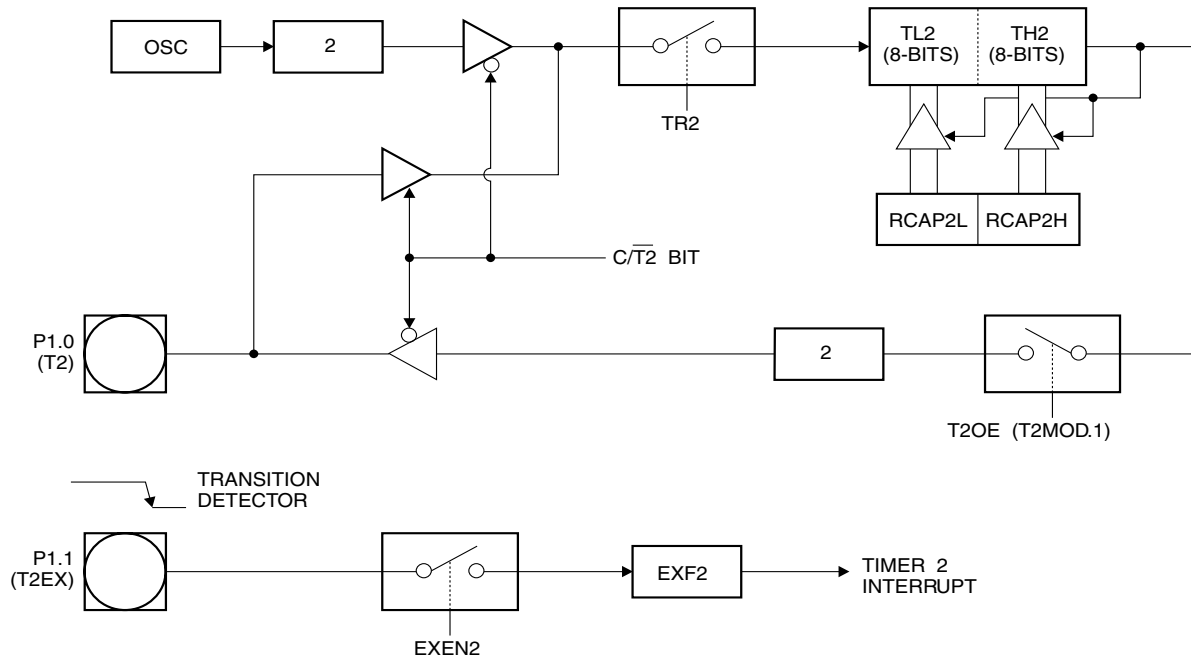**Figure 9.** Timer 2 in Clock-Out Mode

Table 7. Interrupt Enable (IE) Register

(MSB)						(LSB)	
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

Figure 10. Interrupt Sources
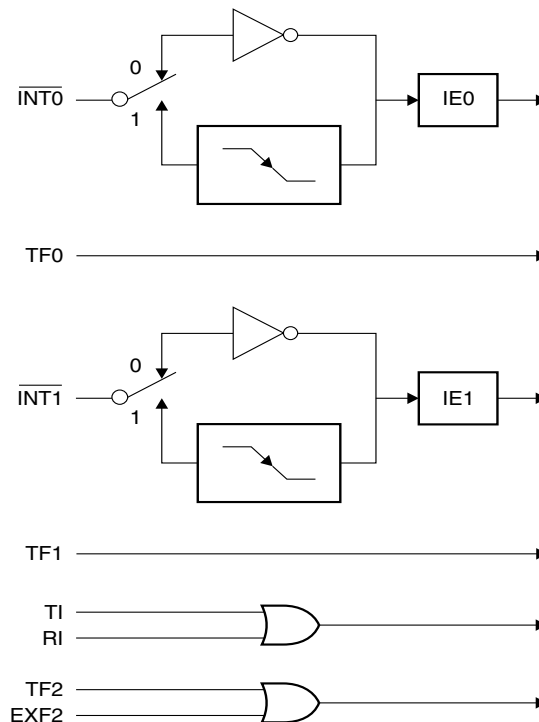
Figure 12. External Clock Drive Configuration
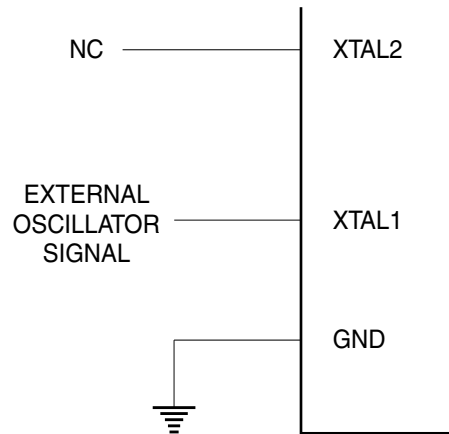
Table 8. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89C55WD has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 9. Lock Bit Protection Modes

	Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled.
3	P	P	U	Same as mode 2, but verify is also disabled.
4	P	P	P	Same as mode 3, but external execution is also disabled.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash

The AT89C55WD is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89C55WD code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89C55WD, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89C55WD, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}$/V$_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Chip Erase Sequence: Before the AT89C55WD can be reprogrammed, a Chip Erase operation needs to be performed. To erase the contents of the AT89C55WD, follow this sequence:

1. Raise V$_{CC}$ to 6.5V.
2. Pulse ALE/$\overline{PROG}$ once (duration of 200 - 500 ns).
3. Wait for 150 ms.
4. Power V$_{CC}$ down and up to 6.5V.
5. Pulse ALE/$\overline{PROG}$ once (duration of 200 - 500 ns).
6. Wait for 150 ms.
7. Power V$_{CC}$ down and up to 6.5V.

$\overline{Data}$ **Polling:** The AT89C55WD features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all out-

puts, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be directly verified by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(000H) = 1EH indicates manufactured by Atmel
(100H) = 55H
(200H) = 06H indicates 89C55WD

Programming Interface

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 10. Flash Programming Modes

Mode	V$_{CC}$	RST	$\overline{PSEN}$	ALE/ $\overline{PROG}$	$\overline{EA}$/ V$_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P3.4	P2.5-0	P1.7-0
													Address	
Write Code Data	5V	H	L	⎍ (1)	12V	L	H	H	H	H	D$_{IN}$	A14	A13-8	A7-0
Read Code Data	5V	H	L	H	H/12V	L	L	L	H	H	D$_{OUT}$	A14	A13-8	A7-0
Write Lock Bit 1	6.5V	H	L	⎍ (2)	12V	H	H	H	H	H	X	X	X	X
Write Lock Bit 2	6.5V	H	L	⎍ (2)	12V	H	H	H	L	L	X	X	X	X
Write Lock Bit 3	6.5V	H	L	⎍ (2)	12V	H	L	H	H	L	X	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X	X
Chip Erase	6.5V	H	L	⎍ (3)	12V	H	L	H	L	L	X	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X	XX 0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	55H	X	XX 0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X	XX 0010	00H

Notes: 1. Write Code Data requires a 200 ns $\overline{PROG}$ pulse.
         2. Write Lock Bits requires a 100 µs $\overline{PROG}$ pulse.
         3. Chip Erase requires a 200 ns - 500 ns $\overline{PROG}$ pulse.
         4. RDY/$\overline{BSY}$ signal is output on P3.0 during programming.
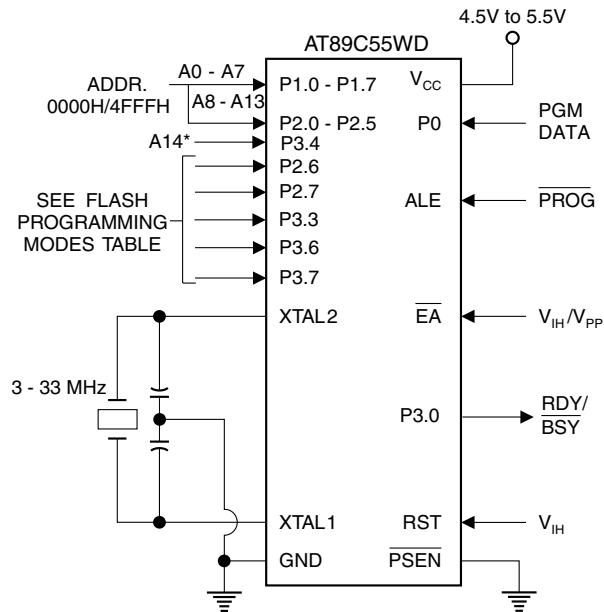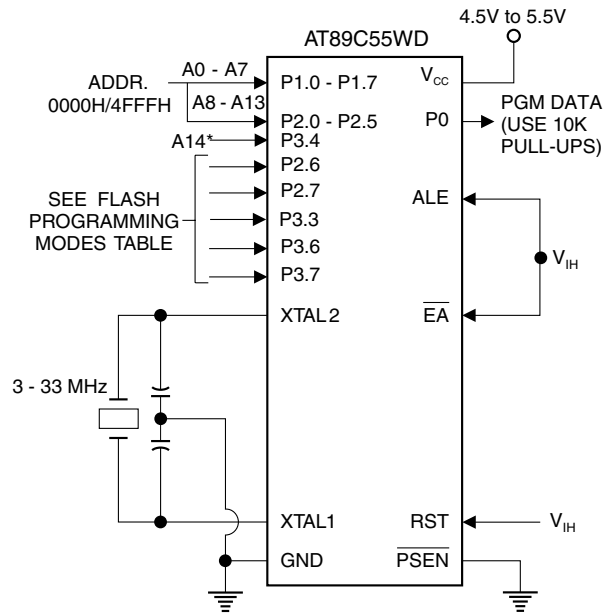
Figure 13. Programming the Flash Memory

Figure 14. Verifying the Flash Memory

Note: *Programming address line A14 (P3.4) is not the same as the external memory address line A14 (P2.6).

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Flash Programming and Verification Characteristics

T_A = 20°C to 30°C, V_{CC} = 4.5V to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		80	µs

Package Information

44A – TQFP
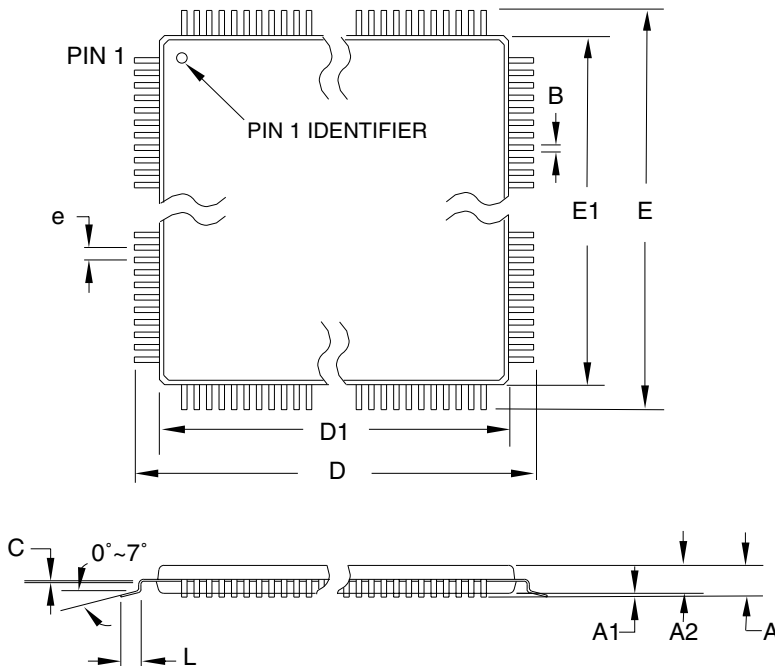
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes: 1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

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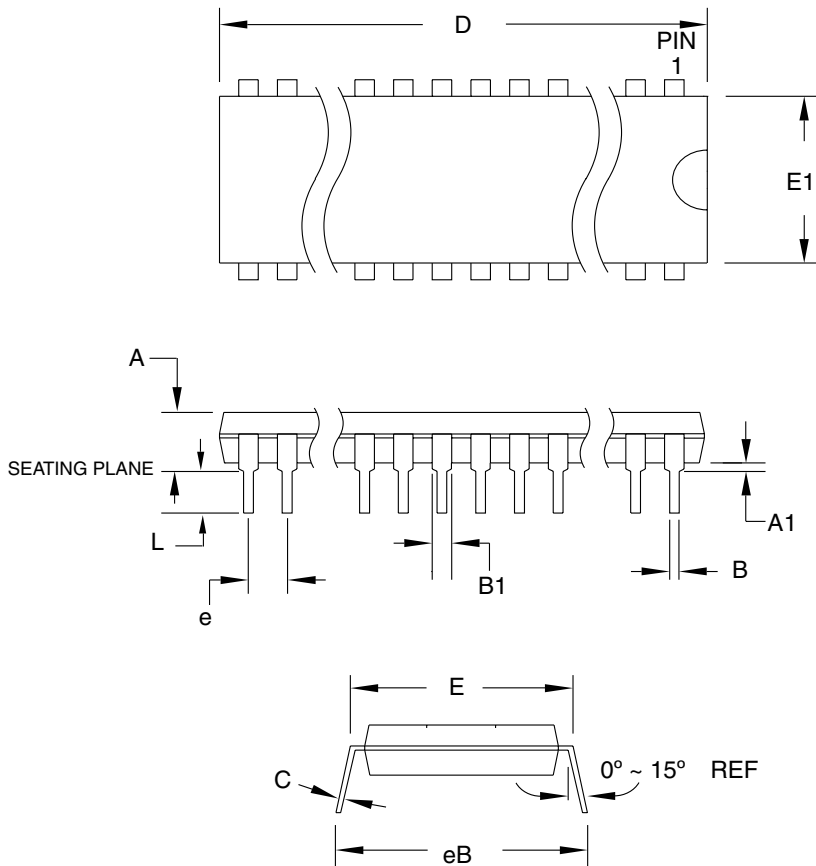|	TITLE	DRAWING NO.	REV.
AMEL 2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
AIMEL 2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

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