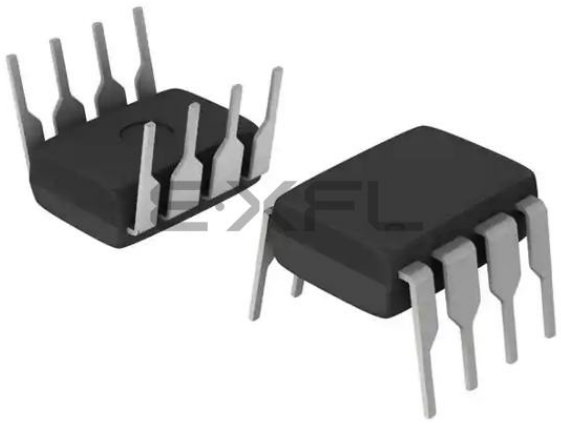

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f752-e-p

TABLE 3-1: SUMMARY OF REGISTERS ASSOCIATED WITH FLASH PROGRAM MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PMCON1	—	—	—	—	—	WREN	WR	RD	25
PMCON2	Program Memory Control Register 2								23*
PMADRL	PMADRL<7:0>								24
PMADRH	—	—	—	—	—	—	PMADRH<1:0>		24
PMDATL	PMDATL<7:0>								24
PMDATH	—	—	PMDATH<5:0>						24
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	15

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Flash program memory module.

* Page provides register information.

TABLE 3-2: SUMMARY OF CONFIGURATION WORD WITH FLASH PROGRAM MEMORY

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG	13:8	—	—	$\overline{\text{DEBUG}}$	$\overline{\text{CLKOUTEN}}$	WRT<1:0>		BOREN<1:0>		126
	7:0	—	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	—	—	FOSC0	

Legend: — = unimplemented location, read as '1'. Shaded cells are not used by Flash program memory.

5.4 PORTA Control Registers

REGISTER 5-2: PORTA: PORTA REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R-x/x	R/W-x/u	R/W-x/u	R/W-x/u
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RA<5:0>**: PORTA I/O Value bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to any PORTx register are written to the corresponding LATx register. Reads from any PORTx register, return the value present on that PORTx I/O pins.

REGISTER 5-3: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	R-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	TRISA5	TRISA4	TRISA3(1)	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bits(1)
1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

Note 1: TRISA3 always reads '1'.

REGISTER 5-4: LATA: PORTA DATA LATCH REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **LATA<5:4>**: PORTA Output Latch Value bits(1)

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **LATA<2:0>**: PORTA Output Latch Value bits(1)

Note 1: Writes to any PORTx register are written to the corresponding LATx register. Reads from any PORTx register, return the value present on that PORTx I/O pins.

5.5.2 WEAK PULL-UPS

Each of the PORTA pins, except RA3, has an individually configurable internal weak pull-up. Control bits WPUx enable or disable each pull-up. Refer to Register 5-9. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the RAPU bit of the OPTION_REG register). A weak pull-up is automatically enabled for RA3 when configured as MCLR and disabled when RA3 is an I/O. There is no software control of the MCLR pull-up.

REGISTER 5-6: WPUA: WEAK PULL-UP PORTA REGISTER (1,2)

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	WPU5	WPU4	WPU3(3)	WPU2	WPU1	WPU0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **WPU<5:0>:** Weak Pull-up Control bits
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global RAPU must be enabled for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISA = 0).
3: The RA3 pull-up is enabled when configured as MCLR in the Configuration Word, otherwise it is disabled as an input and reads as ‘0’.

5.5.3 SLEW RATE CONTROL

Two of the PORTA pins (RA0 and RA2) are equipped with high current driver circuitry. The SLRCONA register provides reduced slew rate control to mitigate possible EMI radiation from these pins.

REGISTER 5-7: SLRCONA: SLEW RATE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0
—	—	—	—	—	SLRA2	—	SLRA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**: Read as ‘0’

bit 2 **SLRA2:** Slew Rate Control bit
1 = Pin voltage slews at limited rate
0 = Pin voltage slews at maximum rate

bit 1 **Unimplemented**: Read as ‘0’

bit 0 **SLRA0:** Slew Rate Control bit
1 = Pin voltage slews at limited rate
0 = Pin voltage slews at maximum rate

REGISTER 11-3: COGxASD: COG AUTO-SHUTDOWN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
GxASDE	GxARSEN	GxASDL1	GxASDL0	GxASDSHLT	GxASDSC2	GxASDSC1	GxASDSFLT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **GxASDE:** Auto-Shutdown Event Status bit
1 = COG is in the shutdown state
0 = COG is not in the shutdown state

bit 6 **GxARSEN:** Auto-Restart Enable bit
1 = Auto-restart is enabled
0 = Auto-restart is disabled

bit 5 **GxASDL1:** COGxOUT1 Auto-shutdown Override Level bit
1 = A logic ‘1’ is placed on COGxOUT1 when a shutdown input is true
0 = A logic ‘0’ is placed on COGxOUT1 when a shutdown input is true

bit 4 **GxASDL0:** COGxOUT0 Auto-shutdown Override Level bit
1 = A logic ‘1’ is placed on COGxOUT0 when a shutdown input is true
0 = A logic ‘0’ is placed on COGxOUT0 when a shutdown input is true

bit 3 **GxASDSHLT:** COG Auto-shutdown Source Enable bit 3
1 = COG is shutdown when HLTMR equals HLTPR is low
0 = HLTimer1 pin has no effect on shutdown

bit 2 **GxASDSC2:** COG Auto-shutdown Source Enable bit 2
1 = COG is shutdown when C2OUT is low
0 = C2OUT pin has no effect on shutdown

bit 1 **GxASDSC1:** COG Auto-shutdown Source Enable bit 1
1 = COG is shutdown when C1OUT is low
0 = C1OUT pin has no effect on shutdown

bit 0 **GxASDSFLT:** COG Auto-shutdown Source Enable bit 0
1 = COG is shutdown when COGxFLT pin is low
0 = COGxFLT pin has no effect on shutdown

12.3 ADC Control Registers

REGISTER 12-1: ADCON0: A/D CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG	CHS<3:0>				GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Conversion Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **VCFG:** Voltage Reference bit
1 = V_{REF} pin
0 = V_{DD}

bit 5-2 **CHS<3:0>:** Analog Channel Select bits
0000 = Channel 00 (AN0)
0001 = Channel 01 (AN1)
0010 = Channel 02 (AN2)
0011 = Channel 03 (AN3)
0100 = Reserved. Do not use.
•
•
•
1101 = Reserved. Do not use.
1110 = Digital-to-Analog Converter (DAC output)
1111 = Fixed Voltage Reference (FVR)

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

13.5 FVR Control Registers

REGISTER 13-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

R/W-0/0	R-q/q	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
FVREN	FVRRDY	FVRBUFEN	FVRBUFSS	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **FVREN:** Fixed Voltage Reference Enable bit
0 = Fixed Voltage Reference is disabled
1 = Fixed Voltage Reference is enabled

bit 6 **FVRRDY:** Fixed Voltage Reference Ready Flag bit
0 = Fixed Voltage Reference output is not ready or not enabled bit
1 = Fixed Voltage Reference output is ready for use

bit 5 **FVRBUFEN:** Voltage Reference Output Pin Buffer Enable
0 = Output buffer is disabled
1 = Output buffer is enabled

bit 4 **FVRBUFSS:** Voltage Reference Pin Buffer Source Select bit
0 = Bandgap (1.2V) is the input to the output voltage buffer
1 = dac_out is the input to the output voltage buffer

bit 3-0 **Unimplemented:** Read as ‘0’

TABLE 13-1: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	FVRBUFEN	FVRBUFSS	—	—	—	—	101

Legend: Shaded cells are not used with the Fixed Voltage Reference.

TABLE 15-2: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1ZLF	C1SP	C1HYS	C1SYNC	113
CM1CON1	C1INTP	C1INTN	C1PCH<1:0>		—	—	—	C1NCH0	114
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2ZLF	C2SP	C2HYS	C2SYNC	113
CM2CON1	C2INTP	C2INTN	C2PCH<1:0>		—	—	—	C2NCH0	114
CMOUT	—	—	—	—	—	—	MCOUT2	MCOUT1	114
DACCON0	DACEN	DACRNG	DACOE	—	—	DACPSS0	—	—	105
DACCON1	—	—	—	DACR<4:0>					105
FVRCON	FVREN	FVRRDY	FVR-BUFEN	FVR-BUFSS	—	—	—	—	101
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	15
PIE2	—	—	C2IE	C1IE	—	COG1IE	—	CCP1IE	17
PIR2	—	—	C2IF	C1IF	—	COG1IF	—	CCP1IF	19
TRISA	—	—	TRISA5	TRISA4	TRISA3(1)	TRISA2	TRISA1	TRISA0	40
ANSELA	—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0	41

Legend: — = unimplemented location, read as '0'. Shaded cells are unused by the comparator module.

Note 1: TRISA3 always reads '1'.

RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.
Words:	1
Cycles:	2
Example:	`RETFIE` After Interrupt PC = TOS GIE = 1

RETLW	Return with literal in W
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.
Words:	1
Cycles:	2

Example:	`CALL TABLE;W contains`
	`;table offset`
	`;value`
	`GOTO DONE`
	`TABLE` •
	•
	`ADDWF PC ;W = offset`
	`RETLW k1 ;Begin table`
	`RETLW k2 ;`
	•
	•
	•
	`RETLW kn ;End of table`
	`DONE`
	Before Instruction
	W = 0x07
	After Instruction
	W = value of k8

RETURN	Return from Subroutine
Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

17.3.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in Reset until V_{DD} has reached a high enough level for proper operation. To take advantage of the POR, simply connect the $\overline{MCLR}$ pin through a resistor to V_{DD}. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for V_{DD} is required. See **Section 20.0 "Electrical Specifications"** for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until V_{DD} reaches V_{BOR} (see **Section 17.3.4 "Brown-out Reset (BOR)"**).

Note:	The POR circuit does not produce an internal Reset when V_{DD} declines. To re-enable the POR, V_{DD} must reach Vss for a minimum of 100 μs.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure proper operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00000607).

17.3.2 $\overline{MCLR}$

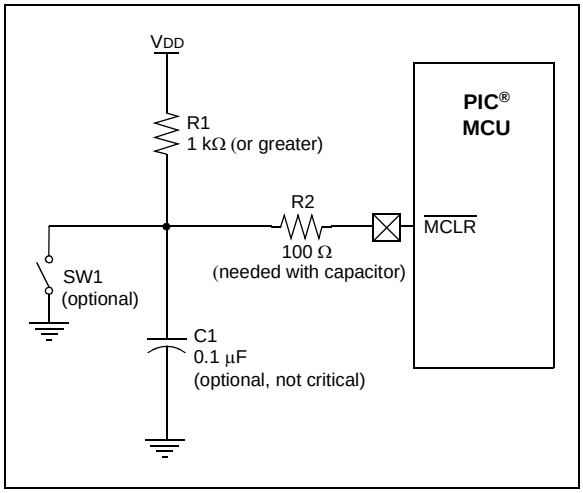
PIC12F752/HV752 has a noise filter in the $\overline{MCLR}$ Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{MCLR}$ pin low.

Voltages applied to the $\overline{MCLR}$ pin that exceed its specification can result in both $\overline{MCLR}$ Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the $\overline{MCLR}$ pin no longer be tied directly to V_{DD}. The use of an RC network, as shown in Figure 17-2, is suggested.

An internal $\overline{MCLR}$ option is enabled by clearing the MCLRE bit in the Configuration Word register. When MCLRE = 0, the Reset signal to the chip is generated internally. When the MCLRE = 1, the $\overline{MCLR}$ pin becomes an external Reset input. In this mode, the $\overline{MCLR}$ pin has a weak pull-up to V_{DD}.

FIGURE 17-2: RECOMMENDED $\overline{MCLR}$ CIRCUIT



17.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from an internal RC oscillator. For more information, see **Section 4.2.2 "Internal Clock Mode"**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level. A Configuration bit, $\overline{PWRTE}$, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip due to:

- V_{DD} variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 20.0 "Electrical Specifications"**).

Note:	Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

17.3.5 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

- PWRT time-out is invoked after POR has expired
- OST is activated after the PWRT time-out has expired

The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in EC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 17-4, Figure 17-5 and Figure 17-6 depict time-out sequences.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then, bringing MCLR high will begin execution immediately (see Figure 17-5). This is useful for testing purposes or to synchronize more than one PIC12F752/HV752 device operating in parallel.

Table 17-5 shows the Reset conditions for some special registers, while Table 17-4 shows the Reset conditions for all the registers.

17.3.6 POWER CONTROL (PCON) REGISTER

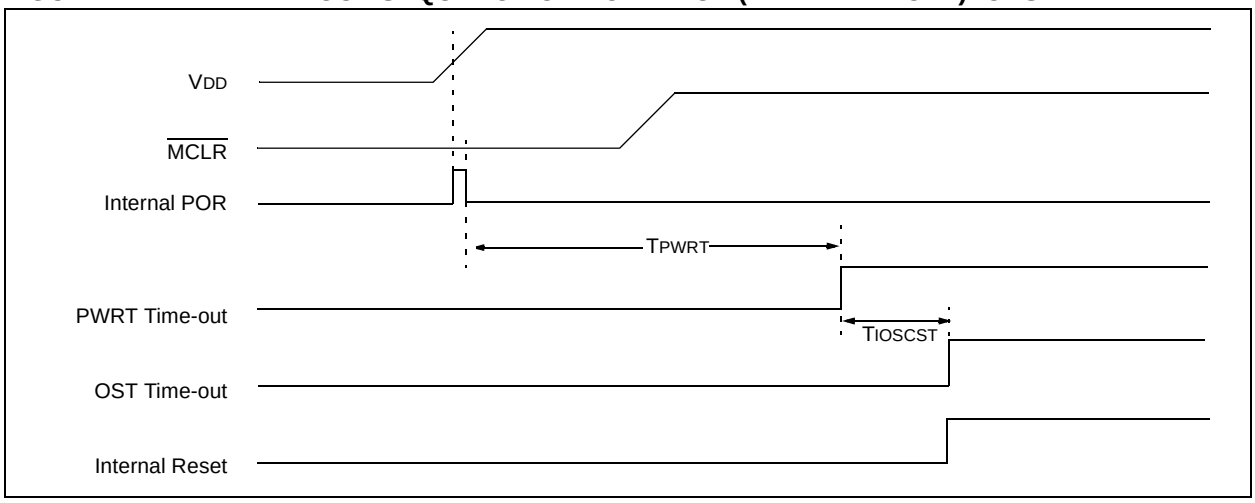
The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset occurred last.

Bit 0 is BOR (Brown-out). BOR is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if BOR = 0, indicating that a Brown-out has occurred. The BOR Status bit is a “don’t care” and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is POR (Power-on Reset). It is a ‘0’ on Power-on Reset and unaffected otherwise. The user must write a ‘1’ to this bit following a Power-on Reset. On a subsequent Reset, if POR is ‘0’, it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see **Section 17.3.4 “Brown-out Reset (BOR)”**.

FIGURE 17-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR): CASE 1



17.5 Context Saving during Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Temporary holding registers W_TEMP and STATUS_TEMP should be placed in the last 16 bytes of GPR (see Figure 2-1). These 16 locations are common to all banks and do not require banking. This makes context save and restore operations simpler. The code shown in Example 17-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register.

Note: The PIC12F752/HV752 does not require saving the PCLATH. However, if computed GOTOs are used in both the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 17-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP              ;Copy W to TEMP register
SWAPF   STATUS,W            ;Swap status to be saved into W
                            ;Swaps are used because they do not affect the status bits
MOVWF   STATUS_TEMP         ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                      ;Insert user code here
:
SWAPF   STATUS_TEMP,W       ;Swap STATUS_TEMP register into W
                            ;(sets bank to original state)
MOVWF   STATUS              ;Move W into STATUS register
SWAPF   W_TEMP,F            ;Swap W_TEMP
SWAPF   W_TEMP,W            ;Swap W_TEMP into W
```

TABLE 17-7: WDT STATUS

Conditions	WDT
WDTE = 0	Cleared
CLRWDT Command	
Exit Sleep	

TABLE 17-8: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS<2:0>			49

Legend: Shaded cells are not used by the Watchdog Timer.

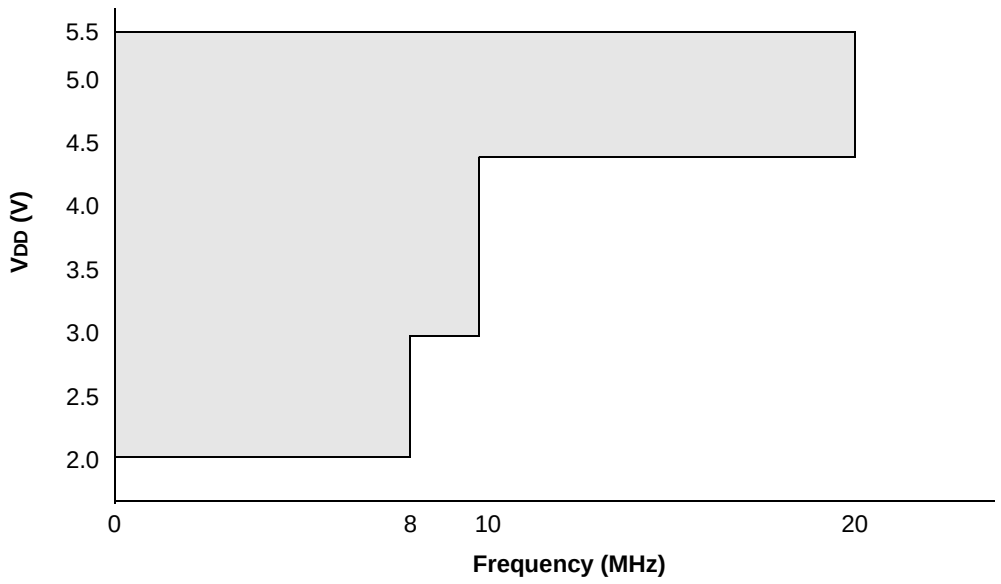
Note 1: See Register 17-1 for operation of all Configuration Word register bits.

TABLE 17-9: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG	13:8	—	—	$\overline{\text{DEBUG}}$	$\overline{\text{CLKOUTEN}}$	WRT<1:0>		BOREN<1:0>		126
	7:0	—	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	—	—	FOSC0	

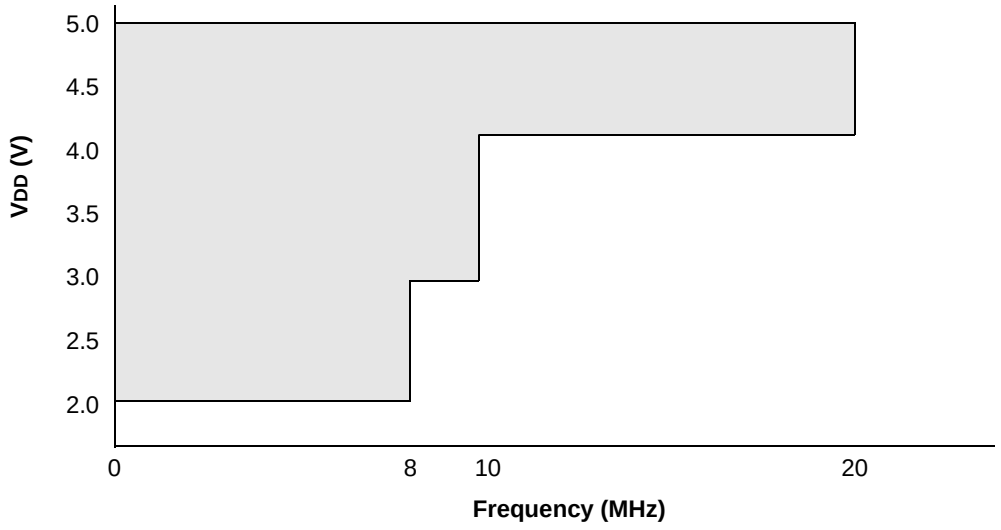
Legend: — = unimplemented location, read as '1'. Shaded cells are not used by Watchdog Timer.

FIGURE 20-1: PIC12F752 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 20-2: PIC12HV752 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

TABLE 20-3: POWER-DOWN CURRENTS (I_{PD}) (1,2)

PIC12F752		Standard Operating Conditions (unless otherwise stated) Sleep mode						
PIC12HV752								
Param. No.	Device Characteristics	Min.	Typ.†	Max. 85°C	Max. 125°C	Units	Conditions	
							V_{DD}	Note
	Power-down Base Current (I_{PD})(2)							
D020		—	0.05	1.2	4.5	µA	2.0	WDT, BOR, Comparator, V_{REF} and T1OSC disabled
		—	0.15	1.6	5.5	µA	3.0	
		—	0.35	2.1	9	µA	5.0	
D020		—	135	200	200	µA	2.0	
		—	210	280	280	µA	3.0	
		—	260	350	350	µA	4.5	
	Power-down Base Current (I_{PD})(2, 3)							
D021		—	0.5	1.5	5	µA	2.0	WDT Current(1)
		—	2.5	4	8	µA	3.0	
		—	9.5	17	19	µA	5.0	
D021		—	135	200	200	µA	2.0	
		—	210	285	285	µA	3.0	
		—	265	360	360	µA	4.5	
D022		—	5	9	15	µA	3.0	BOR Current(1)
		—	6	12	19	µA	5.0	
D022		—	215	285	285	µA	3.0	
		—	265	360	360	µA	4.5	
D023		—	160	235	245	µA	2.0	CxSP = 1, Comparator Current(1), single comparator enabled
		—	180	270	280	µA	3.0	
		—	220	350	360	µA	5.0	
D023		—	280	415	415	µA	2.0	
		—	385	540	540	µA	3.0	
		—	455	735	735	µA	4.5	
D024		—	50	70	75	µA	2.0	CxSP = 0, Comparator Current(1), single comparator enabled
		—	55	80	90	µA	3.0	
		—	70	90	120	µA	5.0	
D024		—	185	205	205	µA	2.0	
		—	265	315	315	µA	3.0	
		—	320	445	445	µA	4.5	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral Δ current can be determined by subtracting the base I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: Shunt regulator is always on and always draws operating current.

FIGURE 21-3: IDD TYPICAL, HFINTOSC, PIC12F752 ONLY

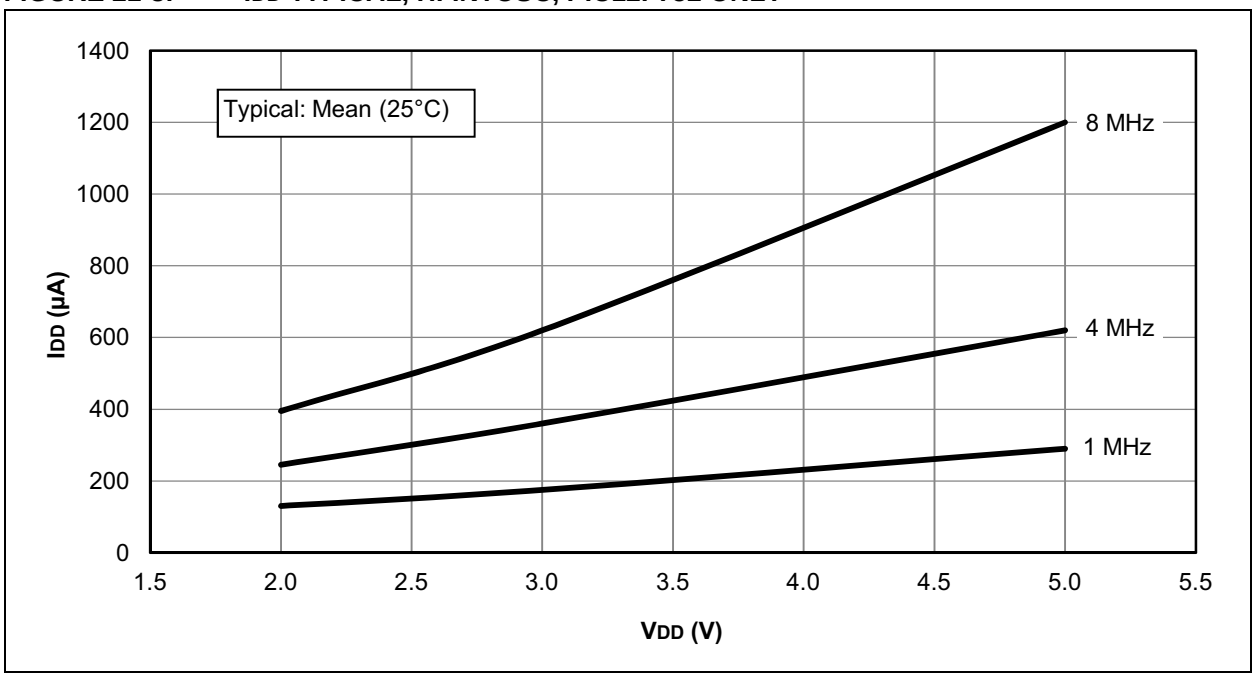


FIGURE 21-4: IDD MAXIMUM, HFINTOSC, PIC12F752 ONLY

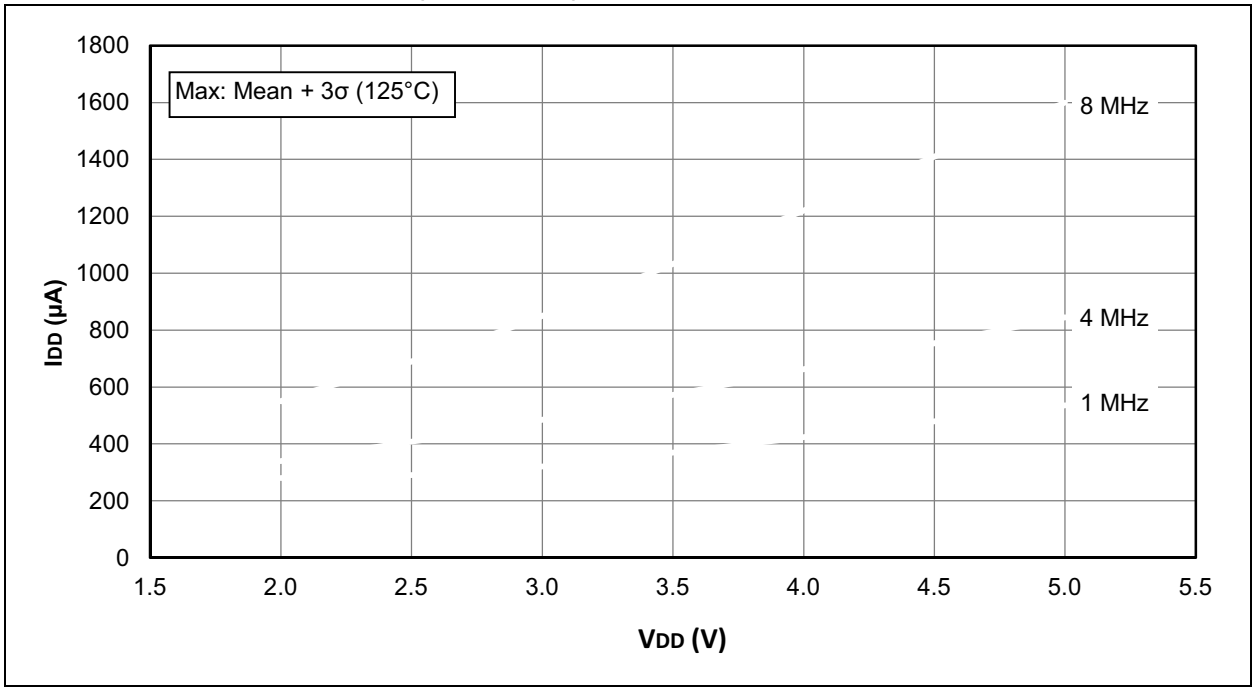


FIGURE 21-22: IPD, DAC, PIC12F752 ONLY

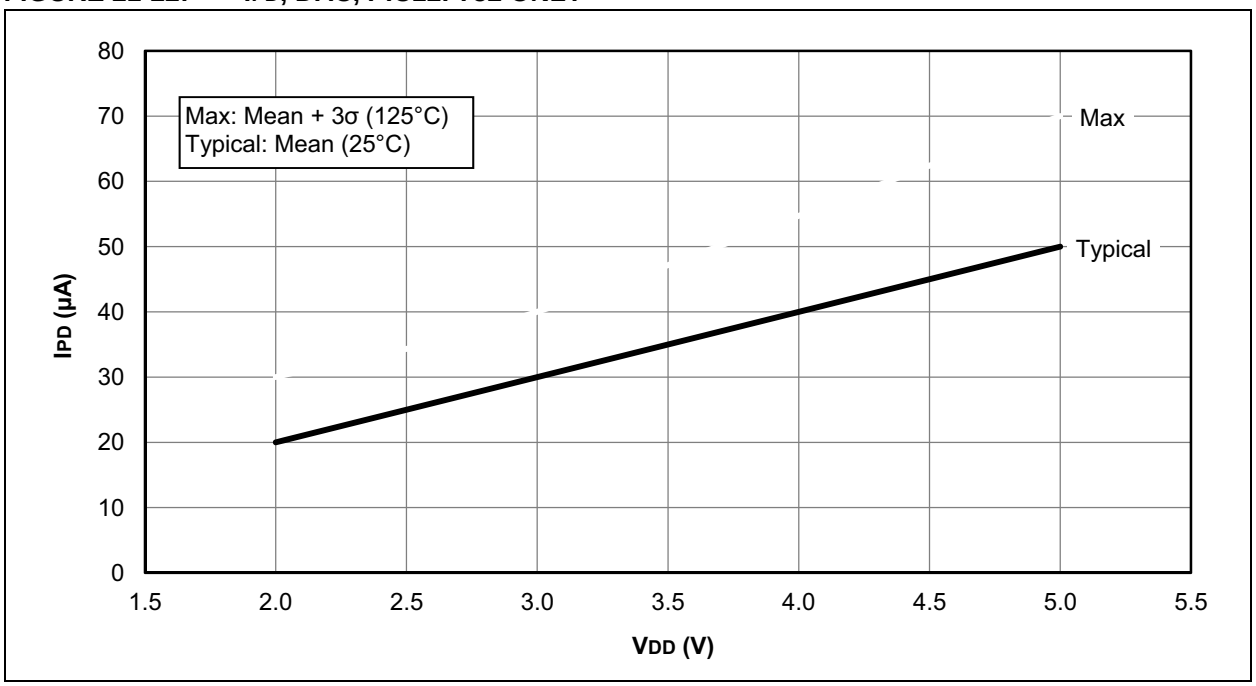


FIGURE 21-23: IPD, DAC, PIC12HV752 ONLY

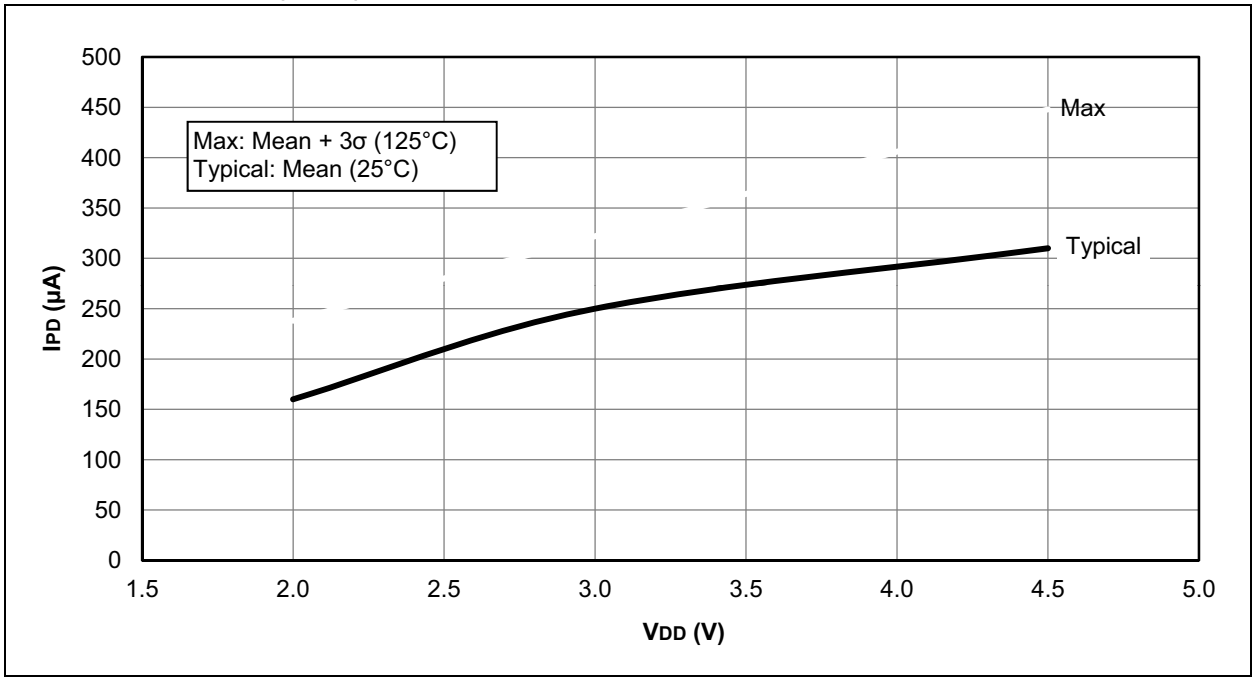


FIGURE 21-24: IPD, COMPARATOR, LOW-POWER MODE, CxSP = 0, PIC12F752 ONLY

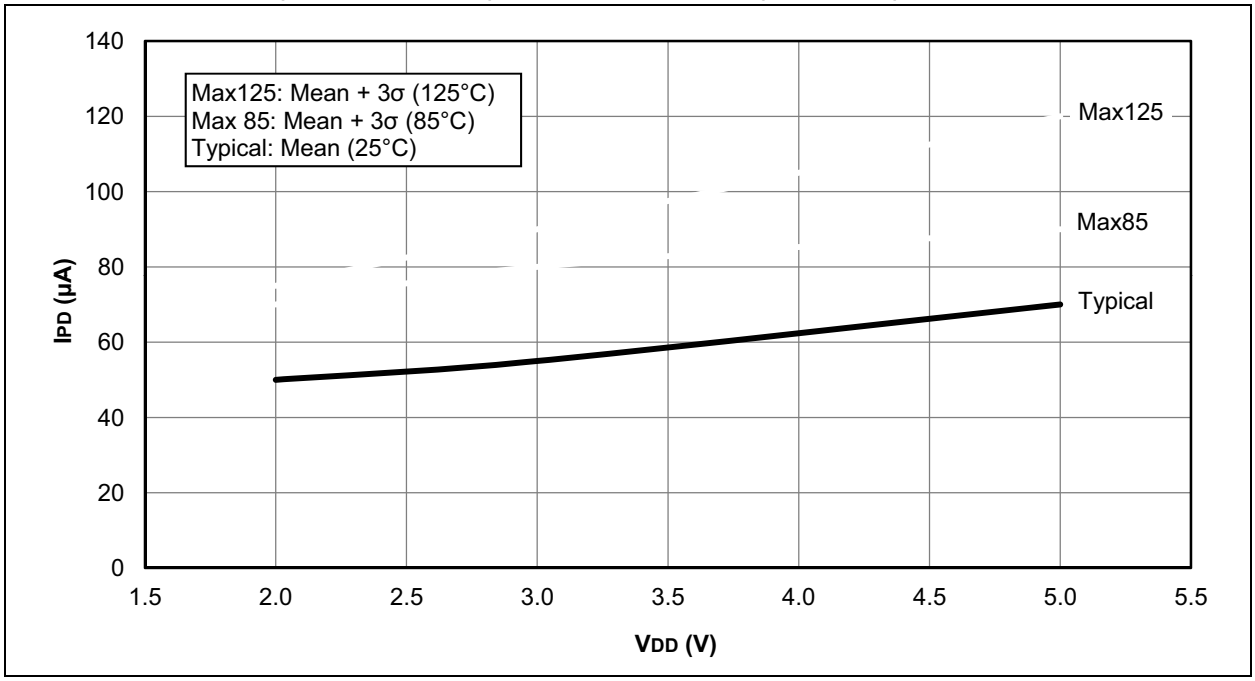


FIGURE 21-25: IPD, COMPARATOR, LOW-POWER MODE, CxSP = 0, PIC12HV752 ONLY