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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f752-e-sn

1.0 DEVICE OVERVIEW

The PIC12F752/HV752 devices are covered by this data sheet. They are available in 8-pin PDIP, SOIC and DFN packages.

Block Diagrams and pinout descriptions of the devices are in Figure 1-1 and Table 1-1.

FIGURE 1-1: PIC12F752/HV752 BLOCK DIAGRAM

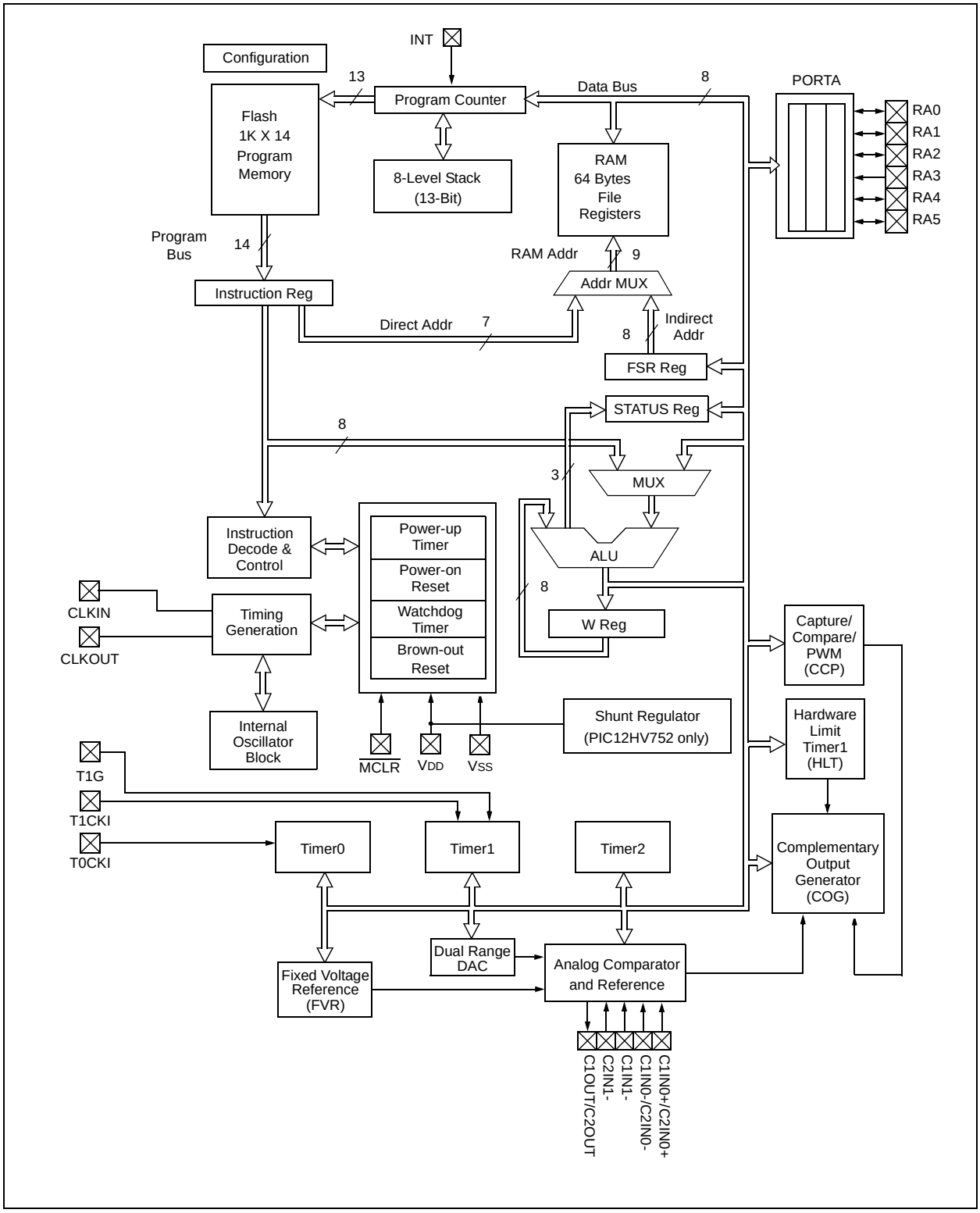


TABLE 2-4: PIC12F752/HV752 SPECIAL REGISTERS SUMMARY BANK 2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR Reset	Value on all other Resets(1)
Bank 2											
100h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
101h	TMR0	Holding Register for the 8-bit Timer0 Register								xxxx xxxx	uuuu uuuu
102h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
103h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
104h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
105h	LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	--xx -xxx	--uu -uuu
106h	—	Unimplemented								—	—
107h	—	Unimplemented								—	—
108h	IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	--00 0000	--00 0000
109h	—	Unimplemented								—	—
10Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	---0 0000
10Bh	INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF(2)	0000 0000	0000 0000
10Ch	WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	--00 0000	--00 0000
10Dh	SLRCONA	—	—	—	—	—	SLRA2	—	SLRA0	---- -0-0	---- -0-0
10Eh	—	Unimplemented								—	—
10Fh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	---- --uu
110h	TMR2	Holding Register for the 8-bit Timer2 Register								0000 0000	0000 0000
111h	PR2	Timer2 Period Register								1111 1111	1111 1111
112h	T2CON	—	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000	-000 0000
113h	HLTMR1	Holding Register for the 8-bit Hardware Limit Timer1 Register								0000 0000	0000 0000
114h	HLTPR1	Hardware Limit Timer1 Period Register								1111 1111	1111 1111
115h	HLT1CON0	—	H1OUTPS<3:0>				H1ON	H1CKPS<1:0>		-000 0000	-000 0000
116h	HLT1CON1	—	—	—	H1ERS<2:0>			H1FEREN	H1REREN	---0 0000	---0 0000
117h to 11Fh	—	Unimplemented								—	—

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition shaded = unimplemented

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: MCLR and WDT Reset does not affect the previous value data latch. The IOCIF bit will be cleared upon Reset but will set again if the mismatch exists.

2.3.2 OPTION REGISTER

The OPTION register is a readable and writable register, which contains various control bits to configure:

- Timer0/WDT Prescaler
- External RA2/INT Interrupt
- Timer0
- Weak Pull-ups on PORTA

Note: To achieve a 1:1 prescaler assignment for Timer0, assign the prescaler to the WDT by setting PSA bit to '1' of the OPTION register. See **Section 6.1.3 "Software Programmable Prescaler"**.

REGISTER 2-2: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{RAPU}$	INTEDG	T0CS	T0SE	PSA	PS<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{RAPU}$:** PORTA Pull-up Enable bit
1 = PORTA pull-ups are disabled
0 = PORTA pull-ups are enabled by individual PORT latch values

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

BIT VALUE	TIMER0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

2.3.7 PIR2 REGISTER

The PIR2 register contains the Peripheral Interrupt flag bits, as shown in Register 2-7.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-7: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 1

U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0
—	—	C2IF	C1IF		COG1IF	—	CCP1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **C2IF:** Comparator 1 Interrupt Flag bit
1 = Comparator output (C2OUT bit) has changed (must be cleared in software)
0 = Comparator output (C2OUT bit) has not changed

bit 4 **C1IF:** Comparator 1 Interrupt Flag bit
1 = Comparator output (C1OUT bit) has changed (must be cleared in software)
0 = Comparator output (C1OUT bit) has not changed

bit 3 **Unimplemented:** Read as '0'

bit 2 **COG1IF:** COG 1 Interrupt Flag bit
1 = COG1 has generated an auto-shutdown interrupt
0 = COG1 has NOT generated an auto-shutdown interrupt

bit 1 **Unimplemented:** Read as '0'

bit 0 **CCP1IF:** ECCP Interrupt Flag bit

Capture Mode
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred

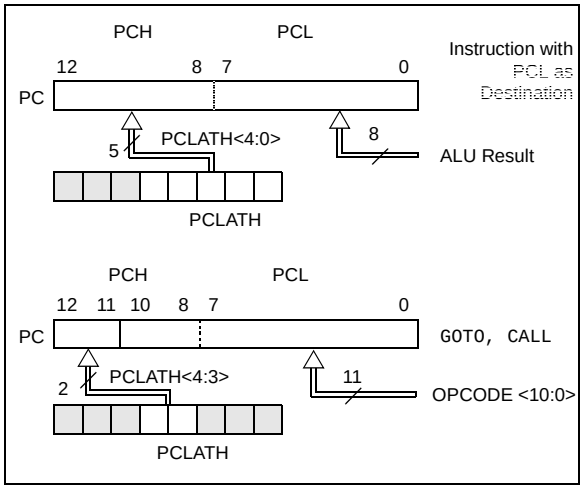
Compare Mode
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred

PWM mode
Unused in this mode

2.4 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-2 shows the two situations for the loading of the PC. The upper example in Figure 2-2 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-2 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-2: LOADING OF PC IN DIFFERENT SITUATIONS



2.4.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper five bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). Care should be exercised when jumping into a look-up table or program branch table (computed GOTO) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower eight bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, "*Implementing a Table Read*" (DS00556).

2.4.2 STACK

The PIC12F752/HV752 Family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1:	There are no Status bits to indicate Stack Overflow or Stack Underflow conditions.
2:	There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.5 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit of the STATUS register, as shown in Figure 2-3.

A simple program to clear RAM location 40h-7Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
        MOVLW   0x40    ;initialize pointer
        MOVWF   FSR     ;to RAM
NEXT    CLRF    INDF    ;clear INDF register
        INCF    FSR     ;inc pointer
        BTFSS   FSR,7   ;all done?
        GOTO    NEXT    ;no clear next
CONTINUE                ;yes continue
```

6.2 Option and Timer0 Control Register

REGISTER 6-1: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{RAPU}}$:** PORTA Pull-up Enable bit
1 = PORTA pull-ups are disabled
0 = PORTA pull-ups are enabled by individual PORT latch values in WPU register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
TMR0	Holding Register for the 8-bit Timer0 Register								47*
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	15
OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS<2:0>			14
TRISA	—	—	TRISA5	TRISA4	TRISA3(1)	TRISA2	TRISA1	TRISA0	40

Legend: — Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.
* Page provides register information.

Note 1: TRISA3 always reads '1'.

7.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

7.4 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If external clock source is selected, then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 7.4.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

7.4.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read, which is taken care of in hardware. However, the user should keep in mind that reading the 16-bit timer in two 8-bit values poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

7.5 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 gate count enable.

Timer1 gate can also be driven by multiple selectable sources.

7.5.1 TIMER1 GATE COUNT ENABLE

The Timer1 gate is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 gate is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate (T1G) input is active, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 gate input is inactive, no incrementing will occur and Timer1 will hold the current count. See Figure 7-3 for timing details.

TABLE 7-3: TIMER1 GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer1 Operation
↑	0	0	Counts
↑	0	1	Holds Count
↑	1	0	Holds Count
↑	1	1	Counts

9.0 HARDWARE LIMIT TIMER (HLT) MODULE

The Hardware Limit Timer (HLT) module is a version of the Timer2-type modules. In addition to all the Timer2-type features, the HLT can be reset on rising and falling events from selected peripheral outputs.

The HLT primary purpose is to act as a timed hardware limit to be used in conjunction with asynchronous analog feedback applications. The external reset source synchronizes the HLTMR1 to an analog application.

In normal operation, the external reset source from the analog application should occur before the HLTMR1 matches the HLTPR1. This resets HLTMR1 for the next period and prevents the HLTimer1 Output from going active.

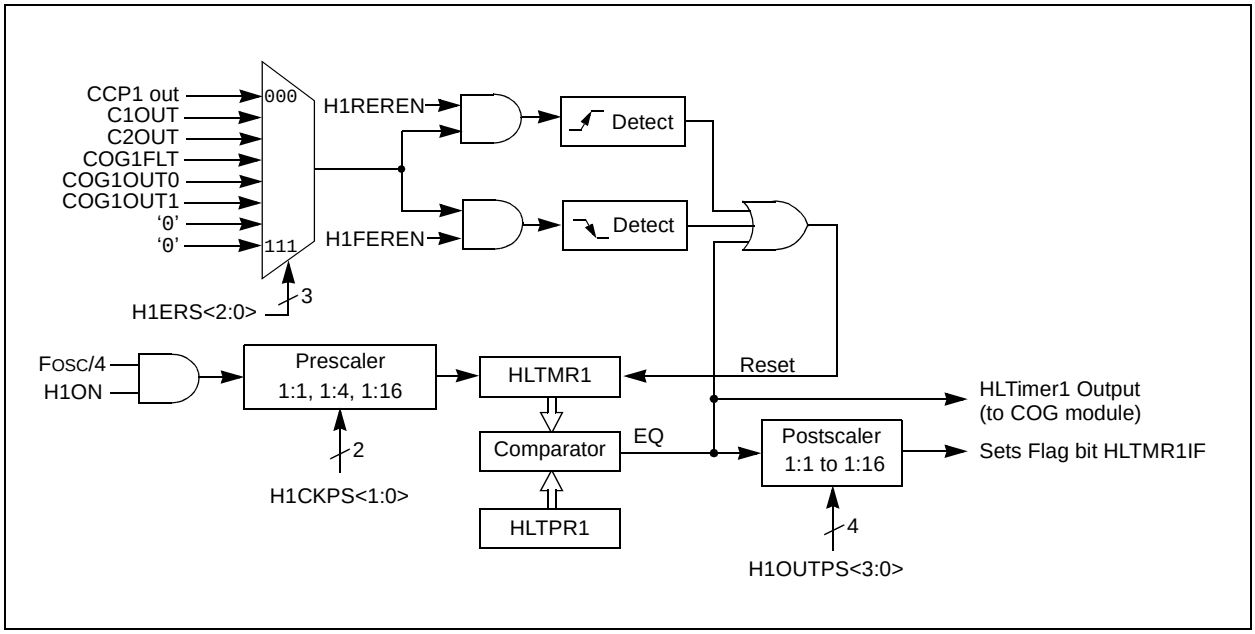
When the external reset source fails to generate a signal within the expected time, allowing the HLTMR1 to match the HLTPR1, then the HLTimer1 Output becomes active.

The HLT module incorporates the following features:

- 8-Bit Read-Write Timer Register (HLTMR1)
- 8-Bit Read-Write Period Register (HLTPR1)
- Software Programmable Prescaler
  - 1:1
  - 1:4
  - 1:16
- Software Programmable Postscaler:
  - 1:1 to 1:16, inclusive
- Interrupt on HLTMR1 Match with HLTPR1
- Eight Selectable Timer Reset Inputs (five reserved)
- Reset on Rising and Falling Event

Refer to Figure 9-1 for a block diagram of the HLT.

FIGURE 9-1: HLTMR1 BLOCK DIAGRAM



10.4 CCP Control Registers

REGISTER 10-1: CCP1CON: CCP1 CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	DC1B<1:0>		CCP1M<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DC1B<1:0>:** PWM Duty Cycle Least Significant bits

Capture mode:
Unused

Compare mode:
Unused

PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0 **CCP1M<3:0>:** CCP1 Mode Select bits

0000 = Capture/Compare/PWM off (resets CCP1 module)
0001 = Reserved
0010 = Compare mode: toggle output on match
0011 = Reserved

0100 = Capture mode: every falling edge
0101 = Capture mode: every rising edge
0110 = Capture mode: every 4th rising edge
0111 = Capture mode: every 16th rising edge

1000 = Compare mode: initialize CCP1 pin low; set output on compare match (set CCP1IF)
1001 = Compare mode: initialize CCP1 pin high; clear output on compare match (set CCP1IF)
1010 = Compare mode: generate software interrupt only; CCP1 pin reverts to I/O state
1011 = Compare mode: Special Event Trigger (CCP1 resets Timer, sets CCP1IF bit, and starts A/D conversion if A/D module is enabled)
11xx = PWM mode

11.7 Phase Delay

It is possible to delay the assertion of the rising event. This is accomplished by placing a non-zero value in COGxPH register. Refer to Register 11-6 and Figure 11-3 for COG operation with CCP1 and phase delay. The delay from the input rising event signal switching to the actual assertion of the events is calculated the same as the dead-band and blanking delays. Please see Equation 11-1.

When the COGxPH value is '0', phase delay is disabled and the phase delay counter output is true, thereby, allowing the event signal to pass straight through to complementary output driver flop.

11.7.1 CUMULATIVE UNCERTAINTY

It is not possible to create more than one COG_clock of uncertainty by successive stages. Consider that the phase delay stage comes after the blanking stage, the dead-band stage comes after either the blanking or phase delay stages, and the blanking stage comes after the dead-band stage. When the preceding stage is enabled, the output of that stage is necessarily synchronous with the COG_clock, which removes any possibility of uncertainty in the succeeding stage.

EQUATION 11-1: PHASE, DEAD-BAND, AND BLANKING TIME CALCULATION

$$T_{\text{min}} = \frac{\text{Count}}{F_{COG\_clock}}$$

$$T_{\text{max}} = \frac{\text{Count} + 1}{F_{COG\_\text{clock}}}$$

$$T_{\text{uncertainty}} = T_{\text{max}} - T_{\text{min}}$$

Also:

$$T_{\text{uncertainty}} = \frac{1}{F_{COG\_\text{clock}}}$$

Where:

T	Count
Phase Delay	GxPH<3:0>
Rising Dead Band	GxDBR<3:0>
Falling Dead Band	GxDBF<3:0>
Rising Event Blanking	GxBLKR<3:0>
Falling Event Blanking	GxBLKF<3:0>

EXAMPLE 11-1: TIMER UNCERTAINTY

Given:

$$Count = Ah = 10d$$
$$F_{COG\_\text{Clock}} = 8\text{MHz}$$

Therefore:

$$T_{\text{uncertainty}} = \frac{1}{F_{COG\_\text{clock}}} = \frac{1}{8MHz} = 125ns$$

Proof:

$$T_{\text{min}} = \frac{Count}{F_{COG\_\text{clock}}} = 125ns \bullet 10d = 1.25\mu s$$

$$T_{\text{max}} = \frac{Count + 1}{F_{COG\_\text{clock}}} = 125ns \bullet (10d + 1) = 1.375\mu s$$

Therefore:

$$T_{\text{uncertainty}} = T_{\text{max}} - T_{\text{min}} = 1.375\mu s - 1.25\mu s = 125ns$$

REGISTER 11-2: COGxCON1: COG CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
GxFSIM	GxRSIM	GxFS<2:0>			GxRS<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **GxFSIM:** COGx Falling Source Input Mode bit
1 = Input is edge sensitive
0 = Input is level sensitive

bit 6 **GxRSIM:** COGx Rising Source Input Mode bit
1 = Input is edge sensitive
0 = Input is level sensitive

bit 5-3 **GxFS<2:0>:** COGx Falling Source Select bits
111 = COGxFLT or HLTimer1
110 = CCP1 or HLTimer1
101 = C2OUT or HLTimer1
100 = C1OUT or HLTimer1
011 = COGxFLT
010 = CCP1
001 = C2OUT
000 = C1OUT

bit 2-0 **GxRS<2:0>:** COGx Rising Source Select bits
111 = COGxFLT or HLTimer1
110 = CCP1 or HLTimer1
101 = C2OUT or HLTimer1
100 = C1OUT or HLTimer1
011 = COGxFLT
010 = CCP1
001 = C2OUT
000 = C1OUT

12.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
   - Disable pin output driver (See TRIS register)
   - Configure pin as analog
2. Configure the ADC module:
   - Select ADC conversion clock
   - Configure voltage reference
   - Select ADC input channel
   - Select result format
   - Turn on ADC module
3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable peripheral interrupt
   - Enable global interrupt**(1)**
4. Wait the required acquisition time**(2)**
5. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit
6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO/$\overline{\text{DONE}}$ bit
   - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled)

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: See **Section 12.4 "A/D Acquisition Requirements"**.

EXAMPLE 12-1: A/D CONVERSION

```
;This code block configures the ADC
;for polling, Vdd reference, Frc clock
;and RA0 input.
;
;Conversion start & polling for completion
; are included.
;
  BANKSEL  TRISA       ;
  BSF      TRISA,0     ;Set RA0 to input
  BANKSEL  ADCON1      ;
  MOVLW    B'01110000' ;ADC Frc clock,
  IORWF    ADCON1      ; and RA0 as analog
  BANKSEL  ADCON0      ;
  MOVLW    B'10000001' ;Right justify,
  MOVWF    ADCON0      ;Vdd Vref, AN0, On
  CALL     SampleTime  ;Acquisiton delay
  BSF      ADCON0,GO   ;Start conversion
TEST AGAIN
  BTFSC    ADCON0,GO   ;Is conversion done?
  GOTO     TEST AGAIN  ;No, test again
  BANKSEL  ADRESH      ;
  MOVF     ADRESH,W    ;Read upper 2 bits
  MOVWF    RESULTHI    ;Store in GPR space
  BANKSEL  ADRESL      ;
  MOVF     ADRESL,W    ;Read lower 8 bits
  MOVWF    RESULTLO    ;Store in GPR space
```

15.11 Analog Input Connection Considerations

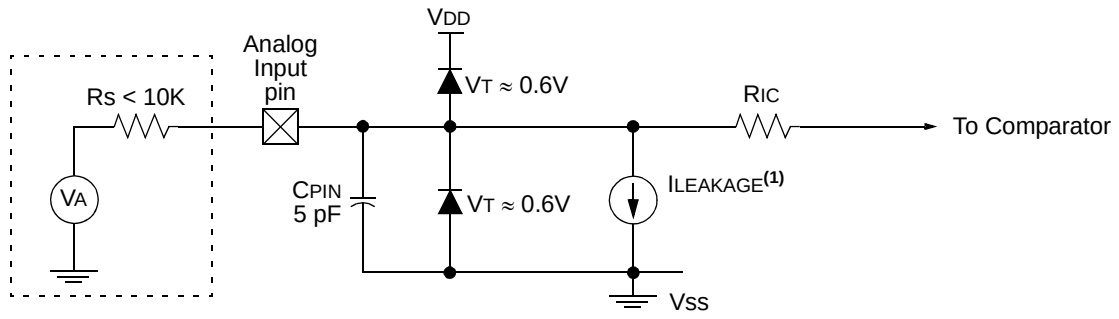
A simplified circuit for an analog input is shown in Figure 15-4. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 15-4: ANALOG INPUT MODEL



Legend: CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC = Interconnect Resistance
RS = Source Impedance
VA = Analog Voltage
VT = Threshold Voltage

Note 1: See **Section 20.0 "Electrical Specifications"**

RLF **Rotate Left f through Carry**

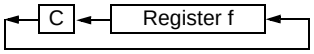
Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register ‘f’ are rotated one bit to the left through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.



Words: 1

Cycles: 1

Example:

```
RLF     REG1,0
```

Before Instruction
```
REG1    =   1110 0110
C       =   0
```
After Instruction
```
REG1    =   1110 0110
W       =   1100 1100
C       =   1
```

RRF **Rotate Right f through Carry**

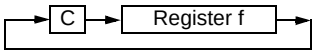
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register ‘f’ are rotated one bit to the right through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.



SLEEP **Enter Sleep mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into Sleep mode with the oscillator stopped.

SUBLW **Subtract W from literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Description: The W register is subtracted (2’s complement method) from the 8-bit literal ‘k’. The result is placed in the W register.

Result	Condition
C = 0	W > k
C = 1	W ≤ k
DC = 0	W<3:0> > k<3:0>
DC = 1	W<3:0> ≤ k<3:0>

REGISTER 17-1: CONFIGURATION WORD

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{DEBUG}}$	$\overline{\text{CLKOUTEN}}$	WRT<1:0>		BOREN<1:0>	
bit 13					bit 8

U-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1	U-1	R/P-1
—	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	—	—	FOSC0
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **$\overline{\text{DEBUG}}$:** Debug Mode Enable bit(2)
1 = Background debugger is disabled
0 = Background debugger is enabled

bit 12 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
1 = Clock out function disabled. CLKOUT pin acts as I/O pin
0 = General purpose I/O disabled. CLKOUT pin acts as CLKOUT

bit 11-10 **WRT<1:0>:** Flash Program Memory Self Write Enable bit
11 = Write protection off
10 = 000h to FFh write-protected, 100h to 3FFh may be modified by PMCON1 control
01 = 000h to 1FFh write-protected, 200h to 3FFh may be modified by PMCON1 control
00 = 000h to 3FFh write-protected, entire program is write-protected

bit 8-9 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
0x = BOR disabled

bit 7 Unimplemented: Read as ‘1’.

bit 6 **$\overline{\text{CP}}$:** Code Protection bit
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 5 **MCLRE:** $\overline{\text{MCLR}}$/V_{PP} Pin Function Select bit
1 = $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$ function and weak internal pull-up is enabled
0 = $\overline{\text{MCLR}}$ pin is input function, $\overline{\text{MCLR}}$ function is internally disabled

bit 4 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-1 Unimplemented: Read as ‘1’.

bit 0 **FOSC:** Oscillator Selection bits
1 = EC oscillator selected: CLKIN on RA5/CLKIN
0 = Internal oscillator: I/O function on RA5/CLKIN

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.

2: The Configuration bit is managed automatically by the device development tools. The user should not attempt to manually write this bit location. However, the user should ensure that this location has been programmed to a ‘1’ and the device checksum is correct for proper operation of production software.

TABLE 17-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1	
EC, INTOSC	TPWRT	—	TPWRT	—	—

TABLE 17-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{BOR}$	$\overline{TO}$	$\overline{PD}$	Condition
0	x	1	1	Power-on Reset
u	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	$\overline{MCLR}$ Reset during normal operation
u	u	1	0	$\overline{MCLR}$ Reset during Sleep

Legend: u = unchanged, x = unknown

TABLE 17-4: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset WDT Reset Brown-out Reset(1)	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h/100h/180h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h/102h/182h	0000 0000	0000 0000	PC + 1(3)
STATUS	03h/83h/103h/183h	0001 1xxx	000q quuu(4)	uuuq quuu(4)
FSR	04h/84h/104h/184h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--xx xxxx	--uu uuuu	--uu uuuu
IOCAF	08h	--00 0000	--00 0000	--uu uuuu
PCLATH	0Ah/8Ah/10Ah/18Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh/10Bh/18Bh	0000 0000	0000 0000	uuuu uuuu(2)
PIR1	0Ch	00-- -0-0	00-- -0-0	uu-- -u-u(2)
PIR2	0Dh	--00 -0-0	--00 -0-0	--uu -u-u(2)
TMR1L	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	10h	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	11h	0000 00-0	uuuu uu-u	uuuu uu-u
T1GCON	12h	0000 0x00	0000 0x00	uuuu uuuu
CCPR1L(1)	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H(1)	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON(1)	15h	--00 0000	--00 0000	--uu uuuu
ADRESL(1)	1Ch	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADRESH(1)	1Dh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0(1)	1Eh	0000 0000	0000 0000	uuuu uuuu
ADCON1(1)	1Fh	-000 ----	-000 ----	-uuu ----
OPTION_REG	81h/181h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
IOCAP	88h	--00 0000	--00 0000	--uu uuuu
PIE1	8Ch	00-- -000	00-- -000	uu-- -uuu
PIE2	8Dh	--00 -0-0	--00 -0-0	--uu -u-u
OSCCON	8Fh	--01 -00-	--uu -uu-	--uu -uu-
FVRCON	90h	0000 ----	0000 ----	uuuu ----
DACCON0	91h	000- -0--	000- -0--	uuu- -u--
DACCON1	92h	---0 0000	---0 0000	---u uuuu
CM2CON0	9Bh	0000 0100	0000 0100	uuuu uuuu
CM2CON1	9Ch	0000 ---0	0000 ---0	uuuu ---u

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIRx will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 17-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

17.4 Interrupts

The PIC12F752/HV752 has multiple sources of interrupt:

- External Interrupt (INT pin)
- Interrupt-On-Change (IOC) Interrupts
- Timer0 Overflow Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Hardware Limit Timer (HLT) Interrupt
- Comparator Interrupt (C1/C2)
- ADC Interrupt
- Complementary Output Generator (COG)
- CCP1 Interrupt
- Flash Memory Self Write

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Registers (PIRx) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

The Global Interrupt Enable bit, GIE of the INTCON register, enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIEx registers. GIE is cleared on Reset.

When an interrupt is serviced, the following actions occur automatically:

- The GIE is cleared to disable any further interrupt
- The return address is pushed onto the stack
- The PC is loaded with 0004h

The Return from Interrupt instruction, `RETFIE`, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- Interrupt-On-Change (IOC) Interrupts
- Timer0 Overflow Interrupt

The peripheral interrupt flags are contained in the PIR1 and PIR2 registers. The corresponding interrupt enable bit is contained in the PIE1 and PIE2 registers.

The following interrupt flags are contained in the PIR1 register:

- A/D Interrupt
- Comparator Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Enhanced CCP Interrupt

For external interrupt events, such as the INT pin or PORTA change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 17-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.
2:	When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, ADC, Enhanced CCP modules, refer to the respective peripheral section.

17.4.1 RA2/INT INTERRUPT

The external interrupt on the RA2/INT pin is edge-triggered; either on the rising edge if the INTEDG bit of the OPTION register is set, or the falling edge, if the INTEDG bit is clear. When a valid edge appears on the RA2/INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared by software in the Interrupt Service Routine before re-enabling this interrupt. The RA2/INT interrupt can wake-up the processor from Sleep, if the INTE bit was set prior to going into Sleep. See **Section 17.7 "Power-down Mode (Sleep)"** for details on Sleep and Figure 17-10 for timing of wake-up from Sleep through RA2/INT interrupt.

Note:	The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0' and cannot generate an interrupt.

17.4.2 TIMER0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set the T0IF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing T0IE bit of the INTCON register. See **Section 6.0 "Timer0 Module"** for operation of the Timer0 module.

TABLE 20-4: I/O PORTS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
		Capacitive Loading Specs on Output Pins					
D101*	COSC2	OSC2 pin	—	—	15	pF	
D101A*	CIO	All I/O pins	—	—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: This specification applies to all weak pull-up pins, including the weak pull-up found on RA3/$\overline{MCLR}$. When RA3/$\overline{MCLR}$ is configured as $\overline{MCLR}$ Reset pin, the weak pull-up is always enabled.

TABLE 20-5: MEMORY PROGRAMMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
		Program Memory Programming Specifications					
D110	V_{IHH}	Voltage on $\overline{MCLR}$/V_{PP} pin	10.0	—	13.0	V	**(Note 1)**
D112	V_{BE}	V_{DD} for Bulk Erase	4.5	—	V_{DDMAX}	V	
D113	V_{PEW}	V_{DD} for Write or Row Erase	4.5	—	V_{DDMAX}	V	
D114	I_{PPPGM}	Current on $\overline{MCLR}$/V_{PP} during Erase/Write	—	300	1000	μA	
		Program Flash Memory					
D121	E_P	Cell Endurance	10K	100K	—	E/W	-40°C ≤ T_A ≤ +85°C **(Note 2)**
D121A	E_P	Cell Endurance	1K	10K	—	E/W	-40°C ≤ T_A ≤ +125°C **(Note 2)**
D122	V_{PRW}	V_{DD} for Read/Write	V_{DDMIN}	—	V_{DDMAX}	V	
D123	T_{IW}	Self-timed Write Cycle Time	—	2	2.5	ms	
D124	T_{RETD}	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

† Data in "Typ." column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Required only if single-supply programming is disabled.

2: Self-write and Block Erase.

FIGURE 21-38: SCHMITT TRIGGER INPUT THRESHOLD, VIN vs. VDD, OVER TEMPERATURE

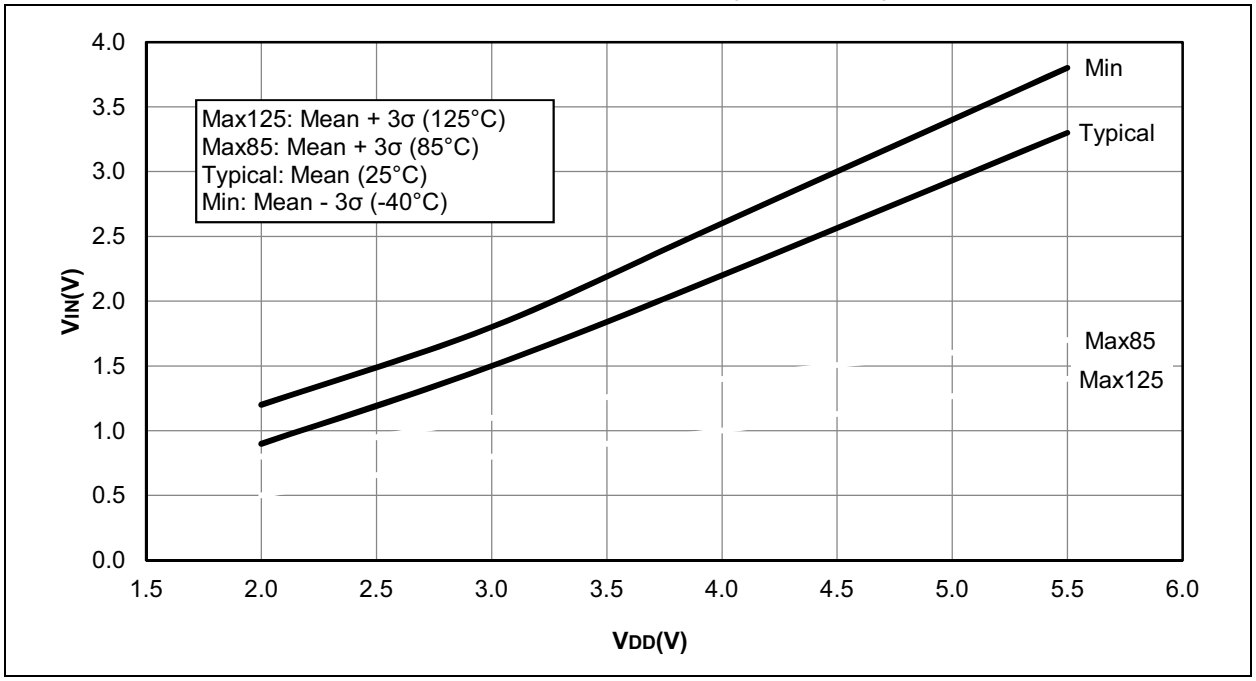


FIGURE 21-39: TTL INPUT THRESHOLD, VIN vs. VDD, OVER TEMPERATURE