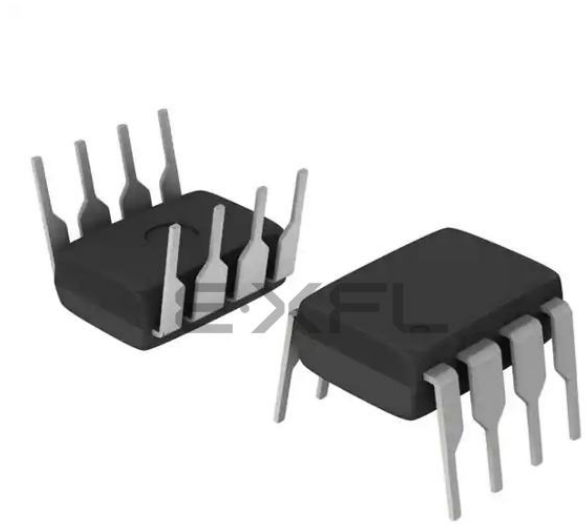


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f752-i-p

TABLE 2-4: PIC12F752/HV752 SPECIAL REGISTERS SUMMARY BANK 2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR Reset	Value on all other Resets(1)
Bank 2											
100h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
101h	TMR0	Holding Register for the 8-bit Timer0 Register								xxxx xxxx	uuuu uuuu
102h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
103h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
104h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
105h	LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	--xx -xxx	--uu -uuu
106h	—	Unimplemented								—	—
107h	—	Unimplemented								—	—
108h	IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	--00 0000	--00 0000
109h	—	Unimplemented								—	—
10Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	---0 0000
10Bh	INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF(2)	0000 0000	0000 0000
10Ch	WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	--00 0000	--00 0000
10Dh	SLRCONA	—	—	—	—	—	SLRA2	—	SLRA0	---- -0-0	---- -0-0
10Eh	—	Unimplemented								—	—
10Fh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	---- --uu
110h	TMR2	Holding Register for the 8-bit Timer2 Register								0000 0000	0000 0000
111h	PR2	Timer2 Period Register								1111 1111	1111 1111
112h	T2CON	—	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000	-000 0000
113h	HLTMR1	Holding Register for the 8-bit Hardware Limit Timer1 Register								0000 0000	0000 0000
114h	HLTPR1	Hardware Limit Timer1 Period Register								1111 1111	1111 1111
115h	HLT1CON0	—	H1OUTPS<3:0>				H1ON	H1CKPS<1:0>		-000 0000	-000 0000
116h	HLT1CON1	—	—	—	H1ERS<2:0>			H1FEREN	H1REREN	---0 0000	---0 0000
117h to 11Fh	—	Unimplemented								—	—

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition shaded = unimplemented

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: MCLR and WDT Reset does not affect the previous value data latch. The IOCIF bit will be cleared upon Reset but will set again if the mismatch exists.

3.4 Reading the Flash Program Memory

To read a program memory location, the user must write two bytes of the address to the PMADRL and PMADRH registers, and then set control bit RD (PMCON1<0>). Once the read control bit is set, the program memory Flash controller will use the second instruction cycle after to read the data. This causes the second instruction immediately following the "`BSF PMCON1,RD`" instruction to be ignored. The data is available in the very next cycle in the PMDATL and PMDATH registers; it can be read as two bytes in the following instructions. PMDATL and PMDATH registers will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 3-1: FLASH PROGRAM READ

```
    BANKSEL  PM_ADR          ; Change STATUS bits RP1:0 to select bank with PMADRL
    MOVLW    MS_PROG_PM_ADDR ;
    MOVWF    PMADRH          ; MS Byte of Program Address to read
    MOVLW    LS_PROG_PM_ADDR ;
    MOVWF    PMADRL          ; LS Byte of Program Address to read
    BANKSEL  PMCON1          ; Bank to containing PMCON1
    BSF      PMCON1, RD      ; PM Read

    NOP                      ; First instruction after BSF PMCON1,RD executes normally

    NOP                      ; Any instructions here are ignored as program
                             ; memory is read in second cycle after BSF PMCON1,RD
                             ;
    BANKSEL  PMDATL          ; Bank to containing PMADRL
    MOVF     PMDATL, W       ; W = LS Byte of Program PMDATL
    MOVF     PMDATH, W       ; W = MS Byte of Program PMDATL
```

REGISTER 5-8: IOCAP: INTERRUPT-ON-CHANGE POSITIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **IOCAP<5:0>:** Interrupt-on-Change Positive Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a positive going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 5-9: IOCAN: INTERRUPT-ON-CHANGE NEGATIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **IOCAN<5:0>:** Interrupt-on-Change Negative Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a negative going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 5-10: IOCAF: INTERRUPT-ON-CHANGE FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HS - Bit is set in hardware

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **IOCAF<5:0>:** Interrupt-on-Change Flag bits
1 = An enabled change was detected on the associated pin.
Set when IOCAPx = 1 and a rising edge was detected on RBx, or when IOCANx = 1 and a falling edge was detected on RAx.
0 = No change was detected, or the user cleared the detected change.

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	ADFM	VCFG	CHS<3:0>				GO/$\overline{\text{DONE}}$	ADON	94
ADCON1	—	ADCS<2:0>			—	—	—	—	94
ANSELA	—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0	41
APFCON	—	—	—	T1GSEL	—	COG1FSEL	COG1O1SEL	COG1O0SEL	38
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1ZLF	C1SP	C1HYS	C1SYNC	113
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2ZLF	C2SP	C2HYS	C2SYNC	113
CM1CON1	C1INTP	C1INTN	C1PCH<1:0>		—	—	—	C1NCH0	114
CM2CON1	C2NTP	C2INTN	C2PCH<1:0>		—	—	—	C2NCH0	114
DACCON0	DACEN	DACRNG	DACOE	—	—	DACPSS0	—	—	105
IOCAF	—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	45
IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	45
IOCAP	—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	45
LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	40
OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS<2:0>			14
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	40
SLRCONA	—	—	—	—	—	SLRA2	—	SLRA0	42
TRISA	—	—	TRISA5	TRISA4	TRISA3(1)	TRISA2	TRISA1	TRISA0	40

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note 1: TRISA3 always reads '1'.

10.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM modules is a peripheral which allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

10.1 Capture Mode

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the CCP1 pin, the 16-bit CCPR1H:CCPR1L register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- Every Falling Edge
- Every Rising Edge
- Every 4th Rising Edge
- Every 16th Rising Edge

When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR2 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPR1H, CCPR1L register pair is read, the old captured value is overwritten by the new captured value.

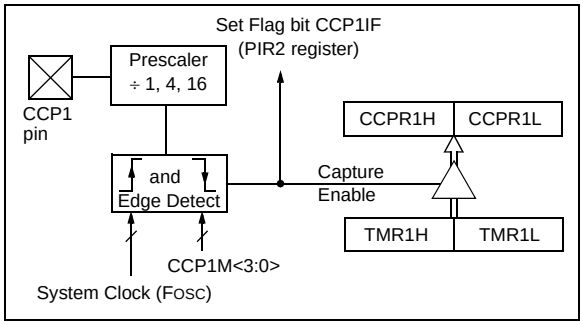
Figure 10-1 shows a simplified diagram of the Capture operation.

10.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the associated TRIS control bit.

Note:	If the CCP1 pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 10-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



10.1.2 TIMER1 MODE RESOURCE

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP1 module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See **Section 7.0 "Timer1 Module with Gate Control"** for more information on configuring Timer1.

10.1.3 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit of the PIE2 register clear to avoid false interrupts. Additionally, the user should clear the CCP1IF interrupt flag bit of the PIR2 register following any change in Operating mode.

Note:	Clocking Timer1 from the system clock (FOSC) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCP1 pin, Timer1 must be clocked from the instruction clock (FOSC/4) or from an external clock source.

10.1.4 CCP1 PRESCALER

There are four prescaler settings specified by the CCP1M<3:0> bits of the CCP1CON register. Whenever the CCP1 module is turned off or the CCP1 module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCP1CON register before changing the prescaler. Example 10-1 demonstrates the code to perform this function.

EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
BANKSEL CCP1CON     ;Set Bank bits to point
                    ;to CCP1CON
CLRF    CCP1CON     ;Turn CCP1 module off
MOVLW   NEW_CAPT_PS ;Load the W reg with
                    ;the new prescaler
                    ;move value and CCP1 ON
MOVWF   CCP1CON     ;Load CCP1CON with this
                    ;value
```

10.1.5 CAPTURE DURING SLEEP

Capture mode depends upon the Timer1 module for proper operation. If the Timer1 clock input source is a clock that is not disabled during Sleep, Timer1 will continue to operate and Capture mode will operate during Sleep to wake the device. The T1CKI is an example of a clock source that will operate during Sleep.

When the input source to Timer1 is disabled during Sleep, such as the HFINTOSC, Timer1 will not increment during Sleep. When the device wakes from Sleep, Timer1 will continue from its previous state.

TABLE 10-1: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>				73
CCPR1L	Capture/Compare/PWM Register x Low Byte (LSB)								67*
CCPR1H	Capture/Compare/PWM Register x High Byte (MSB)								67*
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	15
PIE1	TMR1GIE	ADIE	—	—	—	HLTMR1IE	TMR2IE	TMR1IE	16
PIE2	—	—	C2IE	C1IE	—	COG1IE	—	CCP1IE	17
PIR1	TMR1GIF	ADIF	—	—	—	HLTMR1IF	TMR2IF	TMR1IF	18
PIR2	—	—	C2IF	C1IF	—	COG1IF	—	CCP1IF	19
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		Reserved	$\overline{\text{T1SYNC}}$	—	TMR1ON	58
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	$\overline{\text{T1GVAL}}$	T1GSS<1:0>		59
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								50*
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								50*
TRISA	—	—	TRISA5	TRISA4	TRISA3(1)	TRISA2	TRISA1	TRISA0	40

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by Capture mode.
* Page provides register information.

Note 1: TRISA3 always reads '1'.

11.0 COMPLEMENTARY OUTPUT GENERATOR (COG) MODULE

The primary purpose of the Complementary Output Generator (COG) is to convert a single output PWM signal into a two output complementary PWM signal. The COG can also convert two separate input events into a single or complementary PWM output.

The COG PWM frequency and duty cycle are determined by a rising event input and a falling event input. The rising event and falling event may be the same source. Sources may be synchronous or asynchronous to the COG_clock.

The rate at which the rising event occurs determines the PWM frequency. The time from the rising event input to the falling event input determines the duty cycle.

A selectable clock input is used to generate the phase delay, blanking and dead-band times.

A simplified block diagram of the COG is shown in Figure 11-1.

The COG module has the following features:

- Selectable clock source
- Selectable rising event source
- Selectable falling event source
- Selectable edge or level event sensitivity
- Independent output enables
- Independent output polarity selection
- Phase delay
- Dead-band control with independent rising and falling event dead-band times
- Blanking control with independent rising and falling event blanking times
- Auto-shutdown control with:
  - Selectable shutdown sources
  - Auto-restart enable
  - Auto-shutdown pin override control

11.1 Fundamental Operation

The COG generates a two output complementary PWM waveform from rising and falling event sources. In the simplest configuration, the rising and falling event sources are the same signal, which is a PWM signal with the desired period and duty cycle. The COG converts this single PWM input into a dual complementary PWM output. The frequency and duty cycle of the dual PWM output match those of the single input PWM signal. The off-to-on transition of each output can be delayed from the on-to-off transition of the other output, thereby, creating a time immediately after the PWM transition where neither output is driven. This is referred to as dead time and is covered in **Section 11.5 “Dead-Band Control”**.

A typical operating waveform, with dead band, generated from a single CCP1 input is shown in Figure 11-2.

The COG can also generate a PWM waveform from a periodic rising event and a separate falling event. In this case, the falling event is usually derived from analog feedback within the external PWM driver circuit. In this configuration, high-power switching transients may trigger a false falling event that needs to be blanked out. The COG can be configured to blank falling (and rising) event inputs for a period of time immediately following the rising (and falling) event drive output. This is referred to as input blanking and is covered in **Section 11.6 “Blanking Control”**.

It may be necessary to guard against the possibility of circuit faults. In this case, the active drive must be terminated before the Fault condition causes damage. This is referred to as auto-shutdown and is covered in **Section 11.8 “Auto-Shutdown Control”**.

A feedback falling event arriving too late or not at all can be terminated with auto-shutdown or by using one of the event inputs that is logically or’d with the hardware limit timer (HLT). See **Section 9.0 “Hardware Limit Timer (HLT) Module”** for more information about the HLT.

The COG can be configured to operate in phase delayed conjunction with another PWM. The active drive cycle is delayed from the rising event by a phase delay timer. Phase delay is covered in more detail in **Section 11.7 “Phase Delay”**.

A typical operating waveform, with phase delay and dead band, generated from a single CCP1 input is shown in Figure 11-3.

REGISTER 11-3: COGxASD: COG AUTO-SHUTDOWN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
GxASDE	GxARSEN	GxASDL1	GxASDL0	GxASDSHLT	GxASDSC2	GxASDSC1	GxASDSFLT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **GxASDE:** Auto-Shutdown Event Status bit
1 = COG is in the shutdown state
0 = COG is not in the shutdown state

bit 6 **GxARSEN:** Auto-Restart Enable bit
1 = Auto-restart is enabled
0 = Auto-restart is disabled

bit 5 **GxASDL1:** COGxOUT1 Auto-shutdown Override Level bit
1 = A logic ‘1’ is placed on COGxOUT1 when a shutdown input is true
0 = A logic ‘0’ is placed on COGxOUT1 when a shutdown input is true

bit 4 **GxASDL0:** COGxOUT0 Auto-shutdown Override Level bit
1 = A logic ‘1’ is placed on COGxOUT0 when a shutdown input is true
0 = A logic ‘0’ is placed on COGxOUT0 when a shutdown input is true

bit 3 **GxASDSHLT:** COG Auto-shutdown Source Enable bit 3
1 = COG is shutdown when HLTMR equals HLTPR is low
0 = HLTimer1 pin has no effect on shutdown

bit 2 **GxASDSC2:** COG Auto-shutdown Source Enable bit 2
1 = COG is shutdown when C2OUT is low
0 = C2OUT pin has no effect on shutdown

bit 1 **GxASDSC1:** COG Auto-shutdown Source Enable bit 1
1 = COG is shutdown when C1OUT is low
0 = C1OUT pin has no effect on shutdown

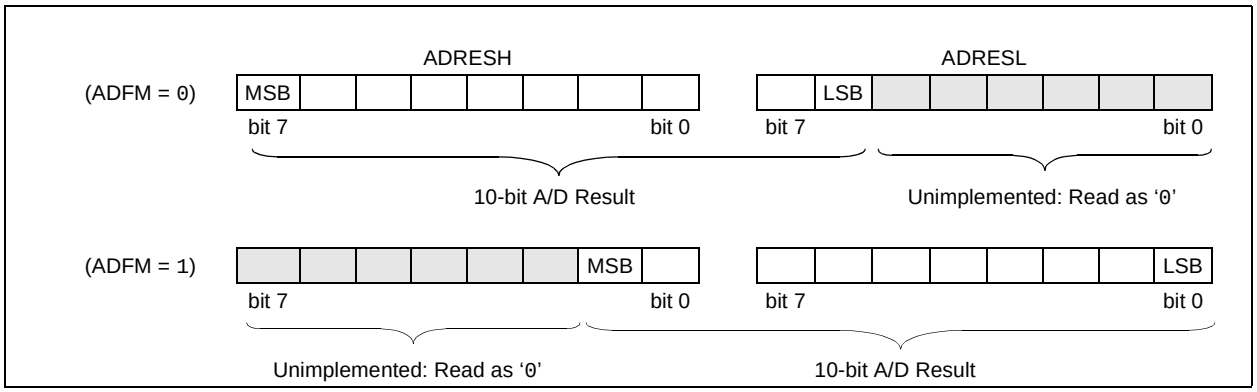
bit 0 **GxASDSFLT:** COG Auto-shutdown Source Enable bit 0
1 = COG is shutdown when COGxFLT pin is low
0 = COGxFLT pin has no effect on shutdown

12.1.6 RESULT FORMATTING

The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON0 register controls the output format.

Figure 12-4 shows the two output formats.

FIGURE 12-3: 10-BIT A/D CONVERSION RESULT FORMAT



12.2 ADC Operation

12.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/$\overline{\text{DONE}}$ bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

Note:	The GO/$\overline{\text{DONE}}$ bit should not be set in the same instruction that turns on the ADC. Refer to **Section 12.2.6 "A/D Conversion Procedure"**.

12.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/$\overline{\text{DONE}}$ bit
- Set the ADIF flag bit
- Update the ADRESH:ADRESL registers with new conversion result

12.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/$\overline{\text{DONE}}$ bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete Analog-to-Digital conversion sample. Instead, the ADRESH:ADRESL register pair will retain the value of the previous conversion. Additionally, a 2 TAD delay is required before another acquisition can be initiated. Following this delay, an input acquisition is automatically started on the selected channel.

Note:	A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

12.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

12.2.5 SPECIAL EVENT TRIGGER

The CCP Special Event Trigger allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/$\overline{\text{DONE}}$ bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See **Section 10.0 "Capture/Compare/PWM Modules"** for more information.

REGISTER 12-3: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0 (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES<9:2>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<9:2>**: ADC Result Register bits
Upper eight bits of 10-bit conversion result

REGISTER 12-4: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0 (READ-ONLY)

R-x	R-x	U-0	U-0	U-0	U-0	U-0	U-0
ADRES<1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **ADRES<1:0>**: ADC Result Register bits
Lower two bits of 10-bit conversion result

bit 5-0 **Unimplemented:** Read as '0'

REGISTER 12-5: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1 (READ-ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	R-x	R-x
—	—	—	—	—	—	ADRES<9:8>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **ADRES<9:8>**: ADC Result Register bits
Upper two bits of 10-bit conversion result

REGISTER 12-6: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1 (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
Lower eight bits of 10-bit conversion result

TABLE 12-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	ADFM	VCFG	CHS<3:0>				GO/$\overline{\text{DONE}}$	ADON	94
ADCON1	—	ADCS<2:0>			—	—	—	—	94
ANSELA	—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0	41
ADRESH(2)	A/D Result Register High Byte								96*
ADRESL(2)	A/D Result Register Low Byte								94*
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	40
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	15
PIE1	TMR1GIE	ADIE	—	—	—	HLTMR1IE	TMR2IE	TMR1IE	16
PIR1	TMR1GIF	ADIF	—	—	—	HLTMR1IF	TMR2IF	TMR1IF	18
TRISA	—	—	TRISA5	TRISA4	TRISA3(1)	TRISA2	TRISA1	TRISA0	40

Legend: x = unknown, u = unchanged, – = unimplemented read as '0'. Shaded cells are not used for ADC module.

* Page provides register information.

Note 1: TRISA3 always reads '1'.

2: Read-only register.

13.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference (FVR) is a stable voltage reference, independent of VDD, with 1.2V output level. The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel
- Comparator 1 positive input (C1VP)
- Comparator 2 positive input (C2VP)
- REFOUT pin

On the PIC12F752, the FVR is enabled by setting the FVREN bit of the FVRCON register. The FVR is always enabled on the PIC12HV752 device.

13.1 Fixed Voltage Reference Output

The FVR output can be applied to the REFOUT pin by setting the FVRBUFSS and FVRBUFEN bits of the FVRCON register. The FVRBUFSS bit selects either the FVR or DAC output reference to the REFOUT pin buffer. The FVRBUFEN bit enables the output buffer to the REFOUT pin.

Enabling the REFOUT pin automatically overrides any digital input or output functions of the pin. Reading the REFOUT pin when it has been configured for a reference voltage output will always return a '0'.

13.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference circuit to stabilize. Once the circuit stabilizes and is ready for use, the FVRRDY bit of the FVRCON register will be set. See **Section 20.0 "Electrical Specifications"** for the minimum delay requirement.

13.3 Operation During Sleep

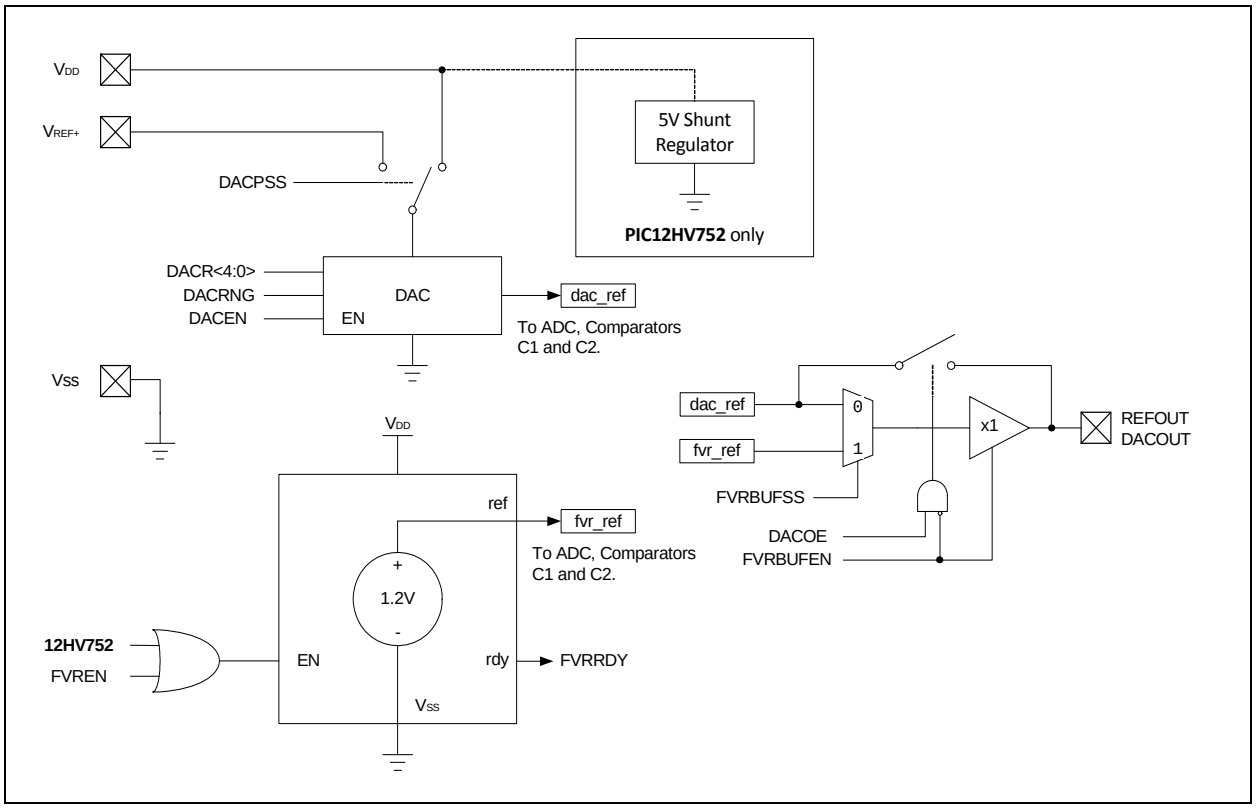
When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the FVRCON register are not affected. To minimize current consumption in Sleep mode, FVR the voltage reference should be disabled.

13.4 Effects of a Reset

A device Reset clears the FVRCON register. As a result:

- The FVR module is disabled
- The FVR voltage output is disabled on the REFOUT pin

FIGURE 13-1: VOLTAGE REFERENCE BLOCK DIAGRAM



16.2 Instruction Descriptions

ADDLW	Add literal and W
Syntax:	[*label*] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the 8-bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW	AND literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the 8-bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b' in register 'f' is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

TABLE 17-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0x
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---- --uu
$\overline{MCLR}$ Reset during Sleep	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 uuuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --u0
Interrupt Wake-up from Sleep	PC + 1(1)	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

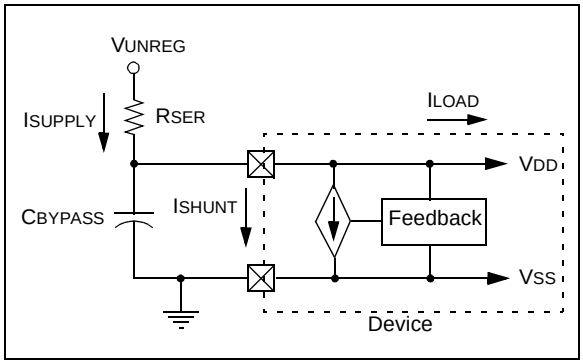
18.0 SHUNT REGULATOR (PIC12HV752 ONLY)

The PIC12HV752 devices include a permanent internal 5 volt (nominal) shunt regulator in parallel with the VDD pin. This eliminates the need for an external voltage regulator in systems sourced by an unregulated supply. All external devices connected directly to the VDD pin will share the regulated supply voltage and contribute to the total VDD supply current (ILOAD).

18.1 Regulator Operation

A shunt regulator generates a specific supply voltage by creating a voltage drop across a pass resistor RSER. The voltage at the VDD pin of the microcontroller is monitored and compared to an internal voltage reference. The current through the resistor is then adjusted, based on the result of the comparison, to produce a voltage drop equal to the difference between the supply voltage VUNREG and the VDD of the microcontroller. See Figure 18-1 for voltage regulator schematic.

FIGURE 18-1: SHUNT REGULATOR



An external current limiting resistor, RSER, located between the unregulated supply, VUNREG, and the VDD pin, drops the difference in voltage between VUNREG and VDD. RSER must be between RMAX and RMIN as defined by Equation 18-1.

EQUATION 18-1: RSER LIMITING RESISTOR

$$R_{MAX} = \frac{(VU_{MIN} - 5V)}{1.05 \bullet (1\ mA + I_{LOAD})}$$

$$R_{MIN} = \frac{(VU_{MAX} - 5V)}{0.95 \bullet (50\ mA)}$$

Where:

RMAX = maximum value of RSER (ohms)

RMIN = minimum value of RSER (ohms)

VUMIN = minimum value of VUNREG

VUMAX = maximum value of VUNREG

VDD = regulated voltage (5V nominal)

ILOAD = maximum expected load current in mA including I/O pin currents and external circuits connected to VDD.

1.05 = compensation for +5% tolerance of RSER

0.95 = compensation for -5% tolerance of RSER

18.2 Regulator Considerations

The supply voltage VUNREG and load current are not constant. Therefore, the current range of the regulator is limited. Selecting a value for RSER must take these three factors into consideration.

Since the regulator uses the band gap voltage as the regulated voltage reference, this voltage reference is permanently enabled in the PIC12HV752 devices.

The shunt regulator will still consume current when below operating voltage range for the shunt regulator.

18.3 Design Considerations

For more information on using the shunt regulator and managing current load, see Application Note AN1035, "*Designing with HV Microcontrollers*" (DS01035).

TABLE 20-8: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)								
Param. No.	**Sym.**	**Characteristic**	**Freq. Tolerance**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
OS06	TWARM	Internal Oscillator Switch when running	—	—	—	2	TOSC	
OS07	INTOSC	Internal Calibrated INTOSC Frequency(1) (4 MHz)	±1%	3.96	4.0	4.04	MHz	VDD = 3.5V, TA = 25°C
			±2%	3.92	4.0	4.08	MHz	2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C
			±5%	3.80	4.0	4.20	MHz	2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.)
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(1)	±1%	7.92	8	8.08	MHz	VDD = 3.5V, TA = 25°C
			±2%	7.84	8	8.16	MHz	2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C
			±5%	7.60	8	8.40	MHz	2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.)
OS09	LFOSC	Internal LFINTOSC Frequency	—	—	31	—	kHz	
OS10*	TIOSC ST	HFINTOSC Wake-up from Sleep Start-up Time	—	—	12	24	µs	VDD = 2.0V -40°C ≤ TA ≤ +85°C
				—	7	14	µs	VDD = 3.0V -40°C ≤ TA ≤ +85°C
				—	6	11	µs	VDD = 5.0V -40°C ≤ TA ≤ +85°C

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

TABLE 20-10: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

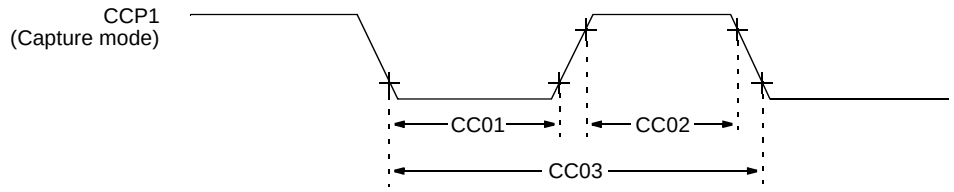
Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
30	T_{MCL}	$\overline{MCLR}$ Pulse Width (low)	2 5	— —	— —	µs µs	V_{DD} = 5V, -40°C to +85°C V_{DD} = 5V, -40°C to +125°C
31	T_{WDTLP}	Low-Power Watchdog Timer Time-out Period	10 10	20 20	30 35	ms ms	V_{DD} = 5V, -40°C to +85°C V_{DD} = 5V, -40°C to +125°C
32*	T_{PWRT}	Power-up Timer Period, PWRTE = 0 (No Prescaler)	40	65	140	ms	
33*	T_{IOZ}	I/O high-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.0	µs	
34	V_{BOR}	Brown-out Reset Voltage (1)	2	2.15	2.3	V	
35*	V_{HYST}	Brown-out Reset Hysteresis	—	100	—	mV	-40°C ≤ T_A ≤ +85°C
36*	T_{BOR}	Brown-out Reset DC Minimum Detection Period	100	—	—	µs	$V_{DD} \leq V_{BOR}$

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these voltage tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

FIGURE 20-9: PIC12F752/HV752 CAPTURE/COMPARE/PWM TIMINGS (CCP)



Note: Refer to Figure 20-3 for load conditions.

TABLE 20-12: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

Standard Operating Conditions (unless otherwise stated)								
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
CC01*	TccL	CCP1 Input Low Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCP1 Input High Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCP1 Input Period		$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 20-13: COMPARATOR SPECIFICATIONS(1)

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.†**	**Max.**	**Units**	**Comments**
CM01	VIOFF	Input Offset Voltage	—	± 10 ± 10	± 20 ± 20	mV mV	CxSP = 1 CxSP = 0
CM02	VICM	Input Common Mode Voltage	0	—	VDD – 1.5	V	
CM03	CMRR	Common Mode Rejection Ratio	—	50	—	dB	
CM04A*	TRT	Response Time	—	38	45	ns	CxSP = 1
			—	81	100	ns	CxSP = 0
CM05*	TMC20V	Comparator Mode Change to Output Valid	—	—	10	µs	
CM06	CHYSTER	Comparator Hysteresis	—	35	50	mV	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: See **Section 21.0 "DC and AC Characteristics Graphs and Charts"** for operating characterization.

FIGURE 21-24: IPD, COMPARATOR, LOW-POWER MODE, CxSP = 0, PIC12F752 ONLY

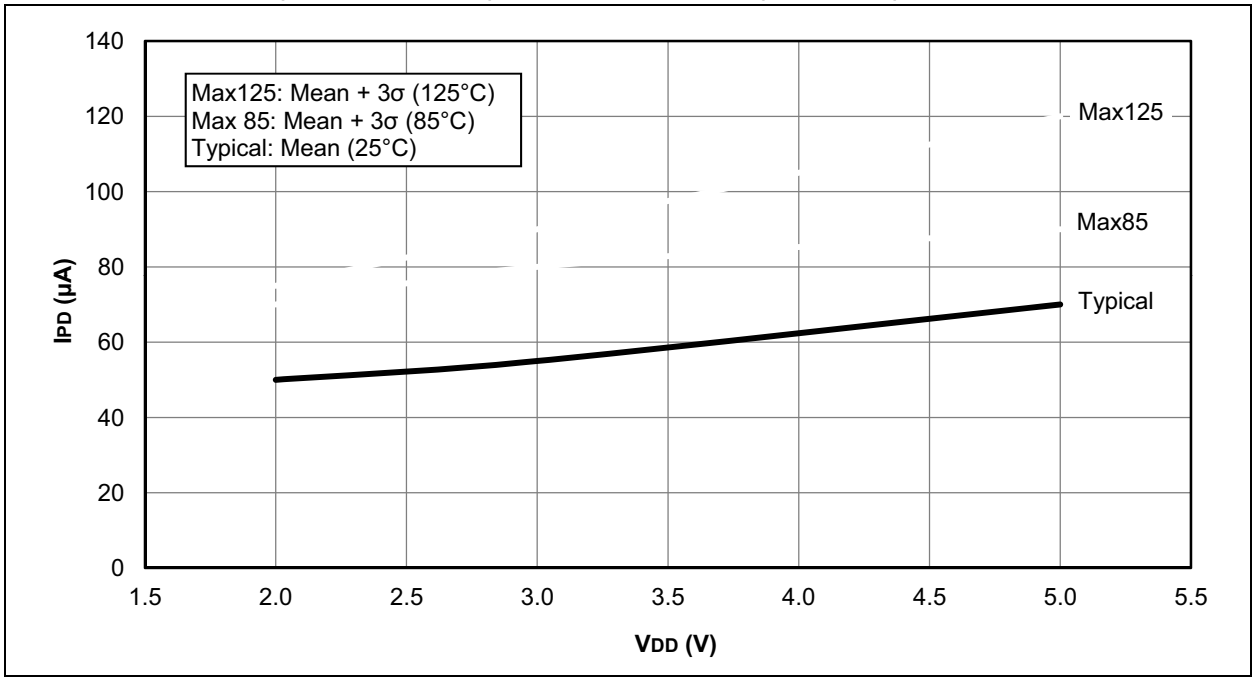


FIGURE 21-25: IPD, COMPARATOR, LOW-POWER MODE, CxSP = 0, PIC12HV752 ONLY

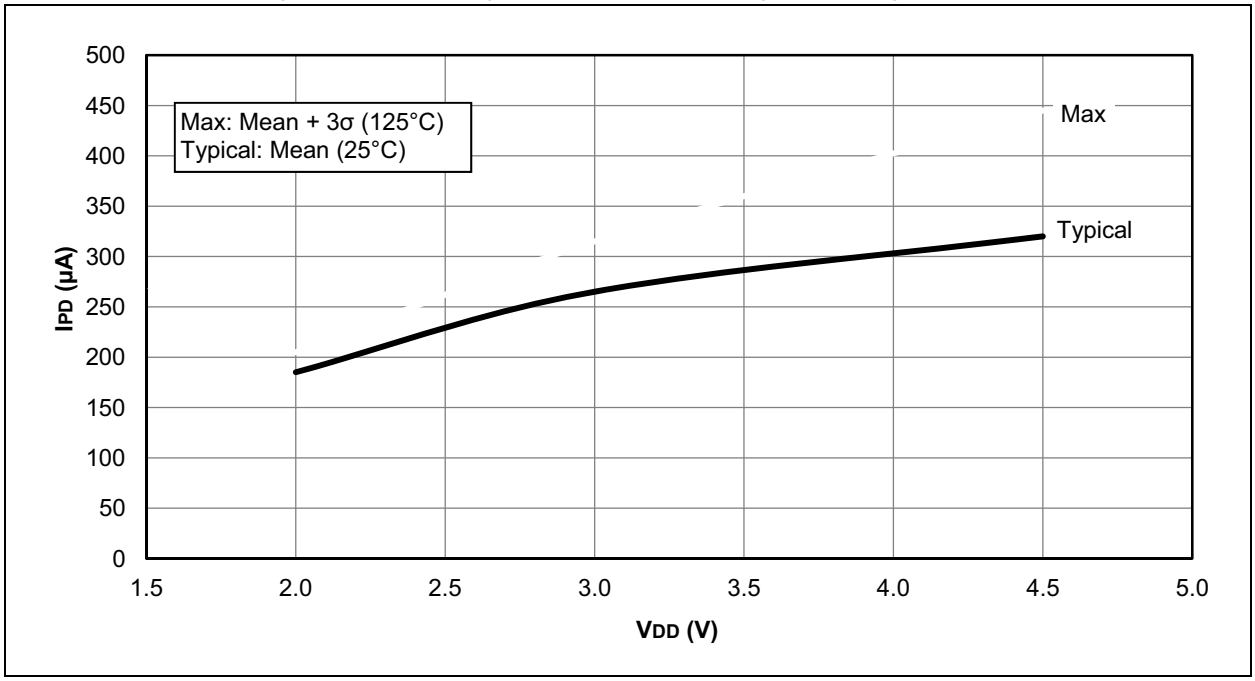


FIGURE 21-32: VOH vs. IOH, RA0/RA2, OVER TEMPERATURE, VDD = 3.0V

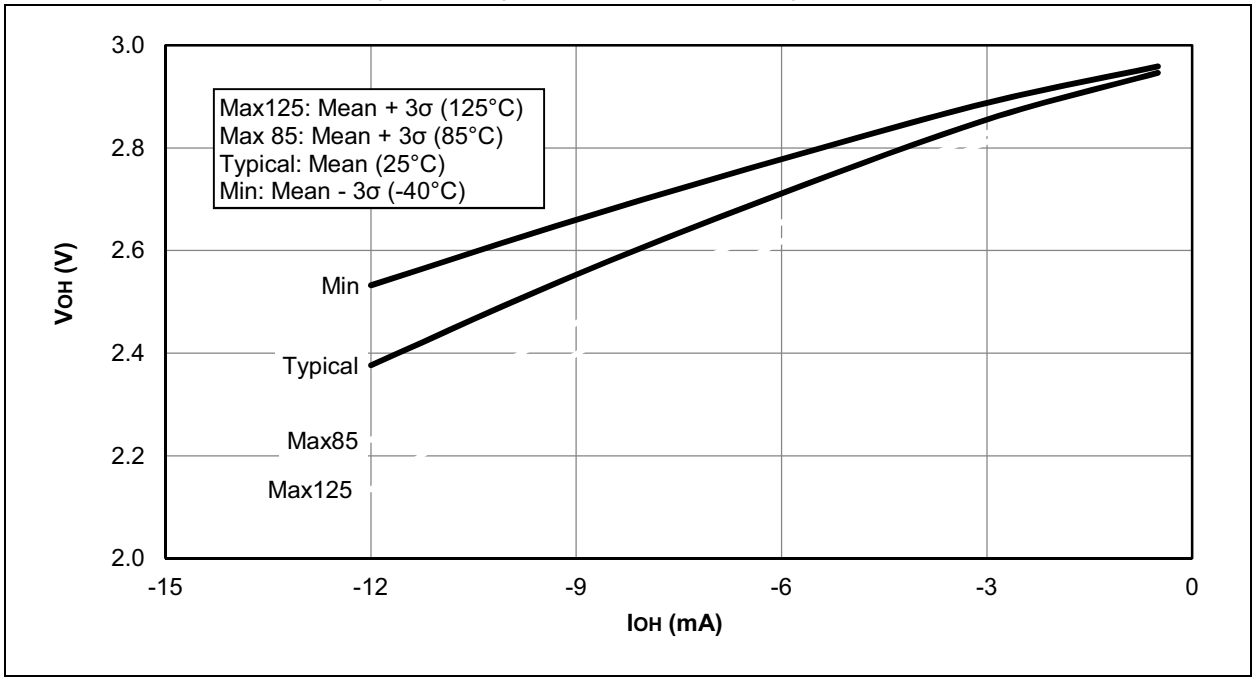


FIGURE 21-33: VOH vs. IOH, RA1/RA4/RA5, OVER TEMPERATURE, VDD = 3.0V