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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f752-i-sn

TABLE 2: 8-PIN ALLOCATION TABLE (PIC12F752/HV752)

I/O	8-Pin PDIP/SOIC/DFN	ADC	Comparators	Timers	CCP	Interrupts	Pull-up	Complementary Output Generator (COG)	Voltage Reference	Basic
RA0(4)	7	AN0	C1IN0+ C2IN0+	—	—	IOC	Y	COG1OUT1	DACOUT REFOUT	ICSPDAT
RA1	6	AN1	C1IN0- C2IN0-	—	—	IOC	Y	—	VREF+	ICSPCLK
RA2(4)	5	AN2	C1OUT C2OUT	T0CKI	CCP1	IOC INT	Y	COG1OUT0	—	—
RA3(1)	4	—	—	T1G(2)	—	IOC	Y(3)	COG1FLT(2)	—	$\overline{\text{MCLR}}$/VPP
RA4	3	AN3	C1IN1-	T1G	—	IOC	Y	COG1FLT COG1OUT1(2)	—	CLKOUT
RA5	2	—	C2IN1-	T1CKI	—	IOC	Y	COG1OUT0(2)	—	CLKIN
—	1	—	—	—	—	—	—	—	—	VDD
—	8	—	—	—	—	—	—	—	—	VSS

Note 1: Input-only.

2: Alternate pin function via the APFCON register.

3: RA3 pull-up is enabled when pin is configured as $\overline{\text{MCLR}}$ in Configuration Word.

4: The port pins for the primary COG1OUTx pins have High-Power (HP) output drivers.

4.0 OSCILLATOR MODULE

4.1 Overview

The oscillator module has a variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 4-1 illustrates a block diagram of the oscillator module.

The oscillator module can be configured in one of two clock modes.

1. EC (External Clock)
2. INTOSC (Internal Oscillator)

Clock Source modes are configured by the FOSC bit in the Configuration Word register (CONFIG).

The internal oscillator module provides the following selectable System Clock modes:

- 8 MHz (HFINTOSC)
- 4 MHz (HFINTOSC Postscaler)
- 1 MHz (HFINTOSC Postscaler)
- 31 kHz (LFINTOSC)

FIGURE 4-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM

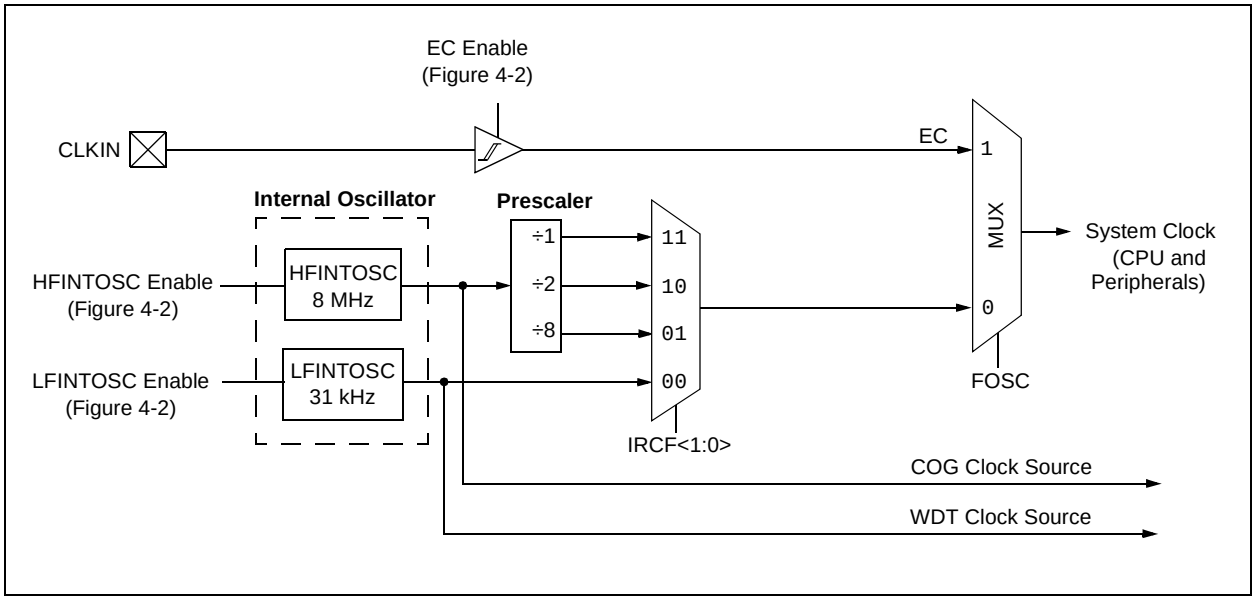
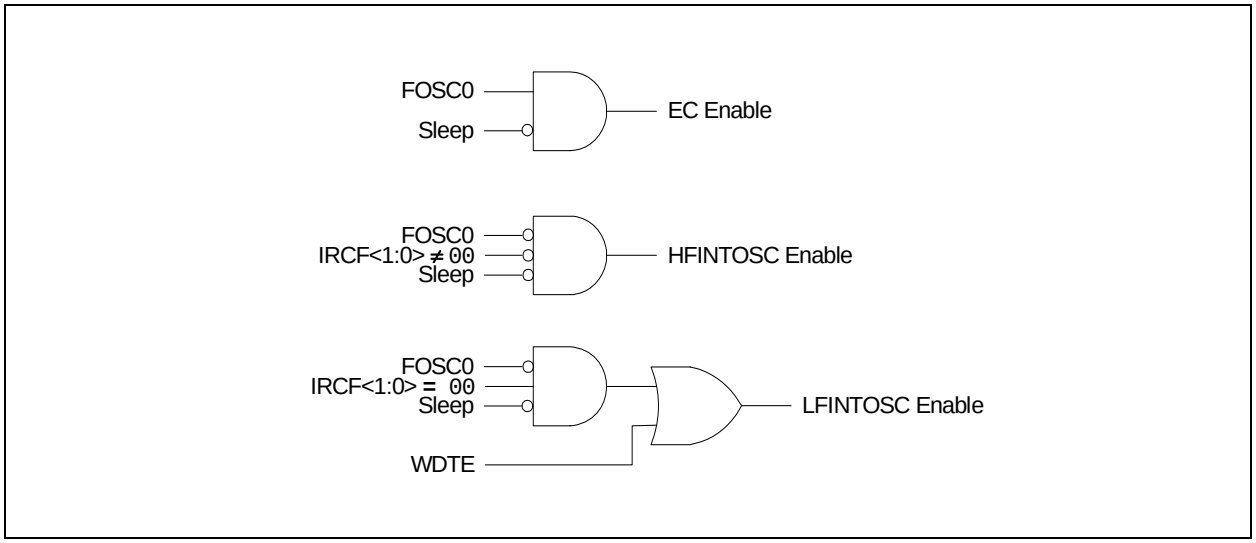


FIGURE 4-2: OSCILLATOR ENABLE



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4.5.1 OSCTUNE REGISTER

The oscillator is factory-calibrated, but can be adjusted in software by writing to the OSCTUNE register (Register 4-2).

The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

REGISTER 4-2: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	TUN<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Oscillator module is running at the calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	—	—	IRCF<1:0>		—	HTS	LTS	—	35
OSCTUNE	—	—	—	TUN<4:0>					36

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

2: See Configuration Word register (Register 17-1) for operation of all register bits.

TABLE 4-3: SUMMARY OF CONFIGURATION WORD CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG	13:8	—	—	$\overline{\text{DEBUG}}$	$\overline{\text{CLKOUTEN}}$	WRT<1:0>		BOREN<1:0>		126
	7:0	—	$\overline{\text{CP}}$	$\overline{\text{MCLRE}}$	$\overline{\text{PWRTE}}$	WDTE	—	—	FOSC0	

Legend: — = unimplemented location, read as '1'. Shaded cells are not used by oscillator module.

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5.5 Additional Pin Functions

Every PORTA pin on the PIC12F752 has an interrupt-on-change option and a weak pull-up option. The next three sections describe these functions.

5.5.1 ANSELA REGISTER

The ANSELA register (Register 5-8) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

REGISTER 5-5: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-4 **ANSA<5:4>**: Analog Select Between Analog or Digital Function on Pin RA<5:4> bits
1 = Analog input. Pin is assigned as analog input(1).
0 = Digital I/O. Pin is assigned to port or special function.

bit 3 **Unimplemented**: Read as '0'

bit 2-0 **ANSA<2:0>**:Analog Select Between Analog or Digital Function on Pin RA<2:0> bits
1 = Analog input. Pin is assigned as analog input.(1)
0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

7.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1 is enabled by configuring the TMR1ON and TMR1GE bits in the T1CON and T1GCON registers, respectively. Table 7-1 displays the Timer1 enable selections.

TABLE 7-1: TIMER1 ENABLE SELECTIONS

TMR1ON	TMR1GE	Timer1 Operation
0	0	Off
0	1	Off
1	0	Always On
1	1	Count Enabled

7.2 Clock Source Selection

The TMR1CS<1:0> bits of the T1CON register are used to select the clock source for Timer1. Table 7-2 displays the clock source selections.

TABLE 7-2: CLOCK SOURCE SELECTIONS

TMR1CS<1:0>	Clock Source
11	Temperature Sense Oscillator
10	External Clocking on T1CKI Pin
01	System Clock (FOSC)
00	Instruction Clock (FOSC/4)

7.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMR1H:TMR1L register pair will increment on multiples of FOSC or FOSC/4 as determined by the Timer1 prescaler.

7.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter. When enabled to count, Timer1 is incremented on the rising edge of the external clock input T1CKI.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge (see Figure 7-2) after any one or more of the following conditions:

- Timer1 enabled after POR Reset
- Write to TMR1H or TMR1L
- Timer1 is disabled
- Timer1 is disabled (TMR1ON = 0) when T1CKI is high; then Timer1 is enabled (TMR1ON=1) when T1CKI is low.

7.2.3 TEMPERATURE SENSE OSCILLATOR

When the Temperature Sense Oscillator source is selected, the TMR1H:TMR1L register pair will increment on multiples of the Temperature Sense Oscillator as determined by the Timer1 prescaler. The Temperature Sense Oscillator operates at 16 kHz typical.

9.0 HARDWARE LIMIT TIMER (HLT) MODULE

The Hardware Limit Timer (HLT) module is a version of the Timer2-type modules. In addition to all the Timer2-type features, the HLT can be reset on rising and falling events from selected peripheral outputs.

The HLT primary purpose is to act as a timed hardware limit to be used in conjunction with asynchronous analog feedback applications. The external reset source synchronizes the HLTMR1 to an analog application.

In normal operation, the external reset source from the analog application should occur before the HLTMR1 matches the HLTPR1. This resets HLTMR1 for the next period and prevents the HLTimer1 Output from going active.

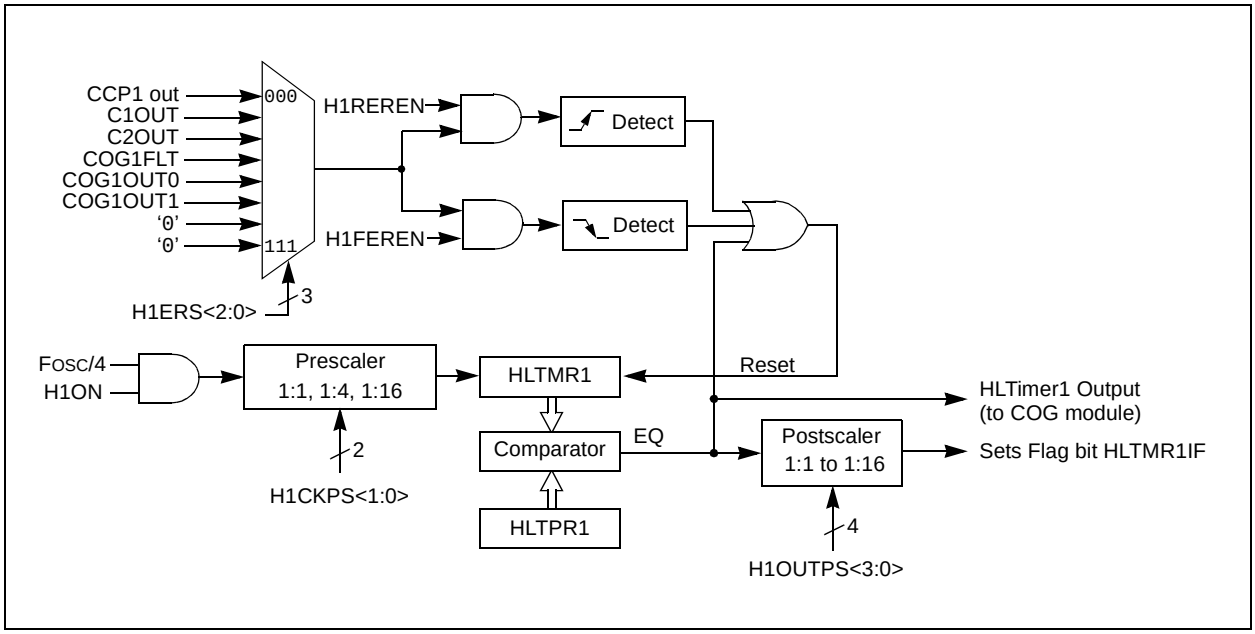
When the external reset source fails to generate a signal within the expected time, allowing the HLTMR1 to match the HLTPR1, then the HLTimer1 Output becomes active.

The HLT module incorporates the following features:

- 8-Bit Read-Write Timer Register (HLTMR1)
- 8-Bit Read-Write Period Register (HLTPR1)
- Software Programmable Prescaler
  - 1:1
  - 1:4
  - 1:16
- Software Programmable Postscaler:
  - 1:1 to 1:16, inclusive
- Interrupt on HLTMR1 Match with HLTPR1
- Eight Selectable Timer Reset Inputs (five reserved)
- Reset on Rising and Falling Event

Refer to Figure 9-1 for a block diagram of the HLT.

FIGURE 9-1: HLTMR1 BLOCK DIAGRAM



9.6 HLT Control Registers

REGISTER 9-1: HLT1CON0: HLT1 CONTROL REGISTER 0

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	H1OUTPS<3:0>				H1ON	H1CKPS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **Unimplemented:** Read as ‘0’

bit 6-3 **H1OUTPS<3:0>:** Hardware Limit Timer 1 Output Postscaler Select bits

0000 = 1:1 Postscaler
0001 = 1:2 Postscaler
0010 = 1:3 Postscaler
0011 = 1:4 Postscaler
0100 = 1:5 Postscaler
0101 = 1:6 Postscaler
0110 = 1:7 Postscaler
0111 = 1:8 Postscaler
1000 = 1:9 Postscaler
1001 = 1:10 Postscaler
1010 = 1:11 Postscaler
1011 = 1:12 Postscaler
1100 = 1:13 Postscaler
1101 = 1:14 Postscaler
1110 = 1:15 Postscaler
1111 = 1:16 Postscaler

bit 2 **H1ON:** Hardware Limit Timer 1 On bit

1 = Timer is on
0 = Timer is off

bit 1-0 **H1CKPS<1:0>:** Hardware Limit Timer 1 Clock Prescale Select bits

00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

10.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP1 module for standard PWM operation:

1. Disable the CCP1 pin output driver by setting the associated TRIS bit
2. Load the PR2 register with the PWM period value
3. Configure the CCP1 module for the PWM mode by loading the CCP1CON register with the appropriate values
4. Load the CCPR1L register and the DC1B<1:0> bits of the CCP1CON register, with the PWM duty cycle value
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR1 register (see Note below)
   - Configure the T2CKPS bits of the T2CON register with the Timer prescale value
   - Enable the Timer by setting the TMR2ON bit of the T2CON register
6. Enable PWM output pin:
   - Wait until the Timer overflows and the TMR2IF bit of the PIR1 register is set. See Note below
   - Enable the CCP1 pin output driver by clearing the associated TRIS bit

Note:	In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

10.3.3 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 10-1.

EQUATION 10-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \bullet 4 \bullet T_{OSC} \bullet (TMR2\ Prescale\ Value)$$

Note 1: TOSC = 1/FOSC

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: If the PWM duty cycle = 0%, the pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer postscaler (see **Section 8.1 "Timer2 Operation"**) is not used in the determination of the PWM frequency.

10.3.4 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPR1L register and DC1B<1:0> bits of the CCP1CON register. The CCPR1L contains the eight MSbs and the DC1B<1:0> bits of the CCP1CON register contain the two LSbs. CCPR1L and DC1B<1:0> bits of the CCP1CON register can be written to at any time. The duty cycle value is not latched into CCPR1H until after the period completes (i.e. a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPR1H register is read-only.

Equation 10-2 is used to calculate the PWM pulse width.

Equation 10-3 is used to calculate the PWM duty cycle ratio.

EQUATION 10-2: PULSE WIDTH

$$Pulse\ Width = (CCPR1L:CCP1CON<5:4>) \bullet T_{OSC} \bullet (TMR2\ Prescale\ Value)$$

EQUATION 10-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(CCPRxL:CCPxCON<5:4>)}{4(PRx + 1)}$$

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPR1H and 2-bit latch, then the CCP1 pin is cleared (see Figure 10-4).

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TABLE 11-1: SUMMARY OF REGISTERS ASSOCIATED WITH COG

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0	41
APFCON	—	—	—	T1GSEL	—	COG1FSEL	COG1O1SEL	COG1O0SEL	38
COG1PH	—	—	—	—	G1PH<3:0>				87
COG1BLK	G1BLKR<3:0>				G1BLKF<3:0>				87
COG1DB	G1DBR<3:0>				G1DBF<3:0>				87
COG1CON0	G1EN	G1OE1	G1OE0	G1POL1	G1POL0	G1LD	G1CS1	G1CS0	84
COG1CON1	G1FSIM	G1RSIM	G1FS<2:0>			G1RS<2:0>			85
COG1ASD	G1ASDE	G1ARSEN	G1ASDL1	G1ASDL0	G1ASDSHLT	G1ASDSC2	G1ASDSC1	G1ASDSFLT	86
INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF	15
LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	40
PIE2	—	—	C2IE	C1IE	—	COG1IE	—	CCP1IE	17
PIR2	—	—	C2IF	C1IF	—	COG1IF	—	CCP1IF	19
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	40

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by COG.

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

2: See Configuration Word register (Register 17-1) for operation of all register bits.

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12.3 ADC Control Registers

REGISTER 12-1: ADCON0: A/D CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG	CHS<3:0>				GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Conversion Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **VCFG:** Voltage Reference bit
1 = V_{REF} pin
0 = V_{DD}

bit 5-2 **CHS<3:0>:** Analog Channel Select bits
0000 = Channel 00 (AN0)
0001 = Channel 01 (AN1)
0010 = Channel 02 (AN2)
0011 = Channel 03 (AN3)
0100 = Reserved. Do not use.
•
•
•
1101 = Reserved. Do not use.
1110 = Digital-to-Analog Converter (DAC output)
1111 = Fixed Voltage Reference (FVR)

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

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15.2 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.

The CMxCON0 registers (see Register 15-1) contain Control and Status bits for the following:

- Enable
- Output selection
- Output pin enable
- Output polarity
- Speed/Power selection
- Hysteresis enable
- Output synchronization

The CMxCON1 registers (see Register 15-2) contain Control bits for the following:

- Interrupt edge polarity (rising and/or falling)
- Positive input channel selection
- Negative input channel selection

15.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

15.2.2 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register. In order to make the output available for an external connection, the following conditions must be true:

- CxOE bit of the CMxCON0 register must be set
- Corresponding TRIS bit must be cleared
- CxON bit of the CMxCON0 register must be set

Note 1:	The CxOE bit of the CMxCON0 register overrides the PORT data latch. Setting the CxON bit of the CMxCON0 register has no impact on the port override.
2:	The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

15.2.3 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 15-1 shows the output state versus input conditions, including polarity control.

TABLE 15-1: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT
CxVN > CxVP	0	0
CxVN < CxVP	0	1
CxVN > CxVP	1	1
CxVN < CxVP	1	0

15.2.4 COMPARATOR SPEED/POWER SELECTION

The trade-off between speed or power can be optimized during program execution with the CxSP control bit. The default state for this bit is '1' which selects the normal speed mode. Device power consumption can be optimized at the cost of slower comparator propagation delay by clearing the CxSP bit to '0'.

15.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the CxHYS bit of the CMxCON0 register.

See **Section 20.0 "Electrical Specifications"** for more information.

15.4 Timer1 Gate Operation

The output resulting from a comparator operation can be used as a source for gate control of Timer1. See **Section 7.5 "Timer1 Gate"** for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to Timer1. This ensures that Timer1 does not increment while a change in the comparator is occurring.

TABLE 17-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset WDT Reset (Continued) Brown-out Reset(1)	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
CM1CON0	9Dh	0000 0100	0000 0100	uuuu uuuu
CM1CON1	9Eh	0000 ---0	0000 ---0	uuuu ---u
CMOUT	9Fh	---- --00	---- --00	---- --uu
LATA	105h	--xx -xxx	--uu -uuu	--uu -uuu
IOCAN	108h	--00 0000	--00 0000	--uu uuuu
WPUA	10Ch	--00 0000	--00 0000	--uu uuuu
SLRCON0	10Dh	---- -0-0	---- -0-0	---- -u-u
PCON	10Fh	---- --qq	---- --uu(1, 5)	---- --uu
TMR2	110h	0000 0000	0000 0000	uuuu uuuu
PR2	111h	1111 1111	1111 1111	uuuu uuuu
T2CON	112h	-000 0000	-000 0000	-uuu uuuu
HLTMR1	113h	0000 0000	0000 0000	uuuu uuuu
HLTPR1	114h	1111 1111	1111 1111	uuuu uuuu
HLT1CON0	115h	-000 0000	-000 0000	-uuu uuuu
HLT1CON1	116h	---0 0000	---0 0000	---u uuuu
ANSELA	185h	--11 -111	--11 -111	--uu -uuu
APFCON	188h	---0 -000	---0 -000	---u -uuu
OSCTUNE	189h	---0 0000	---u uuuu	---u uuuu
PMCON1	18Ch	---- -000	---- -000	---- -uuu
PMCON2	18Dh	---- ----	---- ----	---- ----
PMADRL	18Eh	0000 0000	0000 0000	uuuu uuuu
PMADRH	18Fh	---- --00	---- --00	---- --uu
PMDATL	190h	0000 0000	0000 0000	uuuu uuuu
PMDATH	191h	--00 0000	--00 0000	--uu uuuu
COG1PH	192h	---- xxxx	---- uuuu	---- uuuu
COG1BLK	193h	xxxx xxxx	uuuu uuuu	uuuu uuuu
COG1DB	194h	xxxx xxxx	uuuu uuuu	uuuu uuuu
COG1CON0	195h	0000 0000	0000 0000	uuuu uuuu
COG1CON1	196h	--00 0000	--00 0000	--uu uuuu
COG1ASD	197h	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If V_{DD} goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIRx will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 17-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

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17.4.3 PORTA INTERRUPT-ON-CHANGE

An input change on PORTA sets the IOCIF bit of the INTCON register. The interrupt can be enabled/ disabled by setting/clearing the IOCIE bit of the INTCON register. Plus, individual pins can be configured through the IOC register.

Note:	If a change on the I/O pin should occur when any PORTA operation is being executed, then the IOCIF interrupt flag may not get set.

FIGURE 17-7: INTERRUPT LOGIC

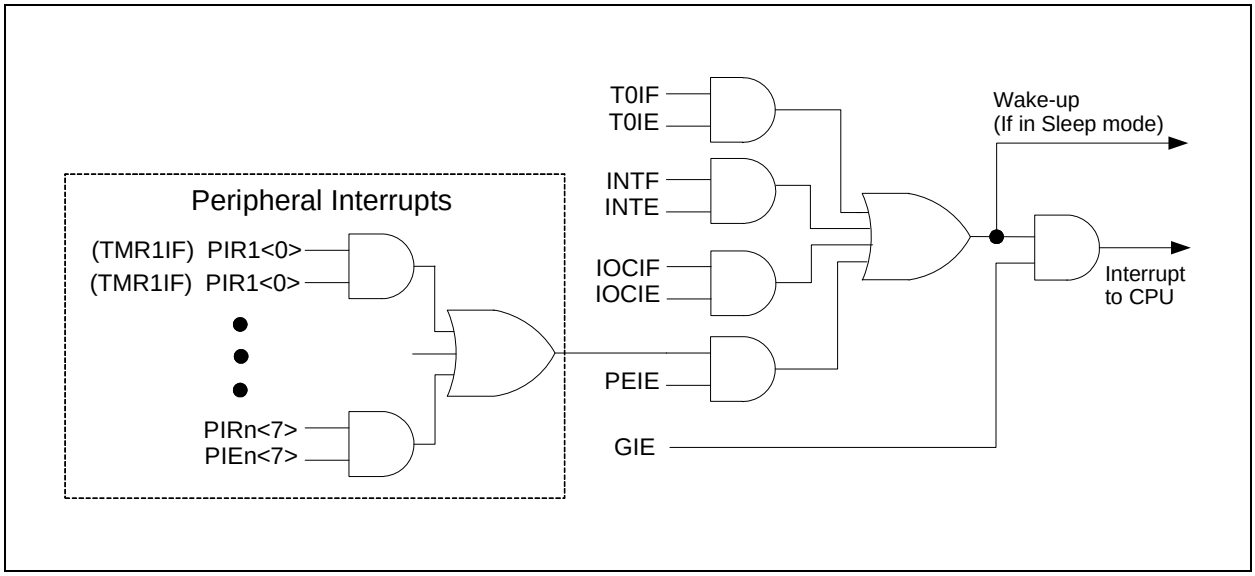
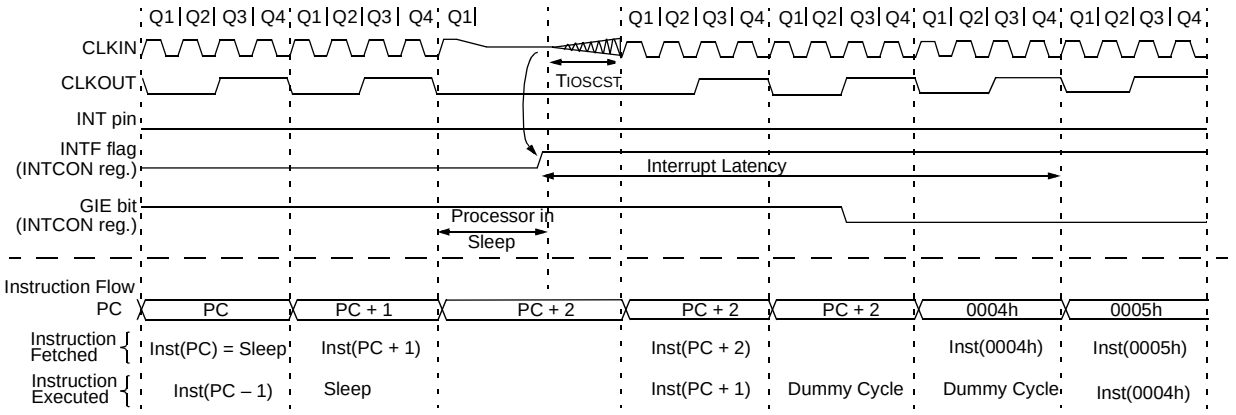


FIGURE 17-10: WAKE-UP FROM SLEEP THROUGH INTERRUPT(1,2)



Note 1: HFINTOSC Oscillator mode assumed.

2: GIE = '1' assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = '0', execution will continue in-line.

17.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note:	The entire Flash program memory will be erased when the code protection is turned off. See the *"PIC12F752/HV752 Flash Memory Programming Specification"* (DS41561) for more information.

17.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify mode. Only the Least Significant seven bits of the ID locations are reported when using MPLAB® IDE.

TABLE 20-2: SUPPLY CURRENT (I_{DD})(1,2)

PIC12F752			Standard Operating Conditions (unless otherwise stated)					
PIC12HV752								
Param. No.	Device Characteristics	Min.	Typ.†	Max. 85°C	Max. 125°C	Units	Conditions	
							V_{DD}	Note
	Supply Current (I_{DD})(1, 2)							
D010		—	13	25	25	µA	2.0	F_{OSC} = 31 kHz LFINTOSC mode
		—	19	29	29	µA	3.0	
		—	32	51	51	µA	5.0	
D010		—	160	230	230	µA	2.0	F_{OSC} = 31 kHz LFINTOSC mode
		—	240	310	310	µA	3.0	
		—	280	400	400	µA	4.5	
D016		—	75	280	280	µA	2.0	F_{OSC} = 1 MHz EC Oscillator mode
		—	155	320	320	µA	3.0	
		—	345	530	530	µA	5.0	
D016		—	215	310	310	µA	2.0	F_{OSC} = 1 MHz EC Oscillator mode
		—	375	470	470	µA	3.0	
		—	570	650	650	µA	4.5	
D011		—	130	280	280	µA	2.0	F_{OSC} = 1 MHz HFINTOSC mode
		—	175	320	320	µA	3.0	
		—	290	535	535	µA	5.0	
D011		—	195	296	296	µA	2.0	F_{OSC} = 1 MHz HFINTOSC mode
		—	315	440	440	µA	3.0	
		—	425	650	650	µA	4.5	
D012		—	185	340	340	µA	2.0	F_{OSC} = 4 MHz EC Oscillator mode
		—	325	475	475	µA	3.0	
		—	665	845	845	µA	5.0	
D012		—	330	475	475	µA	2.0	F_{OSC} = 4 MHz EC Oscillator mode
		—	550	800	800	µA	3.0	
		—	850	1200	1200	µA	4.5	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{SS}; $\overline{MCLR}$ = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

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TABLE 20-2: SUPPLY CURRENT (I_{DD})(1,2) (CONTINUED)

PIC12F752			Standard Operating Conditions (unless otherwise stated)					
PIC12HV752								
Param. No.	Device Characteristics	Min.	Typ.†	Max. 85°C	Max. 125°C	Units	Conditions	
							V_{DD}	Note
	Supply Current (I_{DD})(1, 2)							
D013		—	245	340	340	µA	2.0	F_{OSC} = 4 MHz HFINTOSC mode
		—	360	485	485	µA	3.0	
		—	620	845	845	µA	5.0	
D013		—	310	435	435	µA	2.0	F_{OSC} = 4 MHz HFINTOSC mode
		—	500	700	700	µA	3.0	
		—	740	1100	1100	µA	4.5	
D014		—	395	550	550	µA	2.0	F_{OSC} = 8 MHz HFINTOSC mode
		—	620	850	850	µA	3.0	
		—	1.2	1.6	1.6	mA	5.0	
D014		—	460	650	650	µA	2.0	F_{OSC} = 8 MHz HFINTOSC mode
		—	750	1100	1100	µA	3.0	
		—	1.2	1.6	1.6	mA	4.5	
D015		—	1.9	2.6	2.6	mA	4.5	F_{OSC} = 20 MHz EC Oscillator mode
		—	2.2	3	3	mA	5.0	
D015		—	2.1	3	3	mA	4.5	F_{OSC} = 20 MHz EC Oscillator mode

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{SS}; $\overline{MCLR}$ = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

TABLE 20-3: POWER-DOWN CURRENTS (I_{PD}) (1,2)

PIC12F752		Standard Operating Conditions (unless otherwise stated) Sleep mode						
PIC12HV752								
Param. No.	Device Characteristics	Min.	Typ.†	Max. 85°C	Max. 125°C	Units	Conditions	
							V_{DD}	Note
	Power-down Base Current (I_{PD})(2)							
D020		—	0.05	1.2	4.5	µA	2.0	WDT, BOR, Comparator, V_{REF} and T1OSC disabled
		—	0.15	1.6	5.5	µA	3.0	
		—	0.35	2.1	9	µA	5.0	
D020		—	135	200	200	µA	2.0	
		—	210	280	280	µA	3.0	
		—	260	350	350	µA	4.5	
	Power-down Base Current (I_{PD})(2, 3)							
D021		—	0.5	1.5	5	µA	2.0	WDT Current(1)
		—	2.5	4	8	µA	3.0	
		—	9.5	17	19	µA	5.0	
D021		—	135	200	200	µA	2.0	
		—	210	285	285	µA	3.0	
		—	265	360	360	µA	4.5	
D022		—	5	9	15	µA	3.0	BOR Current(1)
		—	6	12	19	µA	5.0	
D022		—	215	285	285	µA	3.0	
		—	265	360	360	µA	4.5	
D023		—	160	235	245	µA	2.0	CxSP = 1, Comparator Current(1), single comparator enabled
		—	180	270	280	µA	3.0	
		—	220	350	360	µA	5.0	
D023		—	280	415	415	µA	2.0	
		—	385	540	540	µA	3.0	
		—	455	735	735	µA	4.5	
D024		—	50	70	75	µA	2.0	CxSP = 0, Comparator Current(1), single comparator enabled
		—	55	80	90	µA	3.0	
		—	70	90	120	µA	5.0	
D024		—	185	205	205	µA	2.0	
		—	265	315	315	µA	3.0	
		—	320	445	445	µA	4.5	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral Δ current can be determined by subtracting the base I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: Shunt regulator is always on and always draws operating current.

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20.4 AC Characteristics: PIC12F752/HV752 (Industrial, Extended)

FIGURE 20-4: CLOCK TIMING

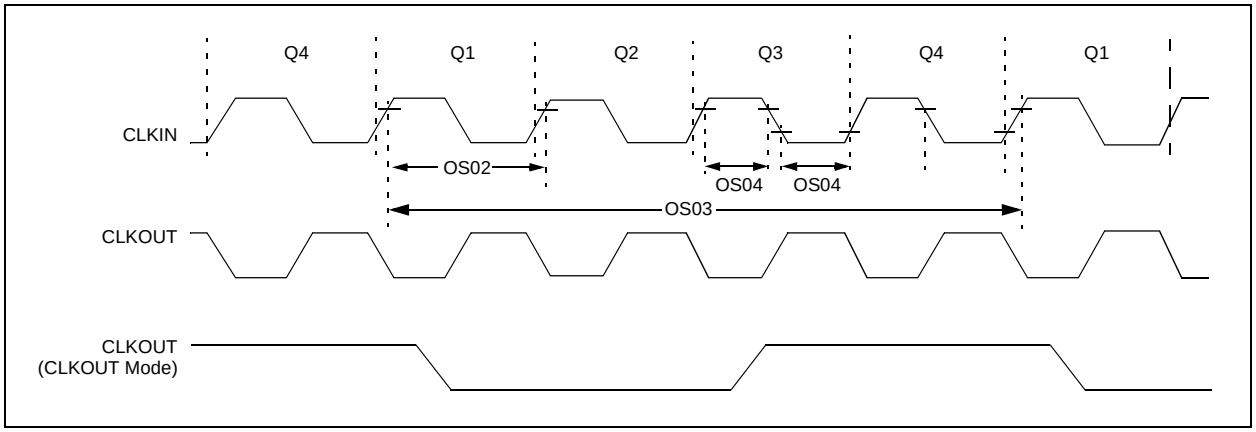

TABLE 20-7: CLOCK OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
OS01	FOSC	External CLKIN Frequency(1)	DC	—	20	MHz	EC Oscillator mode
OS02	TOSC	External CLKIN Period(1)	50	—	∞	ns	EC Oscillator mode
OS03	TCY	Instruction Cycle Time(1)	200	TCY	DC	ns	TCY = 4/FOSC

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to CLKIN pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

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FIGURE 21-32: VOH vs. IOH, RA0/RA2, OVER TEMPERATURE, VDD = 3.0V

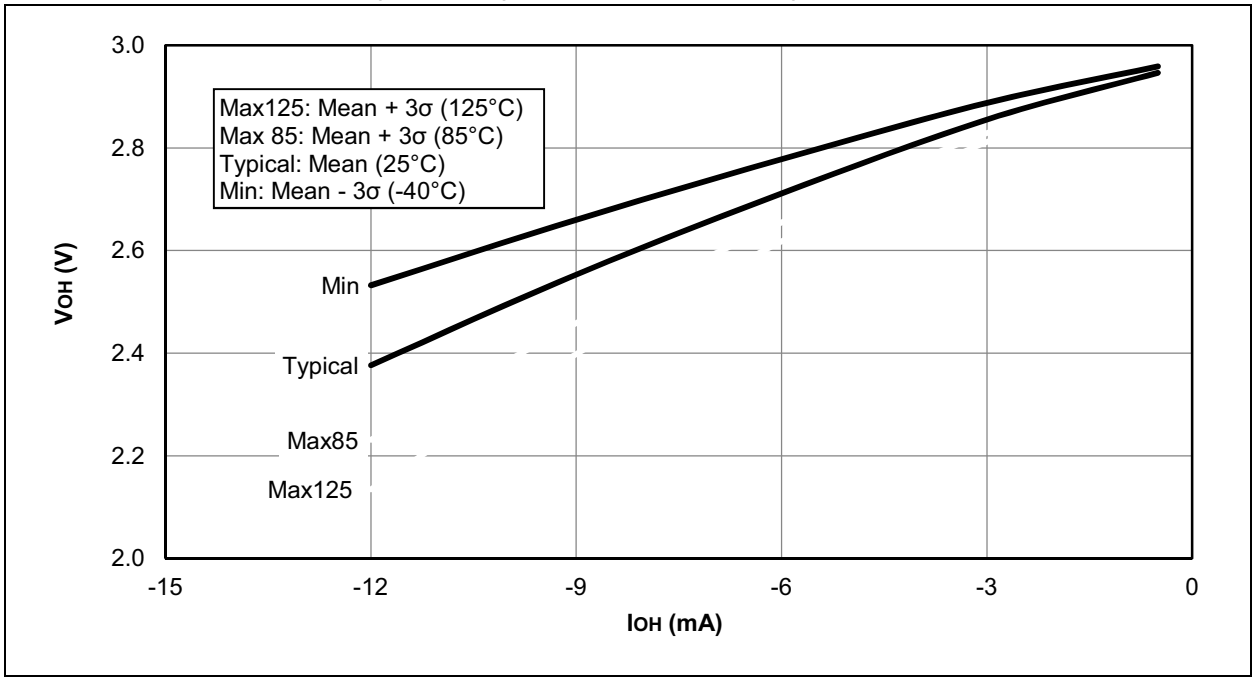
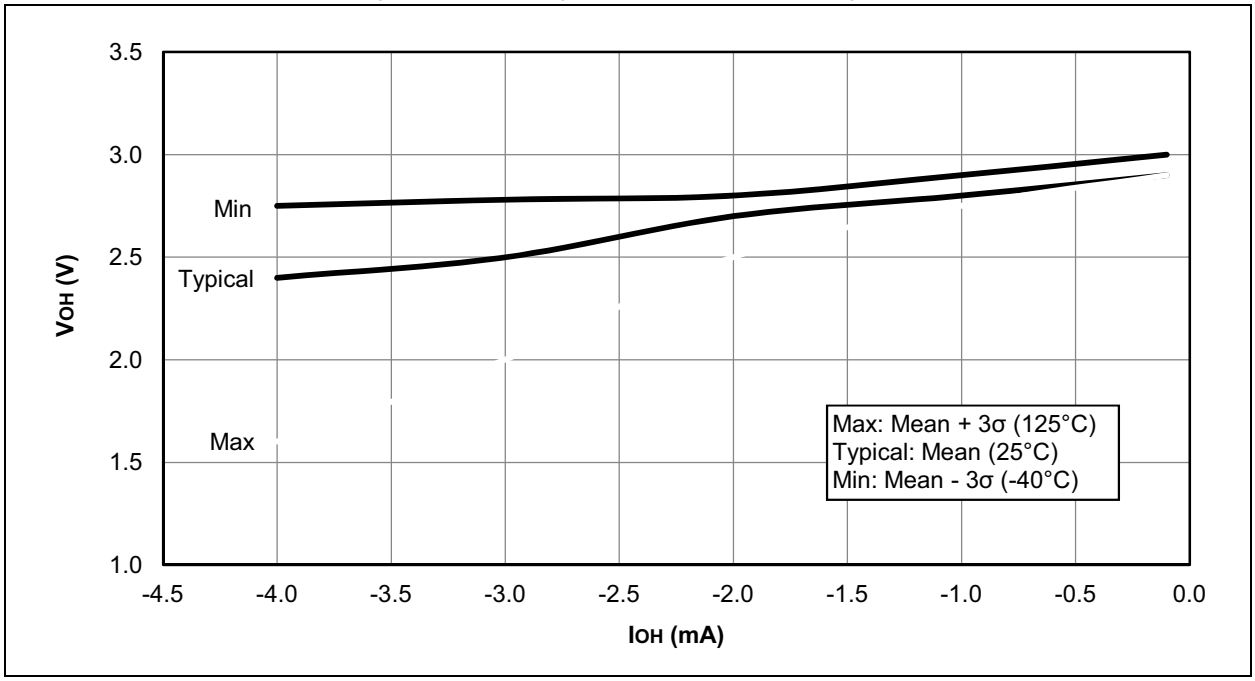


FIGURE 21-33: VOH vs. IOH, RA1/RA4/RA5, OVER TEMPERATURE, VDD = 3.0V



PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	PIC12F752 PIC12HV752	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package:	P SN MF	= Plastic DIP (PDIP) = 8-lead Small Outline (3.90 mm) (SOIC) = 8-lead Plastic Dual Flat, No Lead (3x3) (DFN)
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC12F752T - I/MF 301
Tape and Reel,
Industrial temperature,
DFN 3x3 package,
QTP pattern #301

b) PIC12F752 - E/P
Extended temperature
PDIP package

c) PIC12F752 - E/SN
Extended temperature,
SOIC package

d) PIC12HV752 - E/MF
Extended temperature,
DFN 3x3 package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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