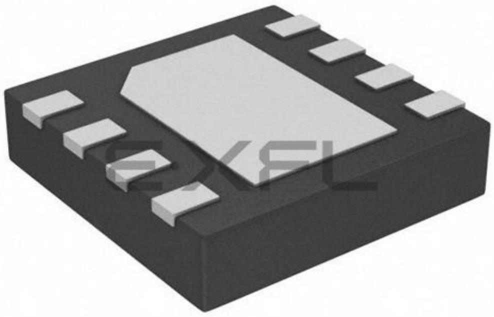

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f752t-i-mf

3.3 Flash Program Memory Control Registers

REGISTER 3-1: PMDATL: PROGRAM MEMORY DATA LOW BYTE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMDATL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **PMDATL<7:0>**: Eight Least Significant Data bits to Write or Read from Program Memory

REGISTER 3-2: PMADRL: PROGRAM MEMORY ADDRESS LOW BYTE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMADRL<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **PMADRL<7:0>**: Eight Least Significant Address bits for Program Memory Read/Write Operation

REGISTER 3-3: PMDATH: PROGRAM MEMORY DATA HIGH BYTE REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	PMDATH<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **PMDATH<5:0>**: Six Most Significant Data bits from Program Memory

REGISTER 3-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH BYTE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	PMADRH<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1-0 **PMADRH<1:0>**: Specifies the two Most Significant Address bits or High bits for Program Memory Reads.

4.5.1 OSCTUNE REGISTER

The oscillator is factory-calibrated, but can be adjusted in software by writing to the OSCTUNE register (Register 4-2).

The default value of the OSCTUNE register is ‘0’. The value is a 5-bit two’s complement number.

When the OSCTUNE register is modified, the frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

REGISTER 4-2: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	TUN<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **TUN<4:0>:** Frequency Tuning bits
01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Oscillator module is running at the calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	—	—	IRCF<1:0>		—	HTS	LTS	—	35
OSCTUNE	—	—	—	TUN<4:0>					36

Legend: x = unknown, u = unchanged, – = unimplemented locations read as ‘0’. Shaded cells are not used by oscillators.
Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.
2: See Configuration Word register (Register 17-1) for operation of all register bits.

TABLE 4-3: SUMMARY OF CONFIGURATION WORD CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG	13:8	—	—	$\overline{\text{DEBUG}}$	$\overline{\text{CLKOUTEN}}$	WRT<1:0>		BOREN<1:0>		126
	7:0	—	$\overline{\text{CP}}$	$\overline{\text{MCLRE}}$	$\overline{\text{PWRTE}}$	WDTE	—	—	FOSC0	

Legend: — = unimplemented location, read as ‘1’. Shaded cells are not used by oscillator module.

9.1 HLT Operation

The clock input to the HLT module is the system instruction clock (FOSC/4). HLTMR1 increments on each rising clock edge.

A 4-bit counter/prescaler on the clock input provides the following prescale options:

- Direct Input
- Divide-by-4
- Divide-by-16

The prescale options are selected by the prescaler control bits, H1CKPS<1:0> of the HLT1CON0 register.

The value of HLTMR1 is compared to that of the Period register, HLTPR1, on each clock cycle. When the two values match, then the comparator generates a match signal as the HLTimer1 output. This signal also resets the value of HLTMR1 to 00h on the next clock rising edge and drives the output counter/postscaler (see **Section 9.2 “HLT Interrupt”**).

The time from HLT reset to the HLT output pulse is calculated as shown in Equation 9-1 below.

EQUATION 9-1: HLT OUTPUT

$$HLT\ Time = (HLTPR1 + 2) \bullet 4 / Fosc$$

Unexpected operation may occur for HLT periods less than half the period of the expected external HLT Reset input.

The HLTMR1 and HLTPR1 registers are both directly readable and writable. The HLTMR1 register is cleared on any device Reset, whereas the HLTPR1 register initializes to FFh. Both the prescaler and postscaler counters are cleared on any of the following events:

- A Write to the HLTMR1 Register
- A Write to the HLT1CON0 Register
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- $\overline{\text{MCLR}}$ Reset
- Watchdog Timer (WDT) Reset
- Stack Overflow Reset
- Stack Underflow Reset
- RESET Instruction.

> **Note:** HLTMR1 is not cleared when HLT1CON0 is written.

9.2 HLT Interrupt

The HLT can also generate an optional device interrupt. The HLTMR1 output signal (HLTMR1-to-HLTPR1 match) provides the input for the 4-bit counter/postscaler. The overflow output of the postscaler sets the HLTMR1IF bit of the PIR1 register. The interrupt is enabled by setting the HLTMR1 Match Interrupt Enable bit, HLTMR1IE of the PIE1 register.

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, H1OUTPS<3:0>, of the HLT1CON0 register.

9.3 Peripheral Resets

Resets driven from the selected peripheral output prevents the HLTMR1 from matching the HLTPR1 register and generating an output. In this manner, the HLT can be used as a hardware time limit to other peripherals.

In this device, the primary purpose of the HLT is to limit the COG PWM duty cycle. Normally, the COG operation uses analog feedback to determine the PWM duty cycle. The same feedback signal is used as an HLT Reset input. The HLTPR1 register is set to occur at the maximum allowed duty cycle. If the analog feedback to the COG exceeds the maximum time, then an HLTMR1-to-HLTPR1 match will occur and generate the output needed to limit the COG drive output.

The HLTMR1 can be reset by one of several selectable peripheral sources. Reset inputs include:

- CCP1 Output
- Comparator 1 Output
- Comparator 2 Output

The Reset input is selected with the H1ERS<2:0> bits of the HLT1CON1 register.

HLTMR1 Resets are synchronous with the HLT clock, i.e. HLTMR1 is cleared on the rising edge of the HLT clock after the enabled Reset event occurs.

The Reset can be enabled to occur on the rising and falling input event. Rising and falling event enables are selected with the respective H1REREN and H1FEREN bits of the HLT1CON1 register. External Resets do not cause an HLTMR1 output event.

9.4 HLTimer1 Output

The unscaled output of HLTMR1 is available only to the COG module, where it is used as a selectable limit to the maximum COG period.

9.5 HLT Operation During Sleep

The HLT cannot be operated while the processor is in Sleep mode. The contents of the HLTMR1 register will remain unchanged while the processor is in Sleep mode.

11.7 Phase Delay

It is possible to delay the assertion of the rising event. This is accomplished by placing a non-zero value in COGxPH register. Refer to Register 11-6 and Figure 11-3 for COG operation with CCP1 and phase delay. The delay from the input rising event signal switching to the actual assertion of the events is calculated the same as the dead-band and blanking delays. Please see Equation 11-1.

When the COGxPH value is '0', phase delay is disabled and the phase delay counter output is true, thereby, allowing the event signal to pass straight through to complementary output driver flop.

11.7.1 CUMULATIVE UNCERTAINTY

It is not possible to create more than one COG_clock of uncertainty by successive stages. Consider that the phase delay stage comes after the blanking stage, the dead-band stage comes after either the blanking or phase delay stages, and the blanking stage comes after the dead-band stage. When the preceding stage is enabled, the output of that stage is necessarily synchronous with the COG_clock, which removes any possibility of uncertainty in the succeeding stage.

EQUATION 11-1: PHASE, DEAD-BAND, AND BLANKING TIME CALCULATION

$$T_{\text{min}} = \frac{\text{Count}}{F_{COG\_clock}}$$

$$T_{\text{max}} = \frac{\text{Count} + 1}{F_{COG\_clock}}$$

$$T_{\text{uncertainty}} = T_{\text{max}} - T_{\text{min}}$$

Also:

$$T_{\text{uncertainty}} = \frac{1}{F_{COG\_clock}}$$

Where:

T	Count
Phase Delay	GxPH<3:0>
Rising Dead Band	GxDBR<3:0>
Falling Dead Band	GxDBF<3:0>
Rising Event Blanking	GxBLKR<3:0>
Falling Event Blanking	GxBLKF<3:0>

EXAMPLE 11-1: TIMER UNCERTAINTY

Given:

$$Count = Ah = 10d$$
$$F_{COG\_\text{Clock}} = 8\text{MHz}$$

Therefore:

$$T_{\text{uncertainty}} = \frac{1}{F_{COG\_\text{clock}}} = \frac{1}{8MHz} = 125ns$$

Proof:

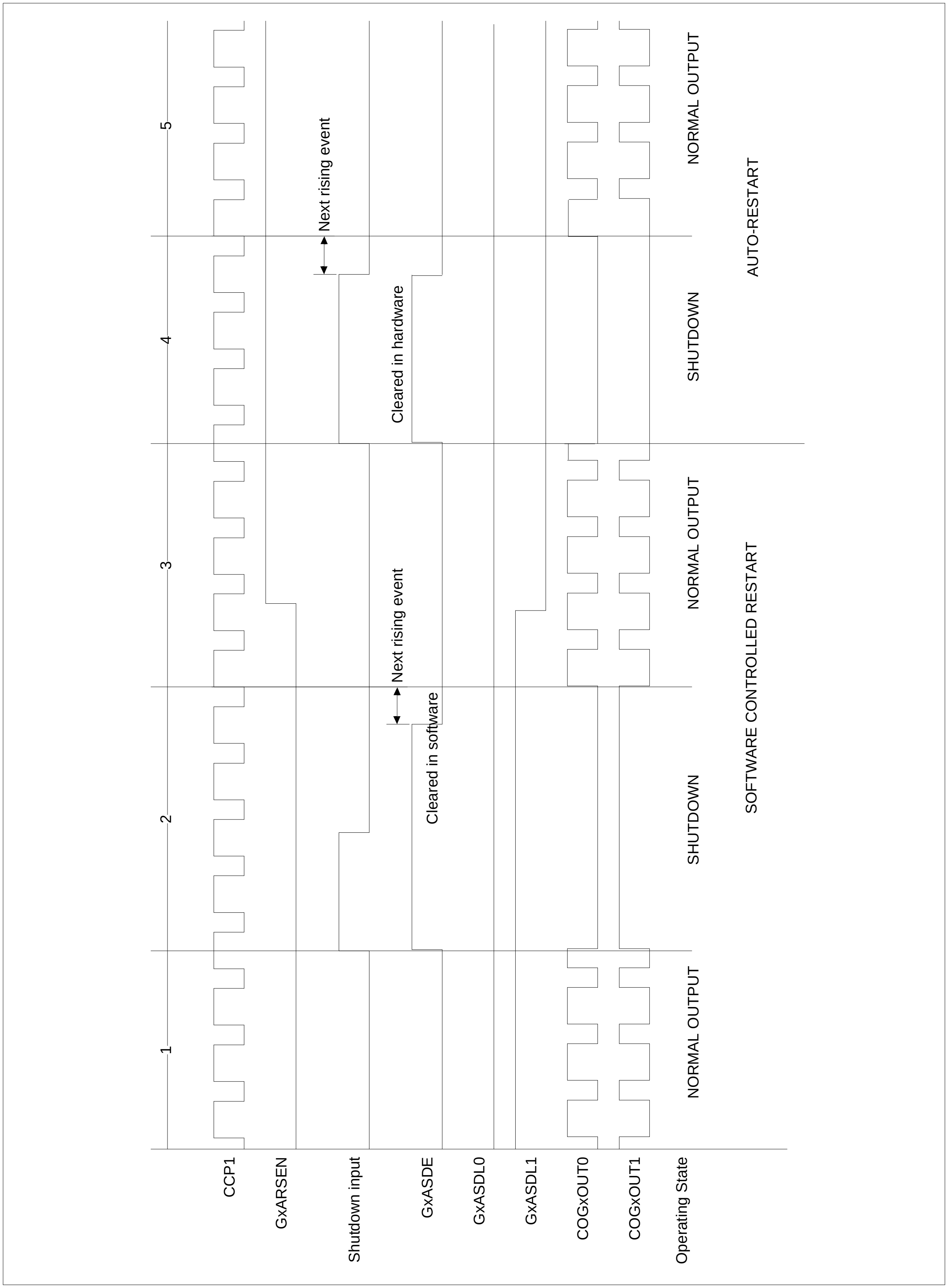
$$T_{\text{min}} = \frac{Count}{F_{COG\_\text{clock}}} = 125ns \bullet 10d = 1.25\mu s$$

$$T_{\text{max}} = \frac{Count + 1}{F_{COG\_\text{clock}}} = 125ns \bullet (10d + 1) = 1.375\mu s$$

Therefore:

$$T_{\text{uncertainty}} = T_{\text{max}} - T_{\text{min}} = 1.375\mu s - 1.25\mu s = 125ns$$

FIGURE 11-5: AUTO-SHUTDOWN WAVEFORM – CCP1 AS RISING AND FALLING EVENT INPUT SOURCE



12.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).

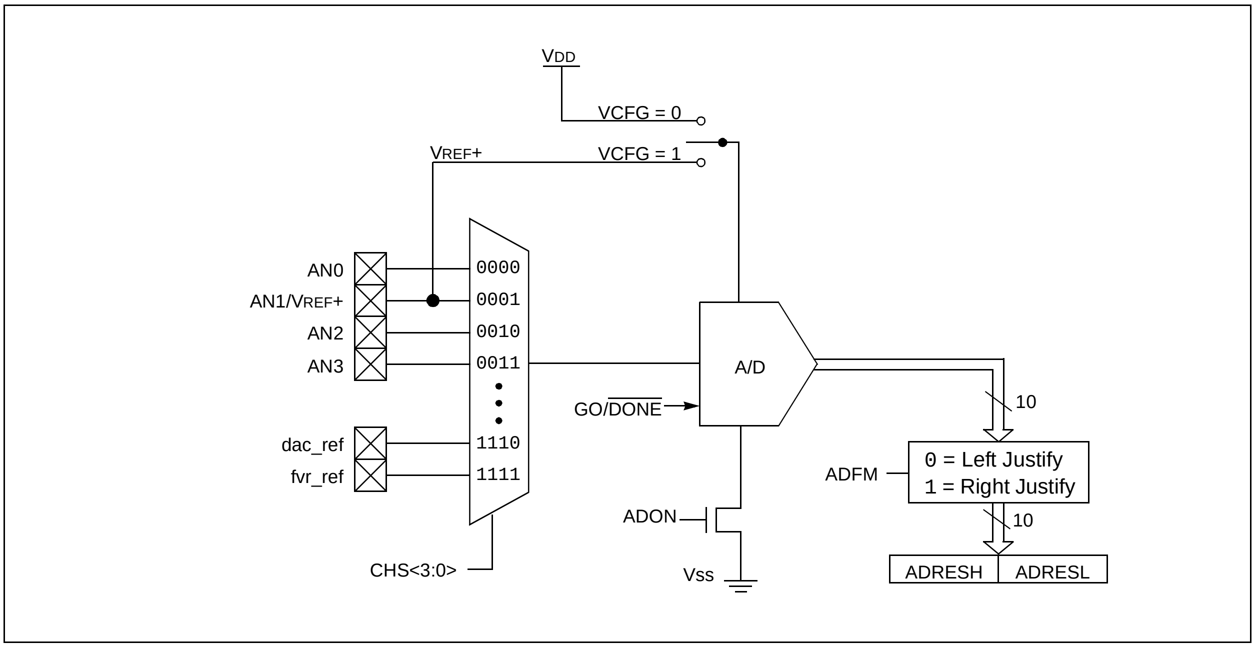
The ADC voltage reference is software selectable to either VDD or a voltage applied to the external reference pins.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

Figure 12-1 shows the block diagram of the ADC.

Note:	The ADRESL and ADRESH registers are read-only.

FIGURE 12-1: ADC BLOCK DIAGRAM



12.4 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (C_{HOLD}) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 12-4. The source impedance (R_S) and the internal sampling switch (R_{SS}) impedance directly affect the time required to charge the capacitor C_{HOLD}. The sampling switch (R_{SS}) impedance varies over the device voltage (V_{DD}), see Figure 12-4. **The maximum recommended impedance for analog sources is 10 kΩ**. As the source impedance is decreased, the acquisition time may be decreased.

After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 12-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 12-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C$ *and external impedance of* $10k\Omega$ $5.0V$ V_{DD}

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \\ &= 2\mu s + T_C + [(Temperature - 25°C)(0.05\mu s/°C)] \end{aligned}$$

The value for T_C *can be approximated with the following equations:*

$$V_{APPLIED}\left(1 - \frac{1}{2047}\right) = V_{CHOLD} \qquad ;[1]\ V_{CHOLD} \text{ charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \qquad ;[2]\ V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{2047}\right) \qquad ;\text{combining [1] and [2]}$$

Solving for T_C:

$$\begin{aligned} T_C &= -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ ln(1/2047) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ ln(0.0004885) \\ &= 1.37\mu s \end{aligned}$$

Therefore:

$$\begin{aligned} T_{ACQ} &= 2\mu s + 1.37\mu s + [(50°C - 25°C)(0.05\mu s/°C)] \\ &= 4.67\mu s \end{aligned}$$

Note 1: The reference voltage (V_{REF}) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (C_{HOLD}) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

FIGURE 12-4: ANALOG INPUT MODEL

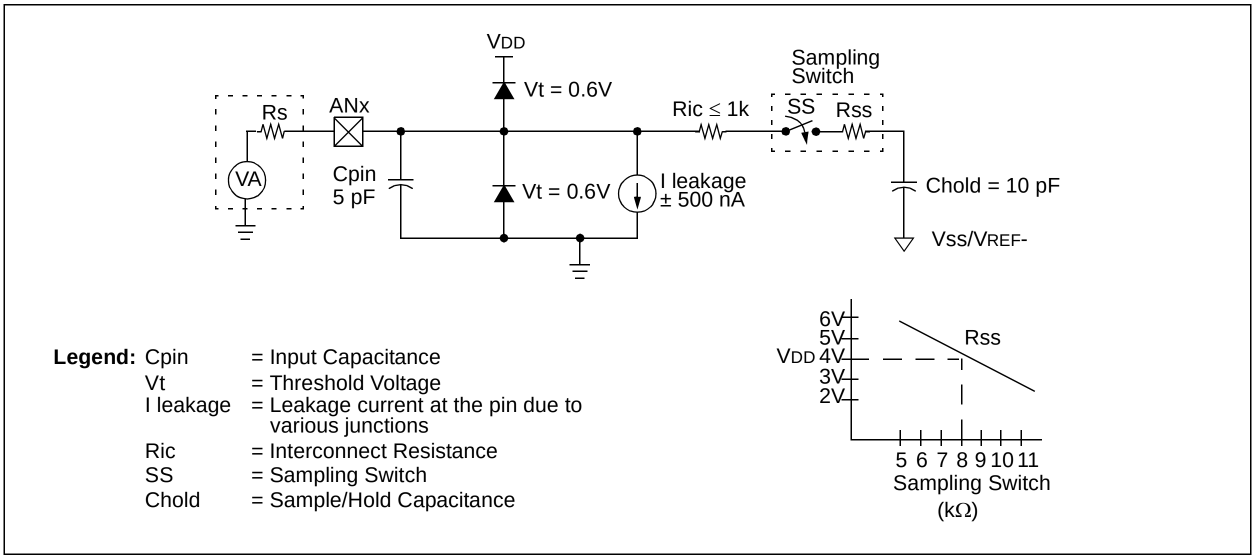
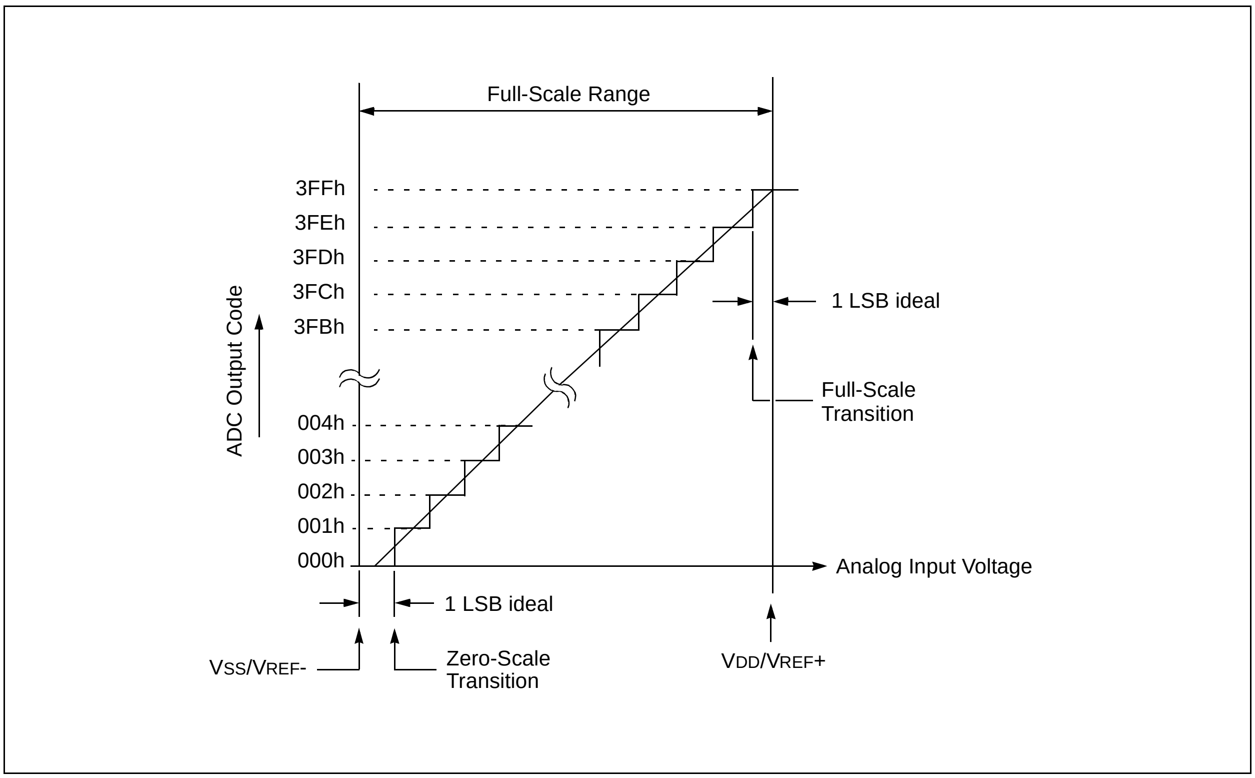


FIGURE 12-5: ADC TRANSFER FUNCTION



14.8 DAC Control Registers

REGISTER 14-1: DACCON0: VOLTAGE REFERENCE CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	U-0	U-0
DACEN	DACRNG	DACOE	—	—	DACPSS	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **DACEN:** DAC Enable bit
1 = DAC is enabled
0 = DAC is disabled

bit 6 **DACRNG:** DAC Range Selection bit(1)
1 = DAC is operating in Full Range mode
0 = DAC is operating in Limited Range mode

bit 5 **DACOE:** DAC Voltage Output Enable bit
1 = DAC reference output is enabled to the DACOUT pin(2)
0 = DAC reference output is disabled

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **DACPSS:** DAC Positive Source Select bits
0 = V_{DD}
1 = V_{REF}+ pin

bit 1-0 **Unimplemented:** Read as '0'

Note 1: Refer to Equation 14-1.
2: The DACOUT pin configuration requires additional control bits in the FVRCON register (see Figure 14-3).

REGISTER 14-2: DACCON1: VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	DACR<4:0>				
bit 7							bit 0

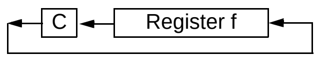
Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **DACR<4:0>:** DAC Voltage Output Select bits
1 1111 = DAC Voltage Maximum Output
•
•
•
0 0000 = DAC Voltage Minimum Output

Note 1: Refer to Equation 14-1 to calculate the value of the DAC Voltage Output.

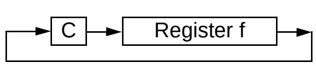
RLF	**Rotate Left f through Carry**
Syntax:	[*label*] RLF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register ‘f’ are rotated one bit to the left through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.



Words:	1
Cycles:	1
Example:	`RLF REG1,0`

Before Instruction
```
REG1 = 1110 0110
C    = 0
```
After Instruction
```
REG1 = 1110 0110
W    = 1100 1100
C    = 1
```

RRF	**Rotate Right f through Carry**
Syntax:	[*label*] RRF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	See description below
Status Affected:	C
Description:	The contents of register ‘f’ are rotated one bit to the right through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.



SLEEP	**Enter Sleep mode**
Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h → WDT, 0 → WDT prescaler, 1 → $\overline{TO}$, 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

SUBLW	**Subtract W from literal**
Syntax:	[*label*] SUBLW k
Operands:	0 ≤ k ≤ 255
Operation:	k - (W) → (W)
Status Affected:	C, DC, Z
Description:	The W register is subtracted (2’s complement method) from the 8-bit literal ‘k’. The result is placed in the W register.

Result	Condition
C = 0	W > k
C = 1	W ≤ k
DC = 0	W<3:0> > k<3:0>
DC = 1	W<3:0> ≤ k<3:0>

17.3.5 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

- PWRT time-out is invoked after POR has expired
- OST is activated after the PWRT time-out has expired

The total time-out will vary based on oscillator configuration and $\overline{\text{PWRTE}}$ bit status. For example, in EC mode with $\overline{\text{PWRTE}}$ bit erased (PWRT disabled), there will be no time-out at all. Figure 17-4, Figure 17-5 and Figure 17-6 depict time-out sequences.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then, bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 17-5). This is useful for testing purposes or to synchronize more than one PIC12F752/HV752 device operating in parallel.

Table 17-5 shows the Reset conditions for some special registers, while Table 17-4 shows the Reset conditions for all the registers.

17.3.6 POWER CONTROL (PCON) REGISTER

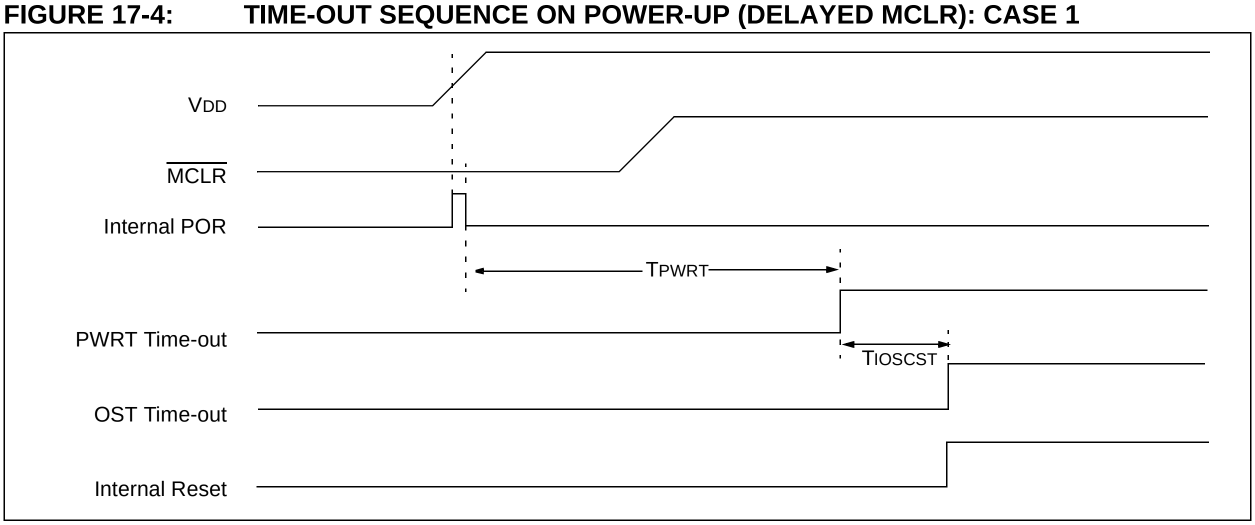
The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset occurred last.

Bit 0 is $\overline{\text{BOR}}$ (Brown-out). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}}$ = 0, indicating that a Brown-out has occurred. The $\overline{\text{BOR}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{\text{POR}}$ is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see **Section 17.3.4 "Brown-out Reset (BOR)"**.

FIGURE 17-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 1



20.2 DC Characteristics

TABLE 20-1: SUPPLY VOLTAGE

PIC12F752			Standard Operating Conditions (unless otherwise stated)				
PIC12HV752							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
D001	VDD	**Supply Voltage**					
			VDDMIN		VDDMAX		
			2.0	—	5.5	V	FOSC ≤ 8 MHz
			3.0	—	5.5	V	FOSC ≤ 10 MHz
			4.5	—	5.5	V	FOSC≤ 20 MHz
D001			2.0	—	5.0	V	FOSC ≤ 8 MHz(2)
			3.0	—	5.0	V	FOSC ≤ 10 MHz(2)
			4.5	—	5.0	V	FOSC ≤ 20 MHz(2)
D002*	VDR	**RAM Data Retention Voltage(1)**					
			1.5	—	—	V	Device in Sleep mode
D002			1.5	—	—	V	Device in Sleep mode
D003*	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal					
			—	1.6	—	V	
D003			—	1.6	—	V	
D004*	SVDD	**VDD Rise Rate** to ensure VDD Rise Rate internal Power-on Reset signal					
			0.05	—	—	V/ms	See Table 17-1 for details.

* These parameters are characterized but not tested.

† Data in “Typ.” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: On the PIC12HV752, VDD is regulated by a Shunt Regulator and is dependent on series resistor (connected between the unregulated supply voltage and the VDD pin) to limit the current to 50 mA. See **Section “”** for design requirements.

TABLE 20-10: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
30	T_{MCL}	$\overline{MCLR}$ Pulse Width (low)	2 5	— —	— —	μs μs	V_{DD} = 5V, -40°C to +85°C V_{DD} = 5V, -40°C to +125°C
31	T_{WDTLP}	Low-Power Watchdog Timer Time-out Period	10 10	20 20	30 35	ms ms	V_{DD} = 5V, -40°C to +85°C V_{DD} = 5V, -40°C to +125°C
32*	T_{PWRT}	Power-up Timer Period, PWRTE = 0 (No Prescaler)	40	65	140	ms	
33*	T_{IOZ}	I/O high-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.0	μs	
34	V_{BOR}	Brown-out Reset Voltage (1)	2	2.15	2.3	V	
35*	V_{HYST}	Brown-out Reset Hysteresis	—	100	—	mV	-40°C ≤ T_A ≤ +85°C
36*	T_{BOR}	Brown-out Reset DC Minimum Detection Period	100	—	—	μs	V_{DD} ≤ V_{BOR}

* These parameters are characterized but not tested.

† Data in “Typ.” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these voltage tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

FIGURE 21-5: IDD TYPICAL, HFINTOSC, PIC12HV752 ONLY

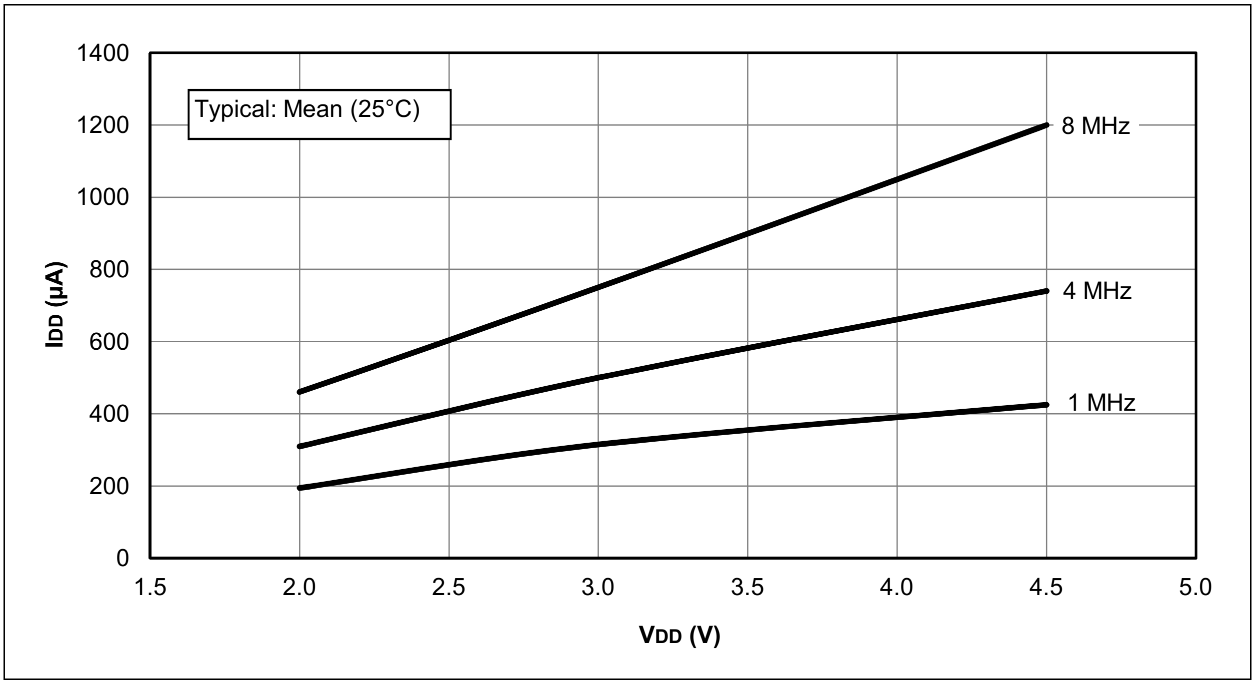


FIGURE 21-6: IDD MAXIMUM, HFINTOSC, PIC12HV752 ONLY

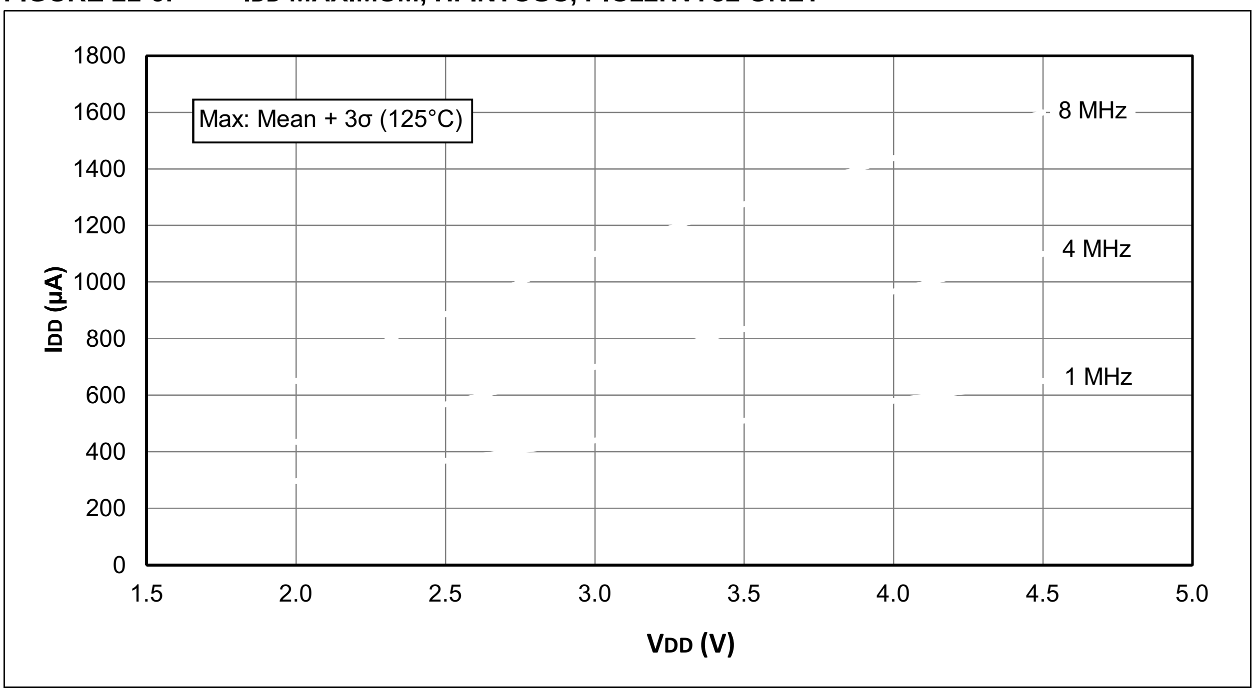


FIGURE 21-7: IDD TYPICAL, EXTERNAL CLOCK (EC), PIC12F752 ONLY

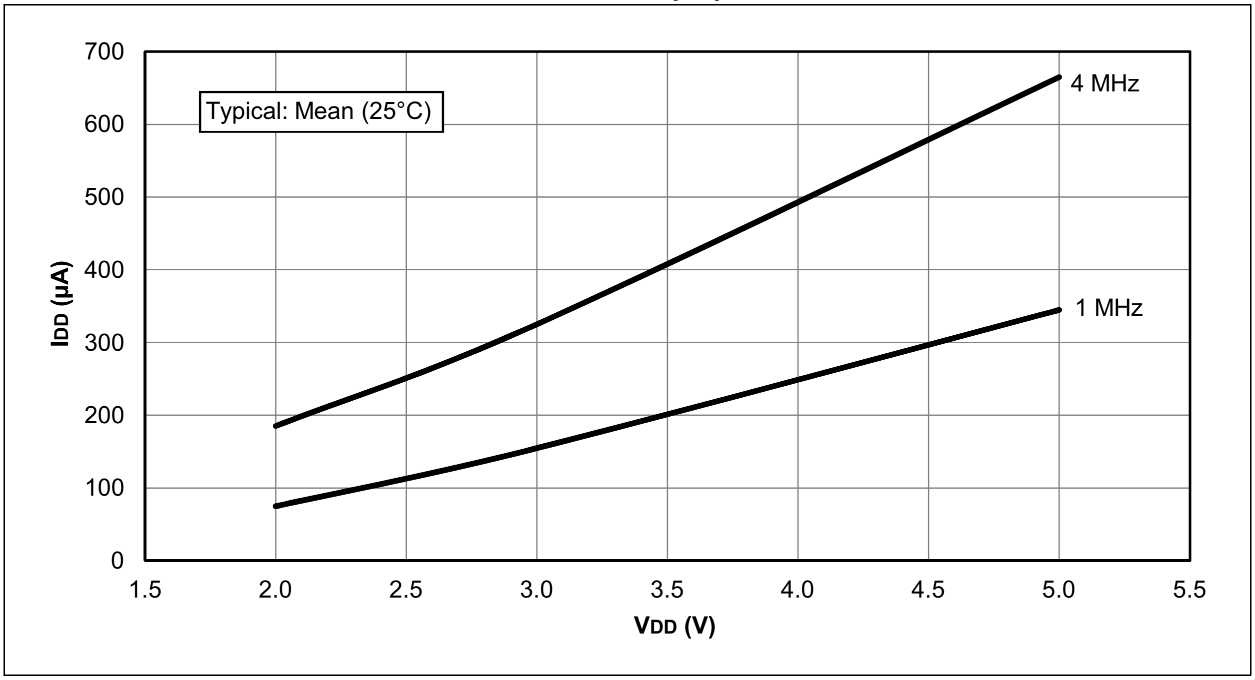


FIGURE 21-8: IDD MAXIMUM, EXTERNAL CLOCK (EC), PIC12F752 ONLY

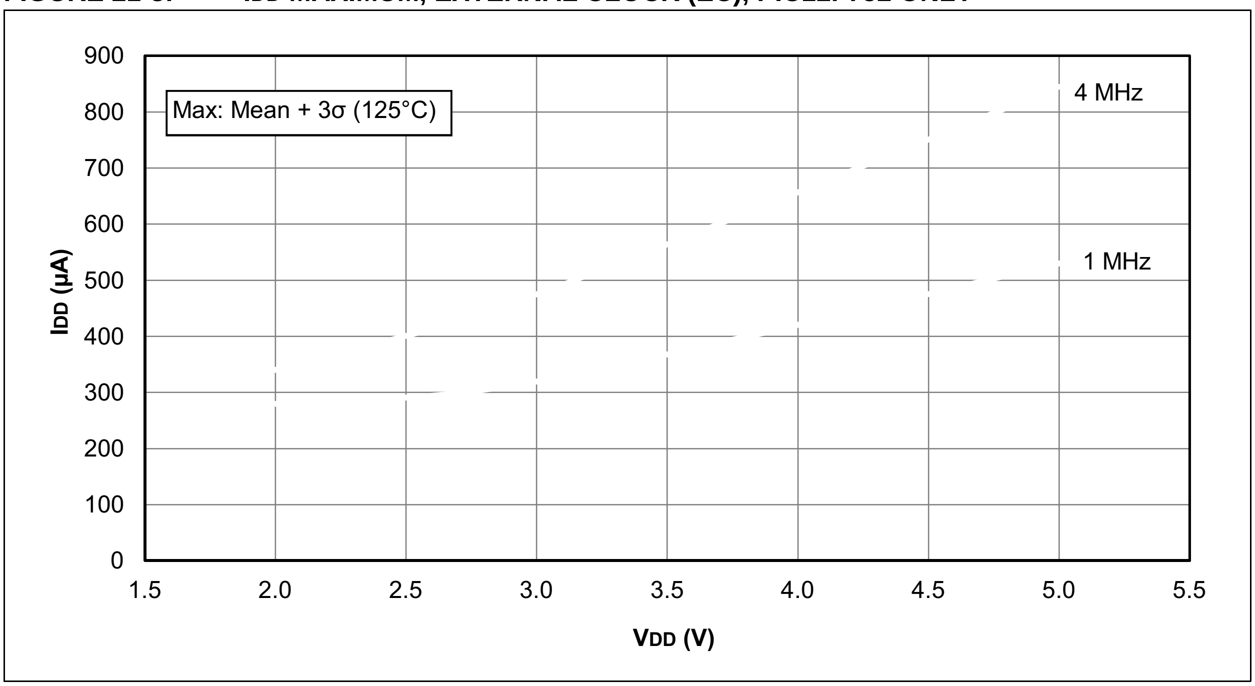


FIGURE 21-11: IDD, EXTERNAL CLOCK (EC), FOSC = 20 MHZ, PIC12F752 ONLY

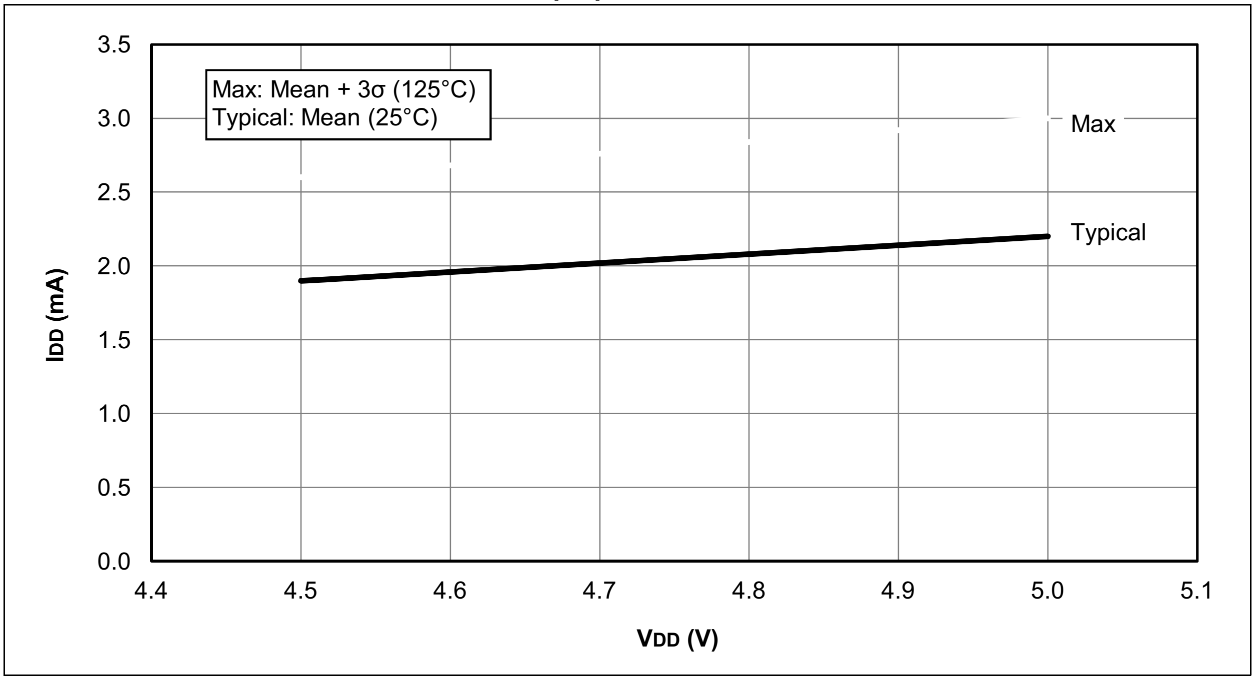


FIGURE 21-14: IPD, WATCHDOG TIMER (WDT), PIC12F752 ONLY

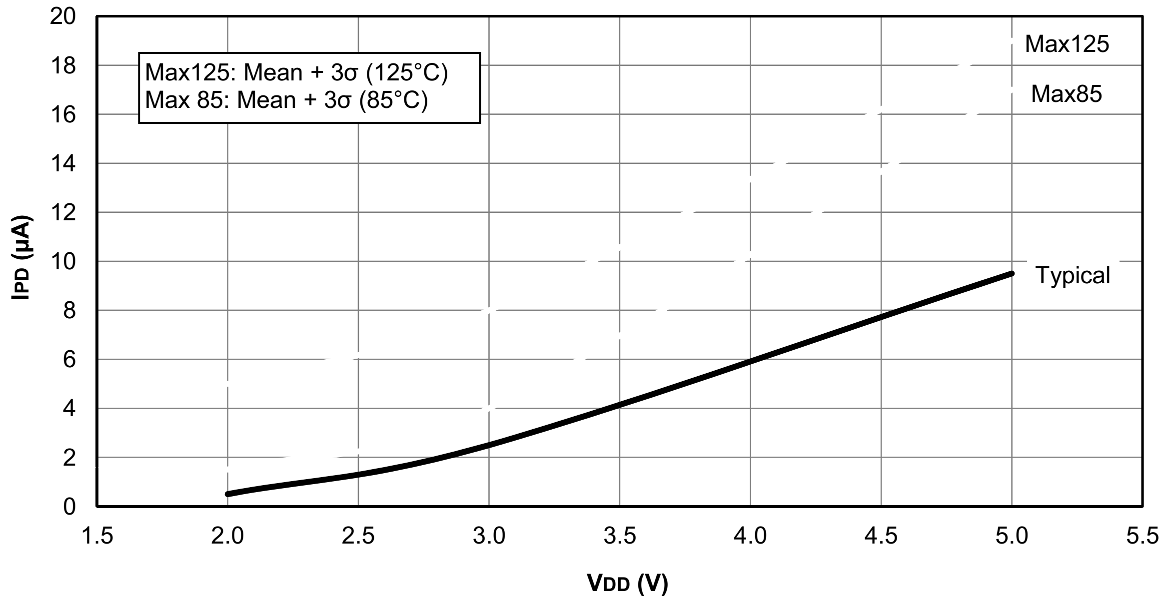


FIGURE 21-15: IPD, WATCHDOG TIMER (WDT), PIC12HV752 ONLY

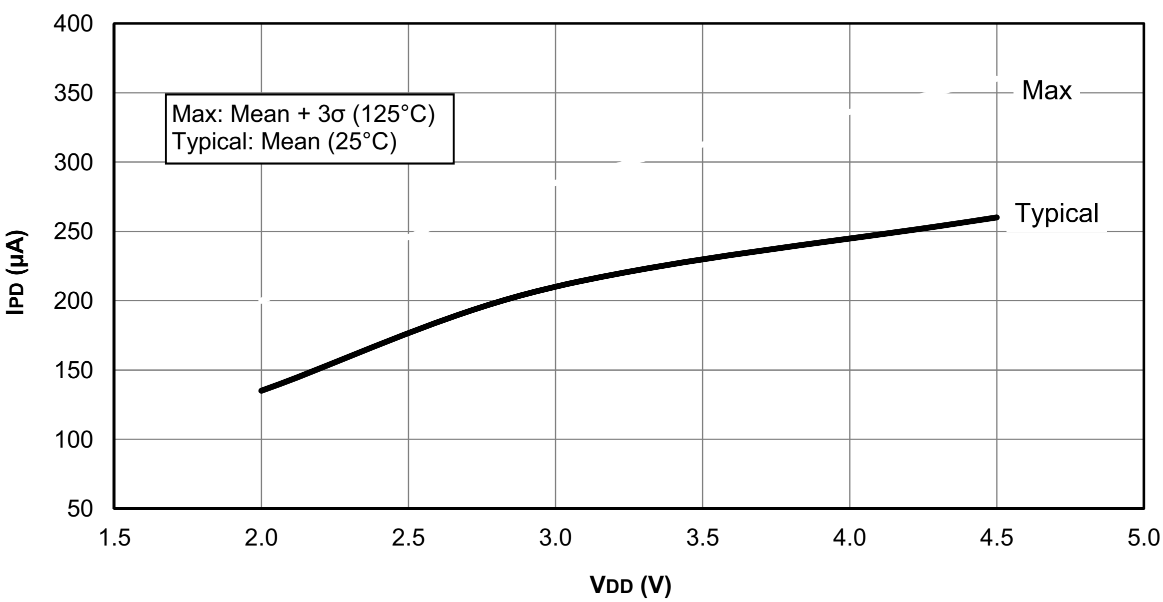


FIGURE 21-16: IPD FIXED VOLTAGE REFERENCE (FVR), PIC12F752 ONLY

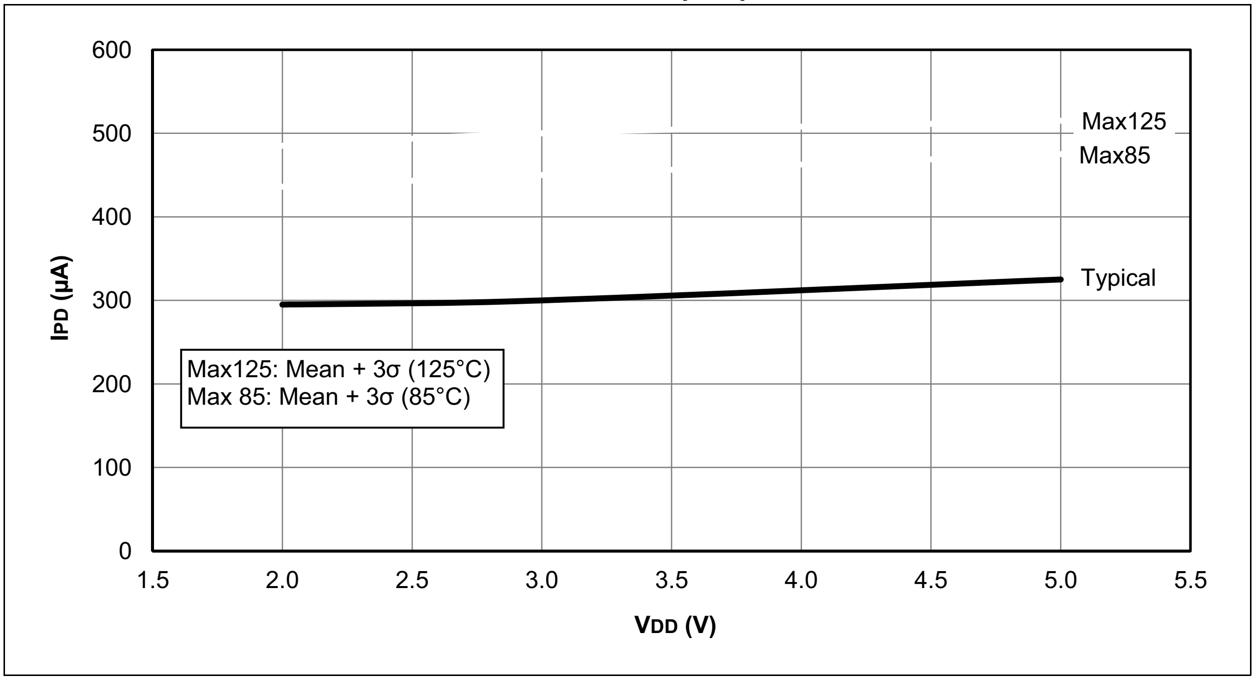


FIGURE 21-17: IPD FIXED VOLTAGE REFERENCE (FVR), PIC12HV752 ONLY

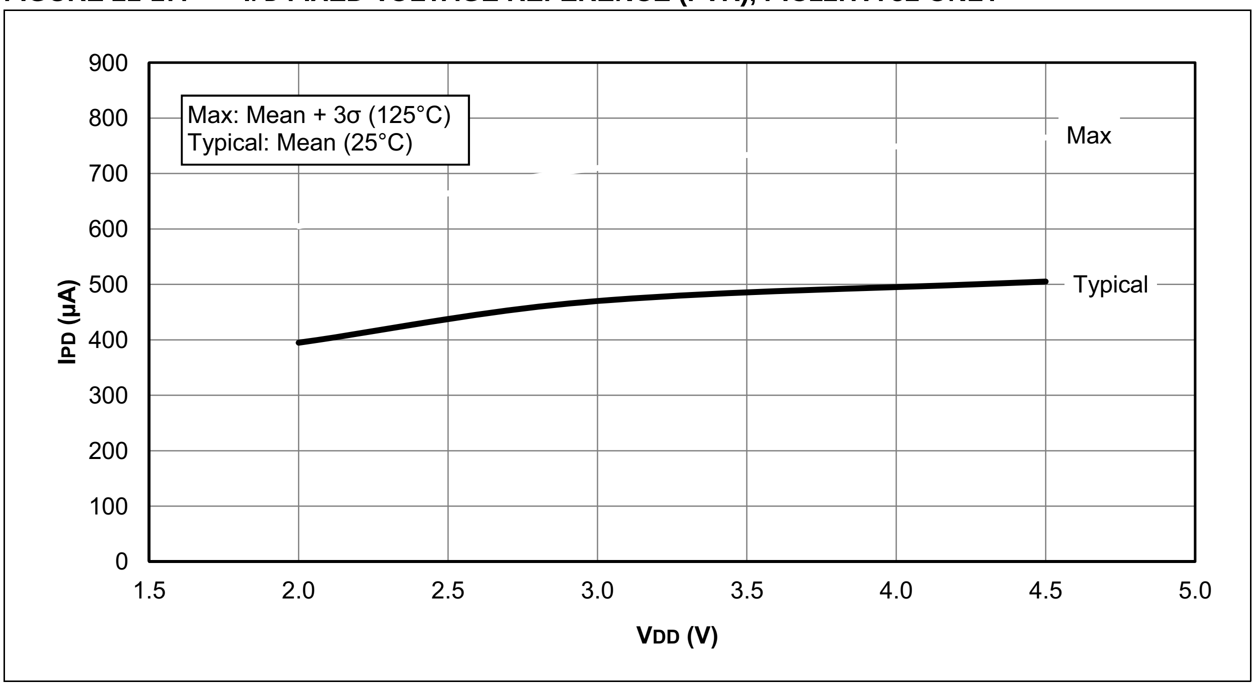


FIGURE 21-20: IPD, TIMER1 OSCILLATOR, FOSC = 32 kHz, PIC12F752 ONLY

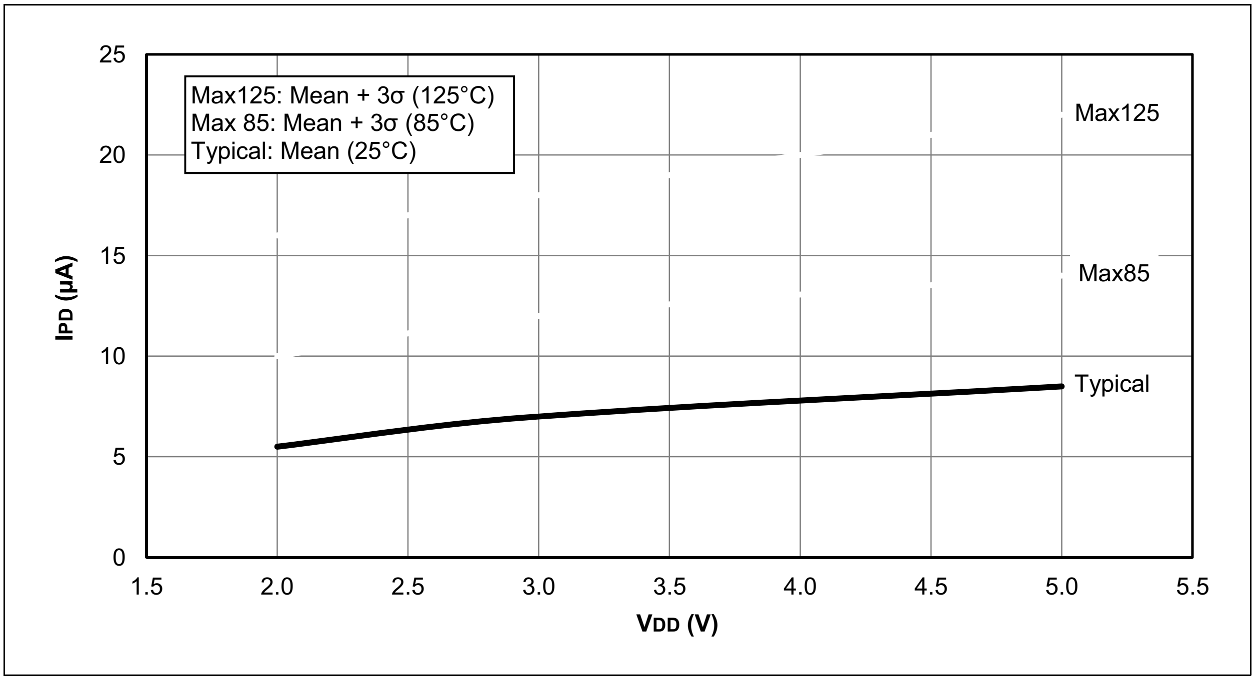
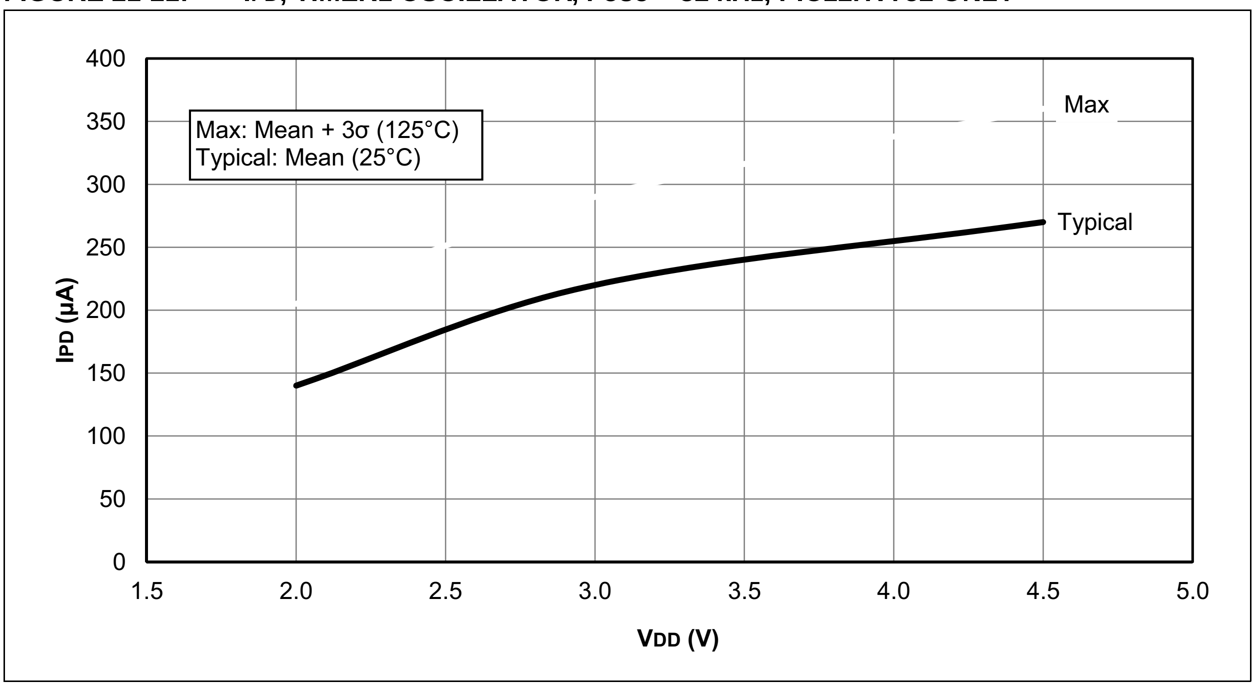


FIGURE 21-21: IPD, TIMER1 OSCILLATOR, FOSC = 32 kHz, PIC12HV752 ONLY



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