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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f752t-i-sn

TABLE 2: 8-PIN ALLOCATION TABLE (PIC12F752/HV752)

I/O	8-Pin PDIP/SOIC/DFN	ADC	Comparators	Timers	CCP	Interrupts	Pull-up	Complementary Output Generator (COG)	Voltage Reference	Basic
RA0(4)	7	AN0	C1IN0+ C2IN0+	—	—	IOC	Y	COG1OUT1	DACOUT REFOUT	ICSPDAT
RA1	6	AN1	C1IN0- C2IN0-	—	—	IOC	Y	—	VREF+	ICSPCLK
RA2(4)	5	AN2	C1OUT C2OUT	T0CKI	CCP1	IOC INT	Y	COG1OUT0	—	—
RA3(1)	4	—	—	T1G(2)	—	IOC	Y(3)	COG1FLT(2)	—	$\overline{\text{MCLR}}$/VPP
RA4	3	AN3	C1IN1-	T1G	—	IOC	Y	COG1FLT COG1OUT1(2)	—	CLKOUT
RA5	2	—	C2IN1-	T1CKI	—	IOC	Y	COG1OUT0(2)	—	CLKIN
—	1	—	—	—	—	—	—	—	—	VDD
—	8	—	—	—	—	—	—	—	—	VSS

Note 1: Input-only.

2: Alternate pin function via the APFCON register.

3: RA3 pull-up is enabled when pin is configured as $\overline{\text{MCLR}}$ in Configuration Word.

4: The port pins for the primary COG1OUTx pins have High-Power (HP) output drivers.

TABLE 2-2: PIC12F752/HV752 SPECIAL REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR Reset	Value on all other Resets(1)
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
01h	TMR0	Holding register for the 8-bit TMR0								xxxx xxxx	uuuu uuuu
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
06h	—	Unimplemented								—	—
07h	—	Unimplemented								—	—
08h	IOCAF	—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	--00 0000	--00 0000
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	---0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	IOCIE	T0IF	INTF	IOCIF(2)	0000 0000	0000 0000
0Ch	PIR1	TMR1GIF	ADIF	—	—	—	HLTMR1IF	TMR2IF	TMR1IF	00---000	00---000
0Dh	PIR2	—	—	C2IF	C1IF	—	COG1IF	—	CCP1IF	--00 -0-0	--00 -0-0
0Eh	—	Unimplemented								—	—
0Fh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	uuuu uuuu
10h	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	uuuu uuuu
11h	T1CON	TMR1CS<1:0>		T1CKPS<1:0>		Reserved	$\overline{T1SYNC}$	—	TMR1ON	0000 00-0	uuuu uu-u
12h	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{DONE}$	T1GVAL	T1GSS<1:0>		0000 0x00	uuuu uxuu
13h	CCPR1L	Capture/Compare/PWM Register1 Low Byte								xxxx xxxx	uuuu uuuu
14h	CCPR1H	Capture/Compare/PWM Register1 High Byte								xxxx xxxx	uuuu uuuu
15h	CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>				--00 0000	--00 0000
16h to 1Bh	—	Unimplemented								—	—
1Ch	ADRESL	Least Significant 2 bits of the left shifted result or 8 bits of the right shifted result								xxxx xxxx	uuuu uuuu
1Dh	ADRESH	Most Significant 8 bits of the left shifted A/D result or 2 bits of right shifted result								xxxx xxxx	uuuu uuuu
1Eh	ADCON0	ADFM	VCFG	CHS<3:0>				GO/$\overline{DONE}$	ADON	0000 0000	0000 0000
1Fh	ADCON1	—	ADCS<2:0>			—	—	—	—	-000 ----	-000 ----

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition shaded = unimplemented

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: MCLR and WDT Reset does not affect the previous value data latch. The IOCIF bit will be cleared upon Reset but will set again if the mismatch exists.

5.5.4 INTERRUPT-ON-CHANGE

All pins on all ports can be configured to operate as Interrupt-on-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual pin or combination of pins can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change Enable (Master Switch)
- Individual Pin Configuration
- Rising and Falling Edge Detection
- Individual Pin Interrupt Flags

Figure 14-1 is a block diagram of the IOC module.

5.5.4.1 Enabling the Module

To allow individual pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

5.5.4.2 Individual Pin Configuration

For each pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCAP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCAN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting the associated bits in both of the IOCAP and IOCAN registers.

5.5.4.3 Interrupt Flags

The bits located in the IOCAF registers are status flags that correspond to the interrupt-on-change pins of each port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCAF bits.

5.5.4.4 Clearing Interrupt Flags

The individual status flags (IOCAF register bits) can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 5-2: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

```
MOVLW  0xff
XORWF  IOCAF, W
ANDWF  IOCAF, F
```

5.5.4.5 Operation in Sleep

The interrupt-on-change interrupt will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the affected IOCAF register will be updated prior to the first instruction executed out of Sleep.

7.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

7.4 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If external clock source is selected, then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 7.4.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

7.4.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read, which is taken care of in hardware. However, the user should keep in mind that reading the 16-bit timer in two 8-bit values poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

7.5 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 gate count enable.

Timer1 gate can also be driven by multiple selectable sources.

7.5.1 TIMER1 GATE COUNT ENABLE

The Timer1 gate is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 gate is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate (T1G) input is active, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 gate input is inactive, no incrementing will occur and Timer1 will hold the current count. See Figure 7-3 for timing details.

TABLE 7-3: TIMER1 GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer1 Operation
↑	0	0	Counts
↑	0	1	Holds Count
↑	1	0	Holds Count
↑	1	1	Counts

FIGURE 7-3: TIMER1 GATE COUNT ENABLE MODE

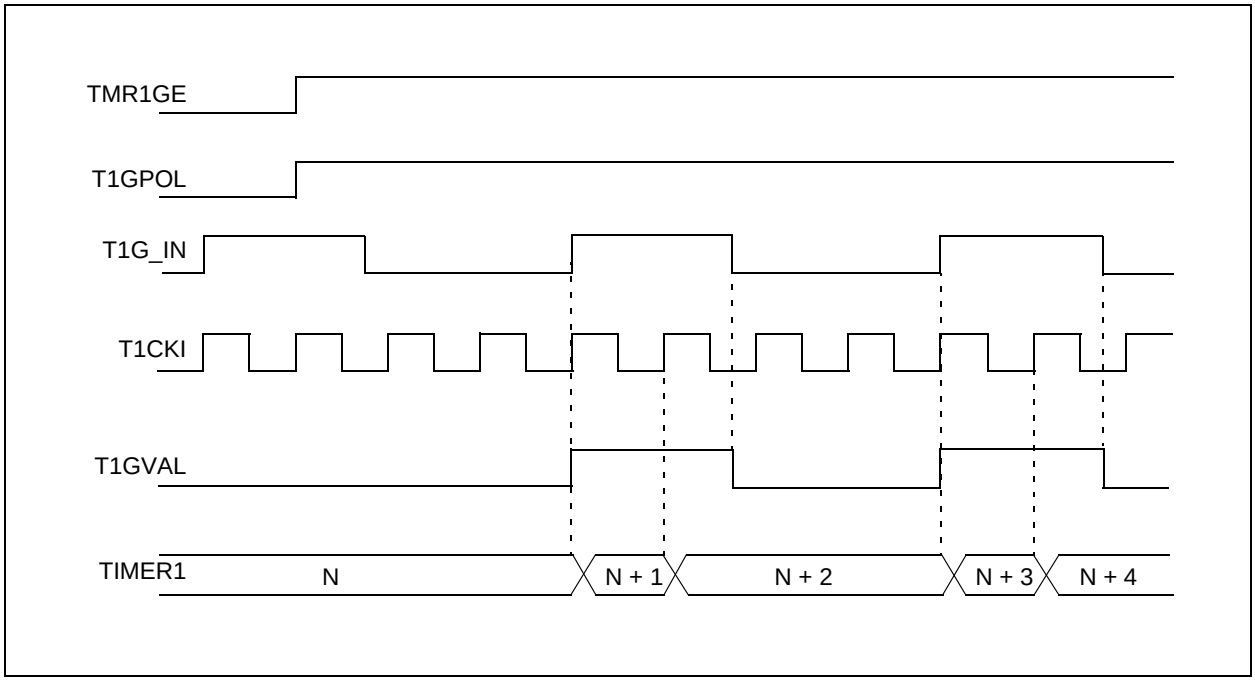
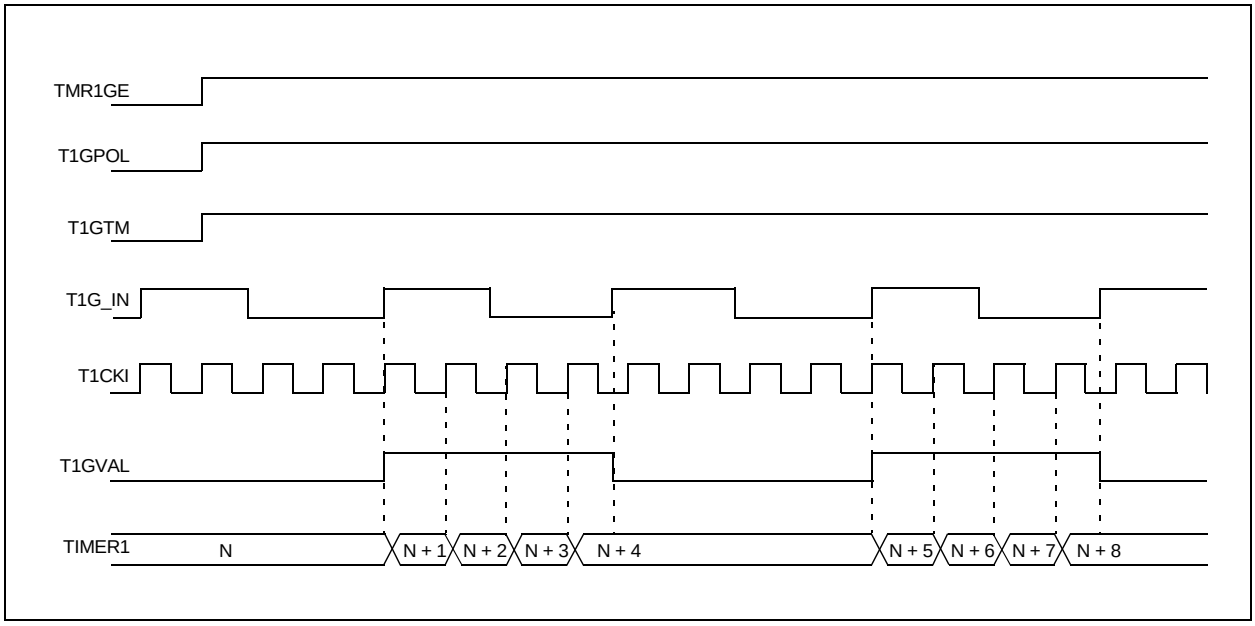


FIGURE 7-4: TIMER1 GATE TOGGLE MODE



10.2 Compare Mode

Compare mode makes use of the 16-bit Timer1 resource. The 16-bit value of the CCPR1H:CCPR1L register pair is constantly compared against the 16-bit value of the TMR1H:TMR1L register pair. When a match occurs, one of the following events can occur:

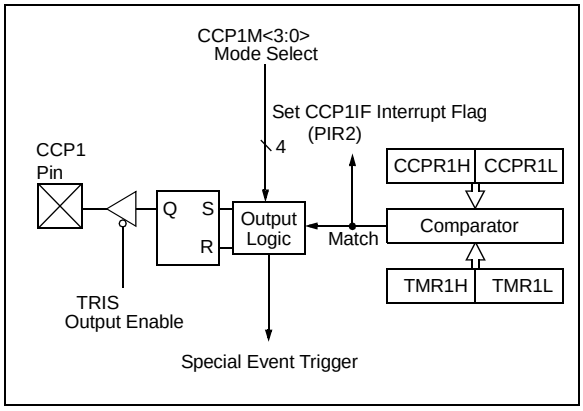
- Toggle the CCP1 Output
- Set the CCP1 Output
- Clear the CCP1 Output
- Generate a Special Event Trigger
- Generate a Software Interrupt

The action on the pin is based on the value of the CCP1M<3:0> control bits of the CCP1CON register. At the same time, the interrupt flag CCP1IF bit is set.

All Compare modes can generate an interrupt.

Figure 10-2 shows a simplified diagram of the Compare operation.

FIGURE 10-2: COMPARE MODE OPERATION BLOCK DIAGRAM



10.2.1 CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the associated TRIS bit.

Note:	Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the PORT I/O data latch.

10.2.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See **Section 7.0 "Timer1 Module with Gate Control"** for more information on configuring Timer1.

Note:	Clocking Timer1 from the system clock (FOSC) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCP1 pin, Timer1 must be clocked from the instruction clock (FOSC/4) or from an external clock source.

10.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCP1M<3:0> = 1010), the CCP1 module does not assert control of the CCP1 pin (see the CCP1CON register).

10.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCP1M<3:0> = 1011), the CCP1 module does the following:

- It resets Timer1
- It starts an ADC conversion if ADC is enabled

The CCP1 module does not assert control of the CCP1 pin in this mode.

The Special Event Trigger output of the CCP1 occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPR1H, CCPR1L register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. The Special Event Trigger output starts an A/D conversion (if the A/D module is enabled). This allows the CCPR1H, CCPR1L register pair to effectively provide a 16-bit programmable period register for Timer1.

TABLE 10-2: SPECIAL EVENT TRIGGER

Device	CCP1
PIC12F752 PIC12HV752	CCP1

Refer to **Section 12.0 "Analog-to-Digital Converter (ADC) Module"** for more information.

Note 1:	The Special Event Trigger from the CCP module does not set interrupt flag bit TMR1IF of the PIR1 register.
2:	Removing the match condition by changing the contents of the CCPR1H and CCPR1L register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

11.7 Phase Delay

It is possible to delay the assertion of the rising event. This is accomplished by placing a non-zero value in COGxPH register. Refer to Register 11-6 and Figure 11-3 for COG operation with CCP1 and phase delay. The delay from the input rising event signal switching to the actual assertion of the events is calculated the same as the dead-band and blanking delays. Please see Equation 11-1.

When the COGxPH value is '0', phase delay is disabled and the phase delay counter output is true, thereby, allowing the event signal to pass straight through to complementary output driver flop.

11.7.1 CUMULATIVE UNCERTAINTY

It is not possible to create more than one COG_clock of uncertainty by successive stages. Consider that the phase delay stage comes after the blanking stage, the dead-band stage comes after either the blanking or phase delay stages, and the blanking stage comes after the dead-band stage. When the preceding stage is enabled, the output of that stage is necessarily synchronous with the COG_clock, which removes any possibility of uncertainty in the succeeding stage.

EQUATION 11-1: PHASE, DEAD-BAND, AND BLANKING TIME CALCULATION

$$T_{\text{min}} = \frac{\text{Count}}{F_{COG\_clock}}$$

$$T_{\text{max}} = \frac{\text{Count} + 1}{F_{COG\_\text{clock}}}$$

$$T_{\text{uncertainty}} = T_{\text{max}} - T_{\text{min}}$$

Also:

$$T_{\text{uncertainty}} = \frac{1}{F_{COG\_\text{clock}}}$$

Where:

T	Count
Phase Delay	GxPH<3:0>
Rising Dead Band	GxDBR<3:0>
Falling Dead Band	GxDBF<3:0>
Rising Event Blanking	GxBLKR<3:0>
Falling Event Blanking	GxBLKF<3:0>

EXAMPLE 11-1: TIMER UNCERTAINTY

Given:

$$Count = Ah = 10d$$
$$F_{COG\_\text{Clock}} = 8\text{MHz}$$

Therefore:

$$T_{\text{uncertainty}} = \frac{1}{F_{COG\_\text{clock}}} = \frac{1}{8MHz} = 125ns$$

Proof:

$$T_{\text{min}} = \frac{Count}{F_{COG\_\text{clock}}} = 125ns \bullet 10d = 1.25\mu s$$

$$T_{\text{max}} = \frac{Count + 1}{F_{COG\_\text{clock}}} = 125ns \bullet (10d + 1) = 1.375\mu s$$

Therefore:

$$T_{\text{uncertainty}} = T_{\text{max}} - T_{\text{min}} = 1.375\mu s - 1.25\mu s = 125ns$$

11.9 Buffer Updates

Changes to the phase, dead band, and blanking count registers need to occur simultaneously during COG operation to avoid unintended operation that may occur as a result of delays between each register write. This is accomplished with the GxLD bit of the COGxCON0 register and double buffering of the phase, blanking, and dead-band count registers.

Before the COG module is enabled, writing the count registers loads the count buffers without need of the GxLD bit. However, when the COG is enabled, the count buffers updates are suspended after writing the count registers until after the GxLD bit is set. When the GxLD bit is set, the phase, dead band and blanking register values are transferred to the corresponding buffers synchronous with COG operation. The GxLD bit is cleared by hardware to indicate that the transfer is complete.

11.10 Alternate Pin Selection

The COGxOUT0, COGxOUT1 and COGxFLT functions can be directed to alternate pins with control bits of the APFCON register. Refer to Register 5-1.

Note:	The default COG outputs have high drive strength capability, whereas the alternate outputs do not.

11.11 Operation During Sleep

The COG continues to operate in Sleep provided that the COG_clock, rising event and falling event sources remain active.

The HFINTSOC remains active during Sleep when the COG is enabled and the HFINTOSC is selected as the COG_clock source.

11.12 Configuring the COG

The following steps illustrate how to properly configure the COG to ensure a synchronous start with the rising event input:

1. Configure the desired COGxFLT input, COGxOUT0 and COGxOUT1 pins with the corresponding bits in the APFCON register.
2. Clear all ANSELA register bits associated with pins that are used for COG functions.
3. Ensure that the TRIS control bits corresponding to COGxOUT0 and COGxOUT1 are set so that both are configured as inputs. These will be set as outputs later.
4. Clear the GxEN bit, if not already cleared.
5. Set desired dead-band times with the COGxDB register.
6. Set desired blanking times with the COGxBLK register.
7. Set desired phase delay with the COGxPH register.
8. Setup the following controls in COGxASD auto-shutdown register:
   - Select desired shutdown sources.
   - Select both output overrides to the desired levels (this is necessary, even if not using auto-shutdown because start-up will be from a shutdown state).
   - Set the GxASDE bit and clear the GxARSEN bit.
9. Select the desired rising and falling event sources and input modes with the COGxCON1 register.
10. Configure the following controls in COGxCON0 register:
    - Select the desired clock source
    - Select the desired output polarities
    - Set the output enables of the outputs to be used.
11. Set the GxEN bit.
12. Clear TRIS control bits corresponding to COGxOUT0 and COGxOUT1 to be used thereby configuring those pins as outputs.
13. If auto-restart is to be used, set the GxARSEN bit and the GxASDE will be cleared automatically. Otherwise, clear the GxASDE bit to start the COG.

13.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference (FVR) is a stable voltage reference, independent of VDD, with 1.2V output level. The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel
- Comparator 1 positive input (C1VP)
- Comparator 2 positive input (C2VP)
- REFOUT pin

On the PIC12F752, the FVR is enabled by setting the FVREN bit of the FVRCON register. The FVR is always enabled on the PIC12HV752 device.

13.1 Fixed Voltage Reference Output

The FVR output can be applied to the REFOUT pin by setting the FVRBUFSS and FVRBUFEN bits of the FVRCON register. The FVRBUFSS bit selects either the FVR or DAC output reference to the REFOUT pin buffer. The FVRBUFEN bit enables the output buffer to the REFOUT pin.

Enabling the REFOUT pin automatically overrides any digital input or output functions of the pin. Reading the REFOUT pin when it has been configured for a reference voltage output will always return a '0'.

13.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference circuit to stabilize. Once the circuit stabilizes and is ready for use, the FVRRDY bit of the FVRCON register will be set. See **Section 20.0 "Electrical Specifications"** for the minimum delay requirement.

13.3 Operation During Sleep

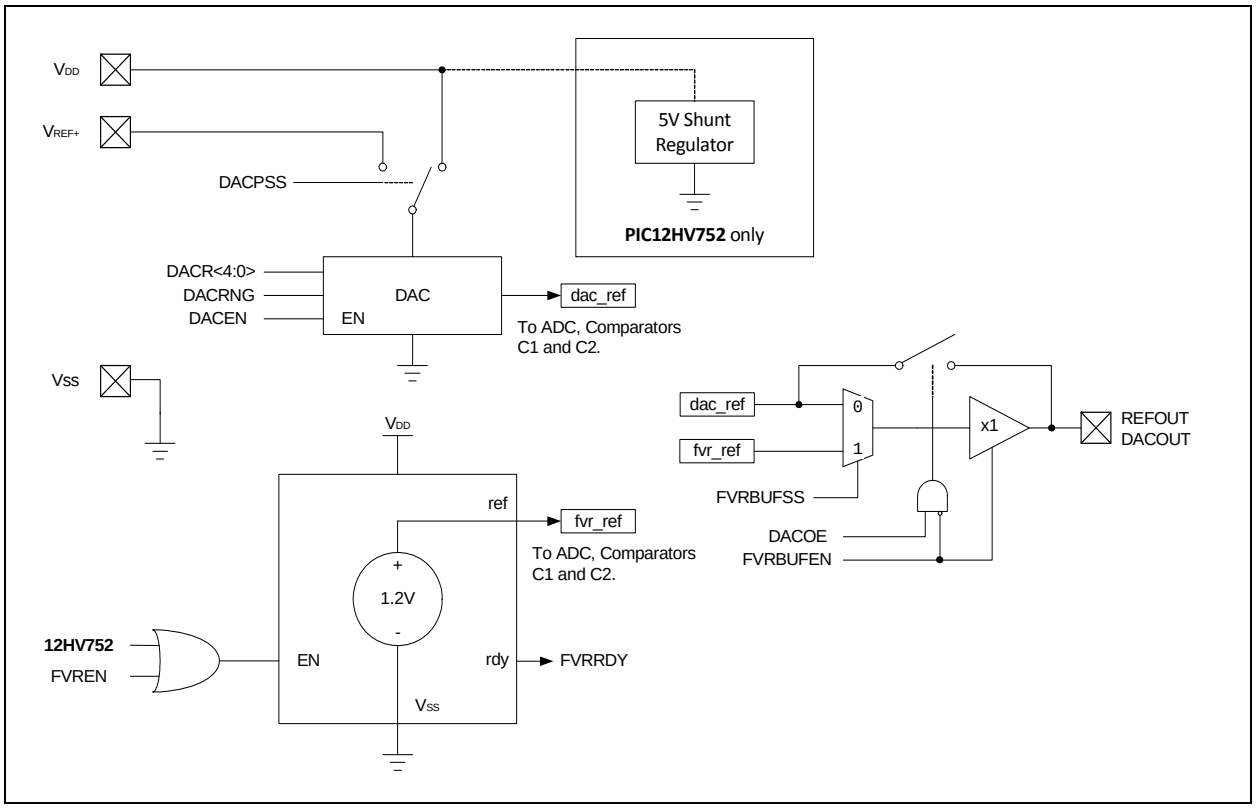
When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the FVRCON register are not affected. To minimize current consumption in Sleep mode, FVR the voltage reference should be disabled.

13.4 Effects of a Reset

A device Reset clears the FVRCON register. As a result:

- The FVR module is disabled
- The FVR voltage output is disabled on the REFOUT pin

FIGURE 13-1: VOLTAGE REFERENCE BLOCK DIAGRAM



14.8 DAC Control Registers

REGISTER 14-1: DACCON0: VOLTAGE REFERENCE CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	U-0	U-0
DACEN	DACRNG	DACOE	—	—	DACPSS	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **DACEN:** DAC Enable bit
1 = DAC is enabled
0 = DAC is disabled

bit 6 **DACRNG:** DAC Range Selection bit(1)
1 = DAC is operating in Full Range mode
0 = DAC is operating in Limited Range mode

bit 5 **DACOE:** DAC Voltage Output Enable bit
1 = DAC reference output is enabled to the DACOUT pin(2)
0 = DAC reference output is disabled

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **DACPSS:** DAC Positive Source Select bits
0 = V_{DD}
1 = V_{REF}+ pin

bit 1-0 **Unimplemented:** Read as '0'

Note 1: Refer to Equation 14-1.
2: The DACOUT pin configuration requires additional control bits in the FVRCON register (see Figure 14-3).

REGISTER 14-2: DACCON1: VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	DACR<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **DACR<4:0>:** DAC Voltage Output Select bits
1 1111 = DAC Voltage Maximum Output
•
•
•
0 0000 = DAC Voltage Minimum Output

Note 1: Refer to Equation 14-1 to calculate the value of the DAC Voltage Output.

17.2 Calibration Bits

The 8 MHz internal oscillator is factory calibrated. These calibration values are stored in fuses located in the Calibration Word (2008h). The Calibration Word is not erased when using the specified bulk erase sequence in the *"PIC12F752/HV752 Flash Memory Programming Specification"* (DS41561) and thus, does not require reprogramming.

17.3 Reset

The PIC12F752/HV752 device differentiates between various kinds of Reset:

a) Power-on Reset (POR)
b) WDT Reset during normal operation
c) WDT Reset during Sleep
d) $\overline{\text{MCLR}}$ Reset during normal operation
e) $\overline{\text{MCLR}}$ Reset during Sleep
f) Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

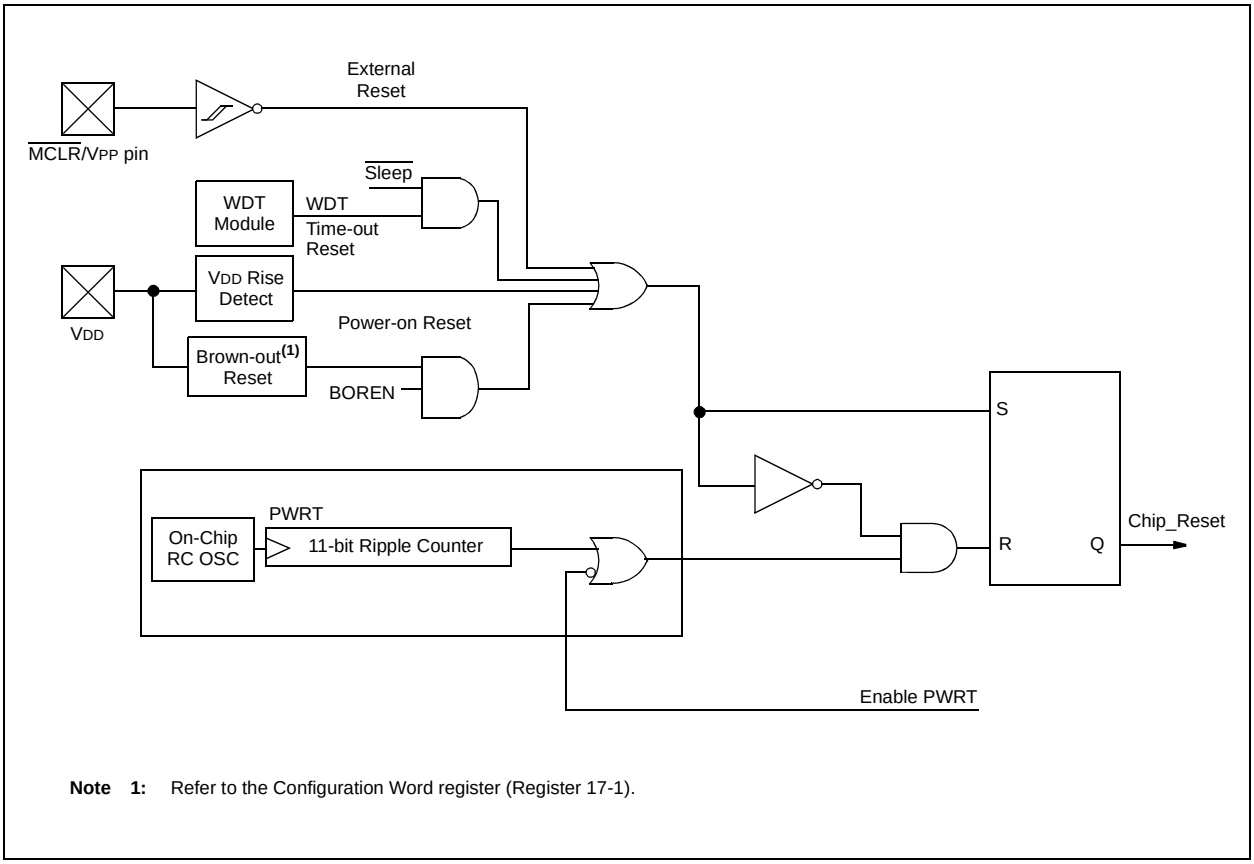
- Power-on Reset
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

WDT wake-up does not cause register resets in the same manner as a WDT Reset since wake-up is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 17-2. Software can use these bits to determine the nature of the Reset. See Table 17-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 17-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 20.0 "Electrical Specifications"** for pulse-width specifications.

FIGURE 17-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: Refer to the Configuration Word register (Register 17-1).

TABLE 20-4: I/O PORTS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
		Capacitive Loading Specs on Output Pins					
D101*	COSC2	OSC2 pin	—	—	15	pF	
D101A*	CIO	All I/O pins	—	—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: This specification applies to all weak pull-up pins, including the weak pull-up found on RA3/$\overline{MCLR}$. When RA3/$\overline{MCLR}$ is configured as $\overline{MCLR}$ Reset pin, the weak pull-up is always enabled.

TABLE 20-5: MEMORY PROGRAMMING SPECIFICATIONS

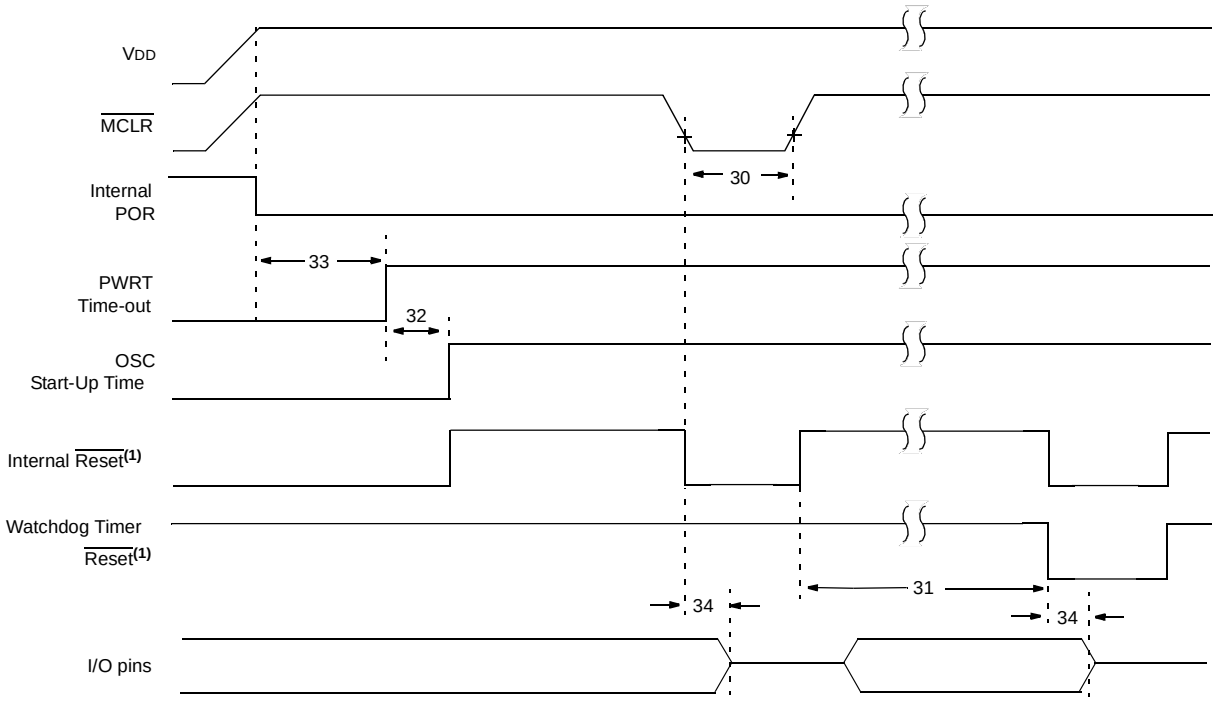
Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
		Program Memory Programming Specifications					
D110	V_{IHH}	Voltage on $\overline{MCLR}$/V_{PP} pin	10.0	—	13.0	V	**(Note 1)**
D112	V_{BE}	V_{DD} for Bulk Erase	4.5	—	V_{DDMAX}	V	
D113	V_{PEW}	V_{DD} for Write or Row Erase	4.5	—	V_{DDMAX}	V	
D114	I_{PPPGM}	Current on $\overline{MCLR}$/V_{PP} during Erase/Write	—	300	1000	μA	
		Program Flash Memory					
D121	E_P	Cell Endurance	10K	100K	—	E/W	-40°C ≤ T_A ≤ +85°C **(Note 2)**
D121A	E_P	Cell Endurance	1K	10K	—	E/W	-40°C ≤ T_A ≤ +125°C **(Note 2)**
D122	V_{PRW}	V_{DD} for Read/Write	V_{DDMIN}	—	V_{DDMAX}	V	
D123	T_{IW}	Self-timed Write Cycle Time	—	2	2.5	ms	
D124	T_{RETD}	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

† Data in "Typ." column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Required only if single-supply programming is disabled.

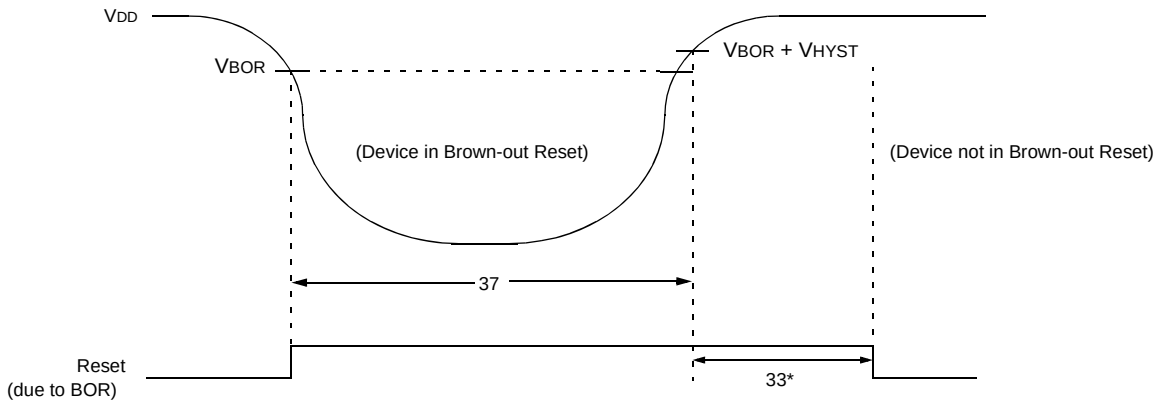
2: Self-write and Block Erase.

FIGURE 20-6: RESET, WATCHDOG TIMER AND POWER-UP TIMER TIMING



Note: Asserted low.

FIGURE 20-7: BROWN-OUT RESET TIMING AND CHARACTERISTICS



* 64 ms delay only if $\overline{\text{PWRTE}}$ bit in the Configuration Word register is programmed to '0'.

FIGURE 20-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

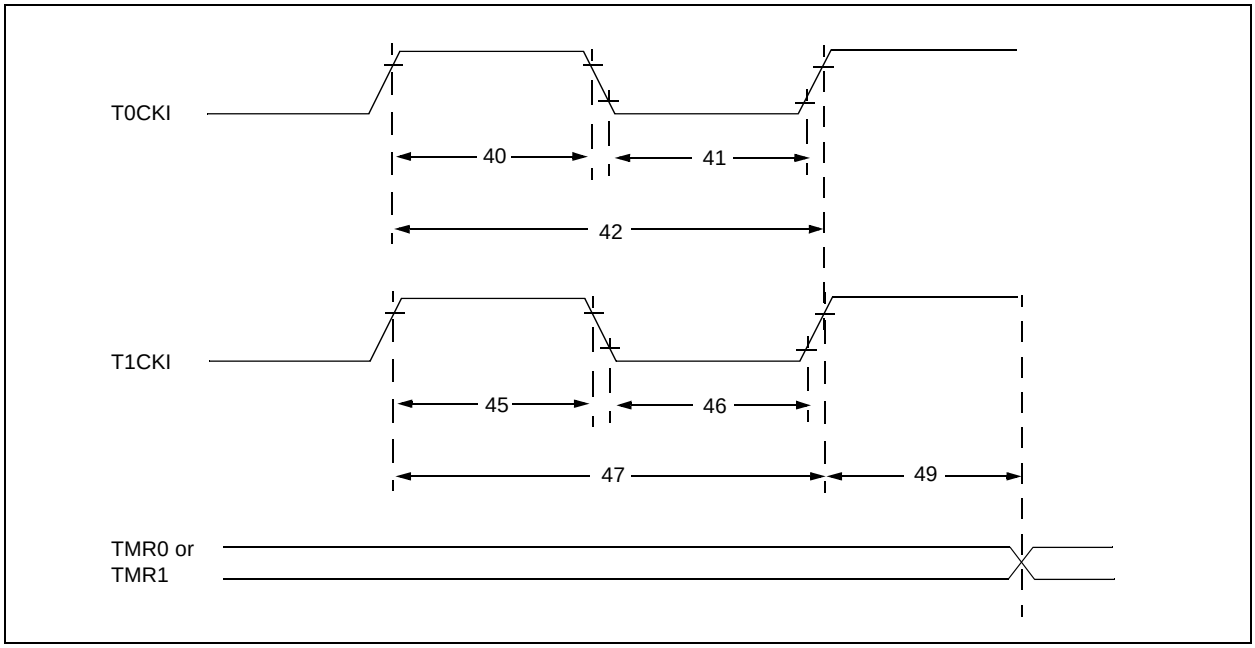


TABLE 20-11: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Param. No.	**Sym.**	**Characteristic**		**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
40*	TT0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period		Greater of: 20 or TCY + 40 / N	—	—	ns	N = prescale value
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous	Greater of: 30 or TCY + 40 / N	—	—	ns	N = prescale value
			Asynchronous	60	—	—	ns	
49*	TCKEZT-MR1	Delay from External Clock Edge to Timer Increment		2 TOSC	—	7 TOSC	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in “Typ.” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 21-22: IPD, DAC, PIC12F752 ONLY

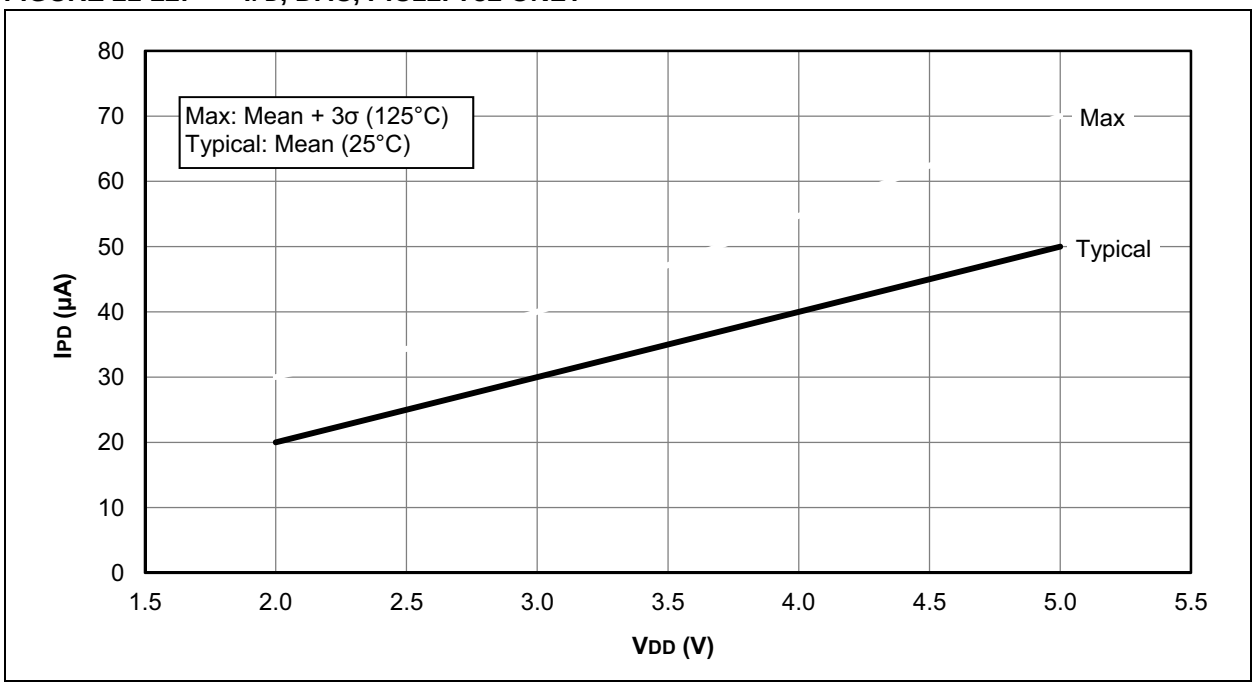


FIGURE 21-23: IPD, DAC, PIC12HV752 ONLY

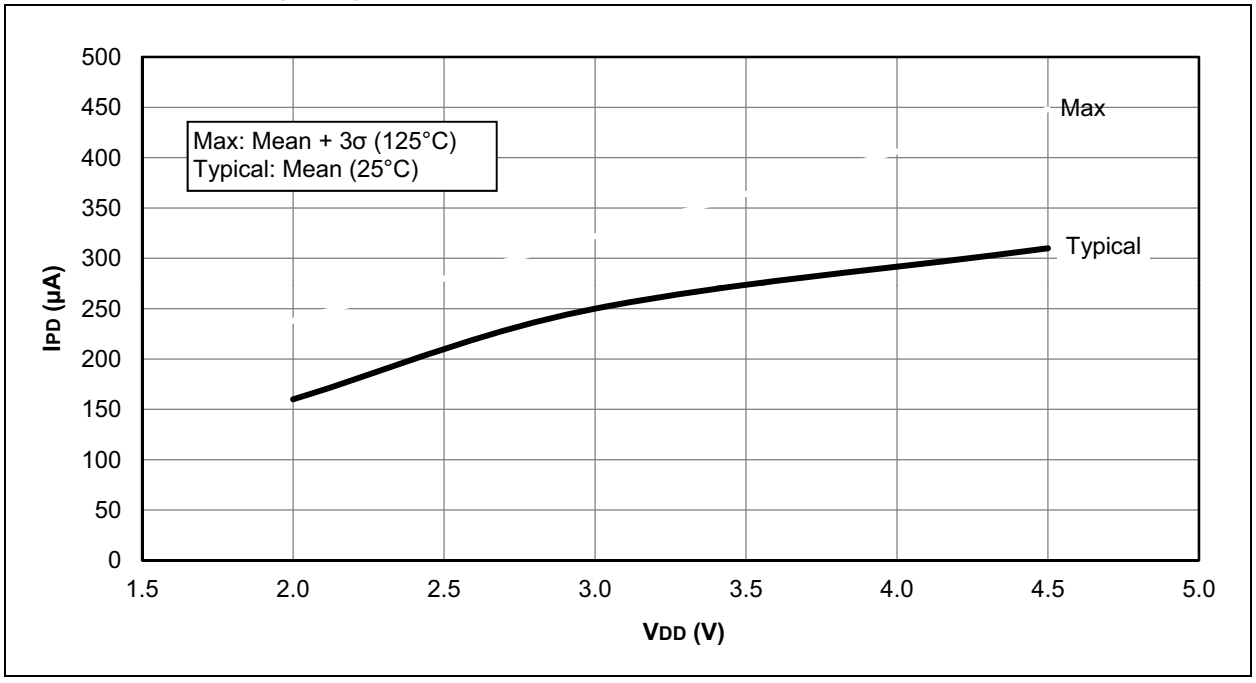


FIGURE 21-24: IPD, COMPARATOR, LOW-POWER MODE, CxSP = 0, PIC12F752 ONLY

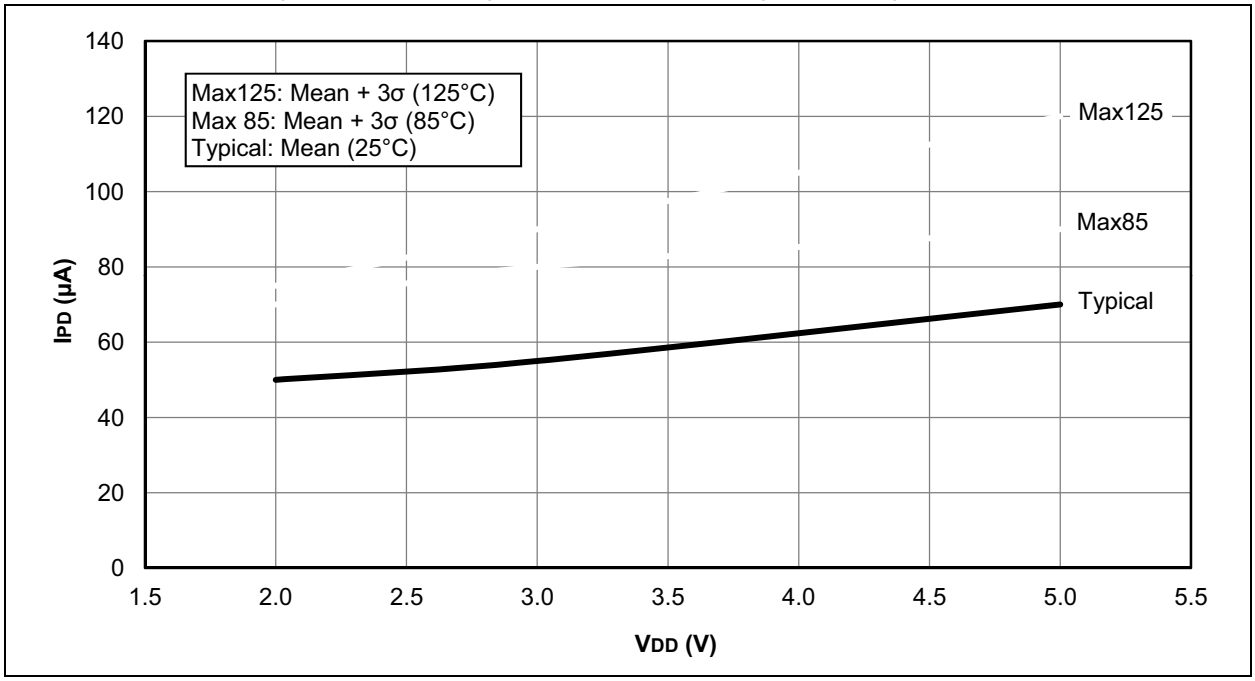
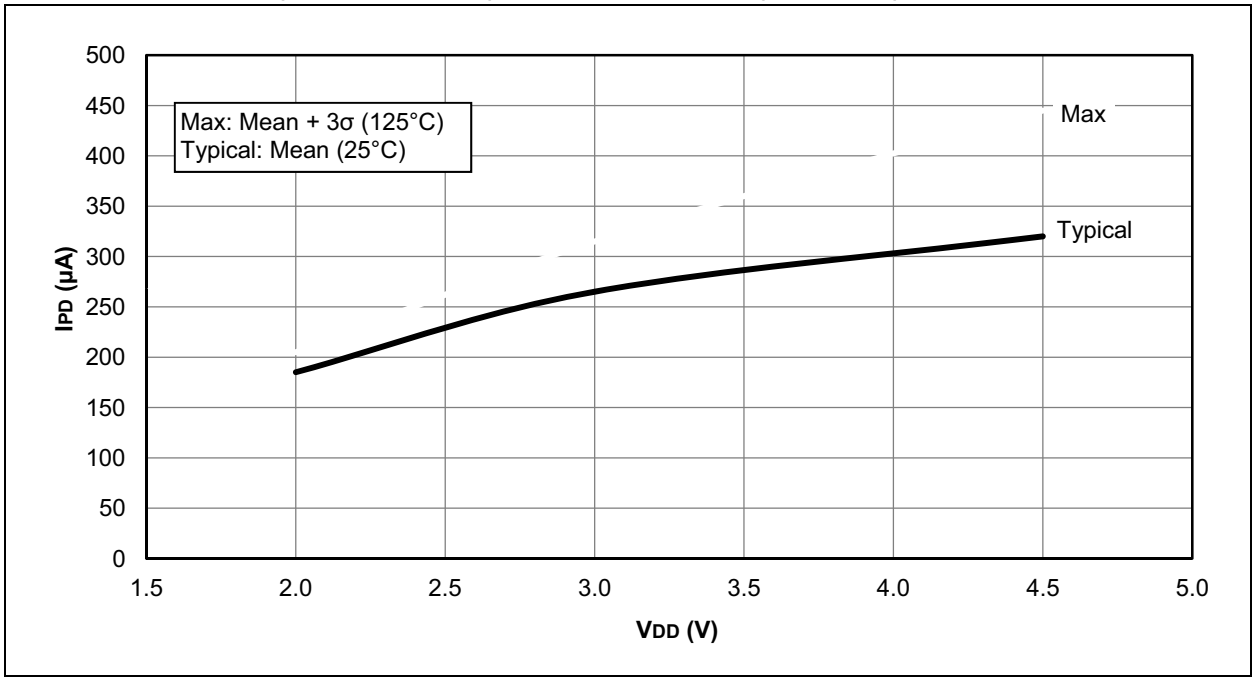
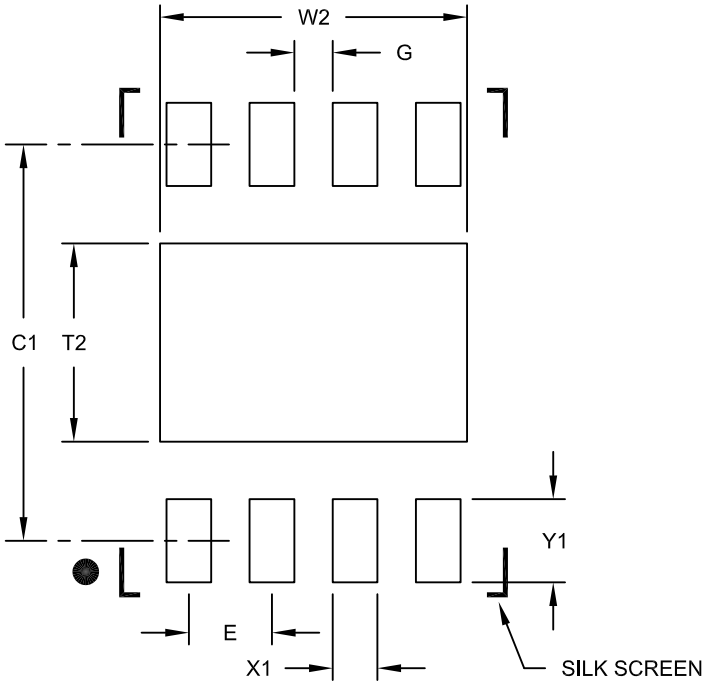


FIGURE 21-25: IPD, COMPARATOR, LOW-POWER MODE, CxSP = 0, PIC12HV752 ONLY



8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	PIC12F752 PIC12HV752	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package:	P SN MF	= Plastic DIP (PDIP) = 8-lead Small Outline (3.90 mm) (SOIC) = 8-lead Plastic Dual Flat, No Lead (3x3) (DFN)
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC12F752T - I/MF 301
Tape and Reel,
Industrial temperature,
DFN 3x3 package,
QTP pattern #301

b) PIC12F752 - E/P
Extended temperature
PDIP package

c) PIC12F752 - E/SN
Extended temperature,
SOIC package

d) PIC12HV752 - E/MF
Extended temperature,
DFN 3x3 package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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