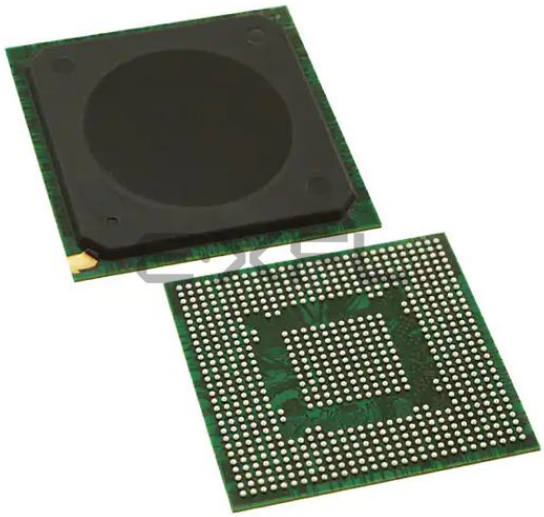


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Security; SEC 3.0
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (4)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 125°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8379ecvralg

1.10 Serial ATA (SATA) Controllers

The serial ATA (SATA) controllers have the following features:

- Supports *Serial ATA Rev 2.5 Specification*
- Spread spectrum clocking on receive
- Asynchronous notification
- Hot Plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- Port multiplier support
- SATA 1.5 and 3.0 Gb/s operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - — Far end/near end loopback
  - — Failed CRC error reporting
  - — Increased ALIGN insertion rates
- Scrambling and CONT override

1.11 Enhanced Secured Digital Host Controller (eSDHC)

The enhanced SD host controller (eSDHC) has the following features:

- Conforms to *SD Host Controller Standard Specification, Rev 2.0* with Test Event register support.
- Compatible with the *MMC System Specification, Rev 4.0*
- Compatible with the *SD Memory Card Specification, Rev 2.0,* and supports High Capacity SD memory cards
- Compatible with the *SDIO Card Specification Rev, 1.2*
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, MMC 4x, and RS-MMC cards
- SD bus clock frequency up to 50 MHz
- Supports 1-/4-bit SD and SDIO modes, 1-/4-bit MMC modes
- Supports internal DMA capabilities

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the chip. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

Table 5. Power Dissipation [1] (continued)

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
450	300	1.45	2.0	3.2	3.8
	225	1.45	1.9	3.1	3.7
500	333	1.45	2.0	3.3	3.9
	250	1.45	1.9	3.2	3.8
533	355	1.45	2.0	3.3	4.0
	266	1.45	2.0	3.2	3.9
600	400	1.45	2.1	3.4	4.1
	300	1.45	2.0	3.3	4.0
667	333	1.45	2.1	3.3	4.1
	266	1.45	2.0	3.3	3.9
800	400	1.45	2.5	3.8	4.3

Notes:

1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
3. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
4. Maximum power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, worst case process, and running an artificial smoke test.

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8. CLKIN AC Timing Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
CLKIN/PCI_CLK frequency	f_{CLKIN}	25	—	66.666	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	40	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	± 150	ps	4, 5

Notes:
1. **Caution:** The system, core and security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter-short term and long term-and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread on CLKIN/PCI_CLK up to 60 KHz.

4.3 eTSEC Gigabit Reference Clock Timing

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 9. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 47	—	 53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:
1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.2, "RGMII and RTBI AC Timing Specifications," for the duty cycle for 10Base-T and 100Base-T reference clock.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Parameter	Symbol	Min	Max	Unit	Note
Output low current (V_{OUT} = 0.3 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

Table 14 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.18	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.18	V	—
Output leakage current	I_{OZ}	–50	50	µA	4
Output high current (V_{OUT} = 1.9 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.38 V)	I_{OL}	15.2	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

Table 26. MII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

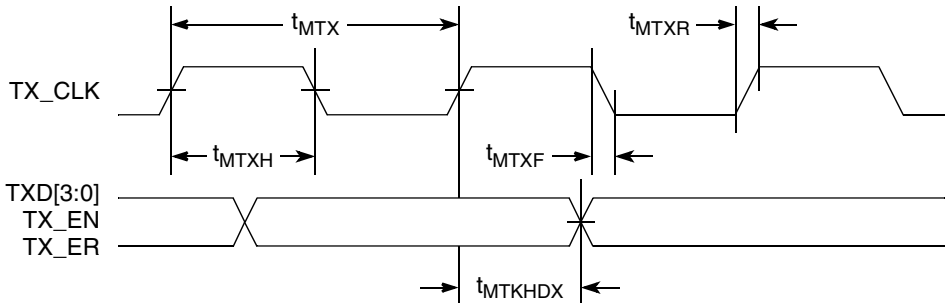


Figure 7. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 27. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
Input low voltage	V_{IL}	—	—	0.7	V
Input high voltage	V_{IH}	1.9	—	—	V
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

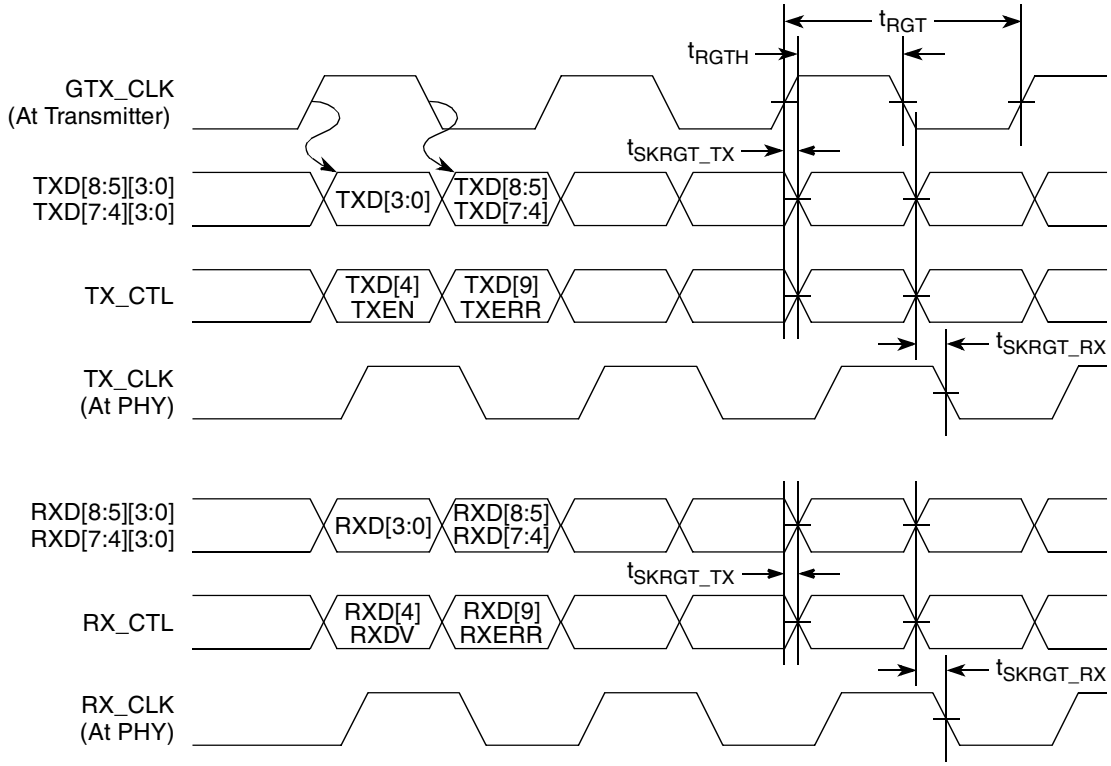


Figure 11. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

This table shows the RMII transmit AC timing specifications.

Table 29. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns

This figures show the local bus signals.

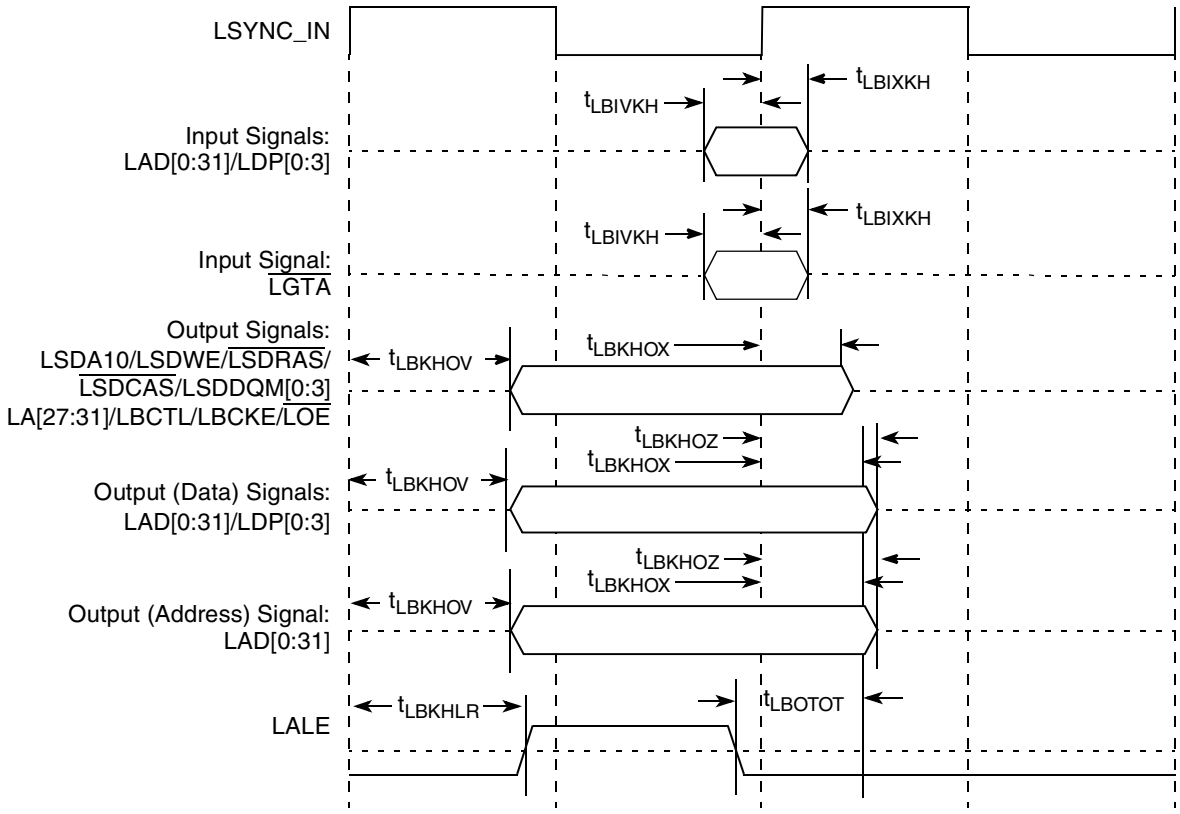


Figure 20. Local Bus Signals, Non-special Signals Only (PLL Enable Mode)

Table 42. eSDHC AC Timing Specifications for Full-Speed Mode (continued)

At recommended operating conditions OV_{DD} = 3.3 V ± 165 mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
Input hold times: SD_CMD, SD_DAT*x*, SD_CD to SD_CLK	$t_{SFSIXKH}$	0	—	ns	2
SD_CLK delay within device	$t_{INT\_CLK\_DLY}$	1.5	—	ns	4
Output valid: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOV}$	—	4	ns	2
Output hold: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOX}$	0	—	—	—
SD card input setup	t_{ISU}	5	—	ns	3
SD card input hold	t_{IH}	5	—	ns	3
SD card output valid	t_{ODLY}	—	14	ns	3
SD card output hold	t_{OH}	0	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

This figure provides the eSDHC clock input timing diagram.

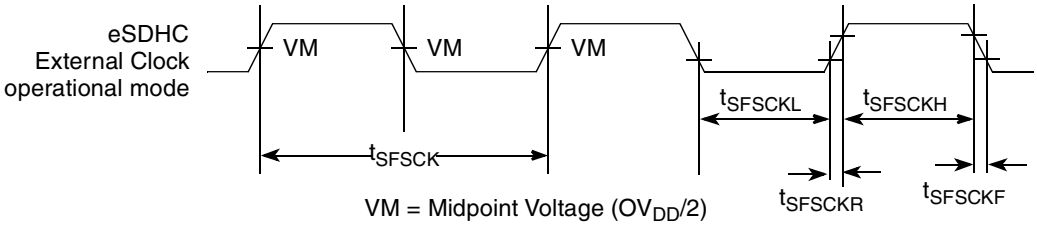


Figure 26. eSDHC Clock Input Timing Diagram

$$t_{CLK\_DELAY} + t_{IH} - t_{SFSKHOX} < t_{SFSCKL} + t_{DATA\_DELAY} \quad \text{Eqn. 5}$$

This means that clock can be delayed versus data up to 15 ns (external delay line) in ideal case of $t_{SFSCLKL}$ = 20 ns:

$t_{CLK\_DELAY} + 5 - 0 < 20 + t_{DATA\_DELAY}$

$t_{CLK\_DELAY} < 15 + t_{DATA\_DELAY}$

11.2.1.3 Full-Speed Write Combined Formula

The following equation is the combined formula to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} + t_{IH} - t_{SFSKHOX} < t_{SFSCKL} + t_{DATA\_DELAY} < t_{SFSCK} + t_{CLK\_DELAY} - t_{ISU} - t_{SFSKHOV} \quad \text{Eqn. 6}$$

11.2.2 Full-Speed Input Path (Read)

This figure provides the data and command input timing diagram.

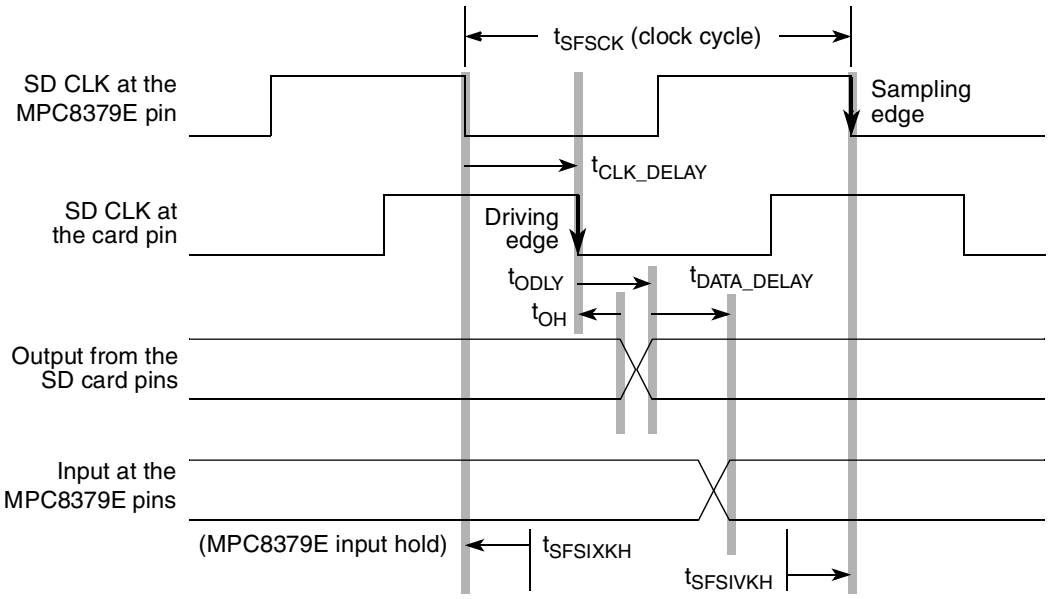


Figure 28. Full Speed Input Path

11.2.2.1 Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{ODLY} + t_{SFSIVKH} < t_{SFSCK} \quad \text{Eqn. 7}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < t_{SFSCK} - t_{ODLY} - t_{SFSIVKH} - t_{INT\_CLK\_DLY} \quad \text{Eqn. 8}$$

11.2.2.2 Full-Speed Read Meeting Hold (Minimum Delay)

There is no minimum delay constraint due to the full clock cycle between the driving and sampling of data.

$$t_{CLK\_DELAY} + t_{OH} + t_{DATA\_DELAY} > t_{SFSIXKH} \quad \textit{Eqn. 9}$$

This means that Data + Clock delay must be greater than –2 ns. This is always fulfilled.

11.3 eSDHC AC Timing Specifications (High-Speed Mode)

This table provides the eSDHC AC timing specifications for high-speed mode as defined in Figure 30 and Figure 31.

Table 43. eSDHC AC Timing Specifications for High-Speed Mode

At recommended operating conditions OV_{DD} = 3.3 V ± 165 mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
SD_CLK clock frequency—high speed mode	f_{SHSCK}	0	50	MHz	—
SD_CLK clock cycle	t_{SHSCK}	20	—	ns	—
SD_CLK clock frequency—identification mode	f_{SIDCK}	0	400	KHz	—
SD_CLK clock low time	t_{SHSCKL}	7	—	ns	2
SD_CLK clock high time	t_{SHSCKH}	7	—	ns	2
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	2
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	5	—	ns	2
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	0	—	ns	2
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	—	4	ns	2
Output Hold time: SD_CLK to SD_CMD, SD_DATx invalid	$t_{SHSKHOX}$	0	—	ns	2
SD_CLK delay within device	$t_{INT\_CLK\_DLY}$	1.5	—	ns	4
SD Card Input Setup	t_{ISU}	6	—	ns	3
SD Card Input Hold	t_{IH}	2	—	ns	3
SD Card Output Valid	t_{ODLY}	—	14	ns	3
SD Card Output Hold	t_{OH}	2.5	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

Table 49. PCI AC Timing Specifications at 66 MHz (continued)

PCI_SYNC_IN clock input levels are with next levels: VIL = $0.1 \times OV_{DD}$, VIH = $0.7 \times OV_{DD}$.

Parameter	Symbol[1]	Min	Max	Unit	Note
Input hold from cock	t_{PCIXKH}	0.25	—	ns	2, 4, 6
Output clock skew	t_{PCKOSK}	—	0.5	ns	5

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. PCI specifications allows 1 ns skew for 66 MHz but includes the total allowed skew, board, connectors, etc.
6. Value does not comply with the *PCI 2.3 Local Bus Specifications*.

This table shows the PCI AC timing specifications at 33 MHz.

Table 50. PCI AC Timing Specifications at 33 MHz

PCI_SYNC_IN clock input levels are with next levels: VIL = $0.1 \times OV_{DD}$, $V_{IH} = 0.7 \times OV_{DD}$.

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.25	—	ns	2, 4, 6
Output clock skew	t_{PCKOSK}	—	0.5	ns	5

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. PCI specifications allows 2 ns skew for 33 MHz but includes the total allowed skew, board, connectors, etc.
6. Value does not comply with the *PCI 2.3 Local Bus Specifications*.

15.2.1 Gen1i/1.5G Transmitter Specifications

This table provides the DC differential transmitter output DC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

Table 52. Gen1i/1.5G Transmitter (Tx) DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Tx differential output voltage	V_{SATA_TXDIFF}	400	500	600	mV_{p-p}	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Note:
1. Terminated by 50 Ω load.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

Table 53. Gen1i/1.5G Transmitter AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit interval	T_{UI}	666.4333	666.667	670.2333	ps	—
Total jitter, data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.355	UI_{p-p}	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.47	UI_{p-p}	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.175	UI_{p-p}	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.22	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

15.2.2 Gen2i/3G Transmitter Specifications

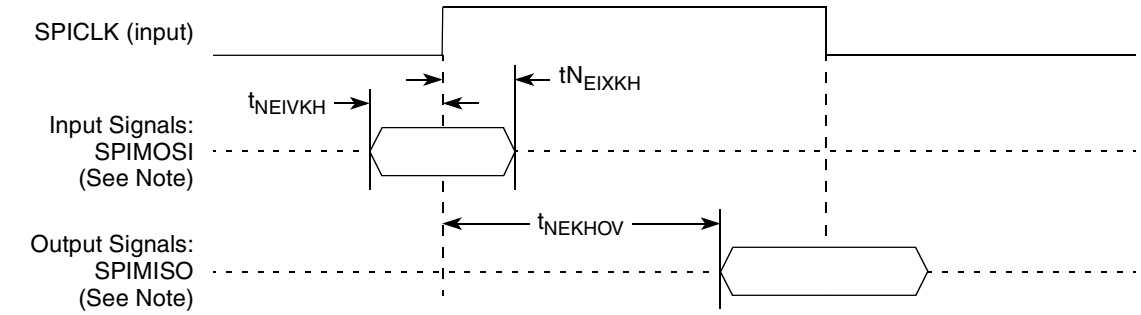
This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 54. Gen 2i/3G Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Tx differential output voltage	V_{SATA_TXDIFF}	400	550	700	mV_{p-p}	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Note:
1. Terminated by 50 Ω load.

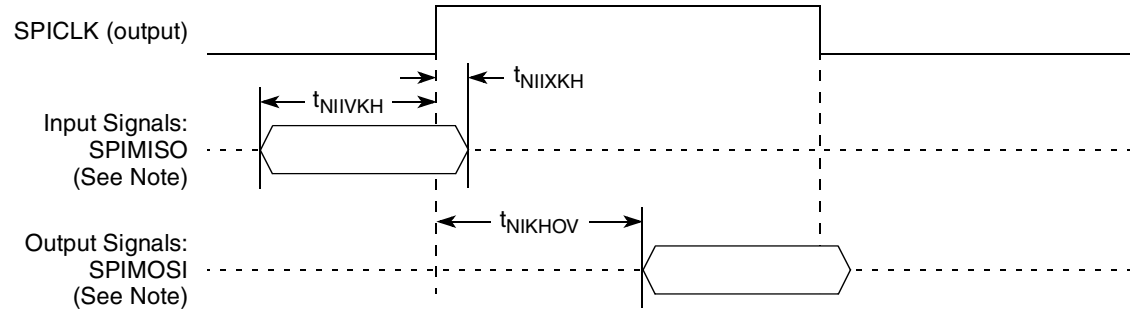
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 46. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 47. SPI AC Timing in Master Mode (Internal Clock) Diagram

20 High-Speed Serial Interfaces (HSSI)

This chip features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. See Table 1 for the interfaces supported.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 48 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

NOTE

Figure 53 to Figure 56 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by the clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the device SerDes reference clock receiver requirement provided in this document.

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with device SerDes reference clock input's DC requirement.

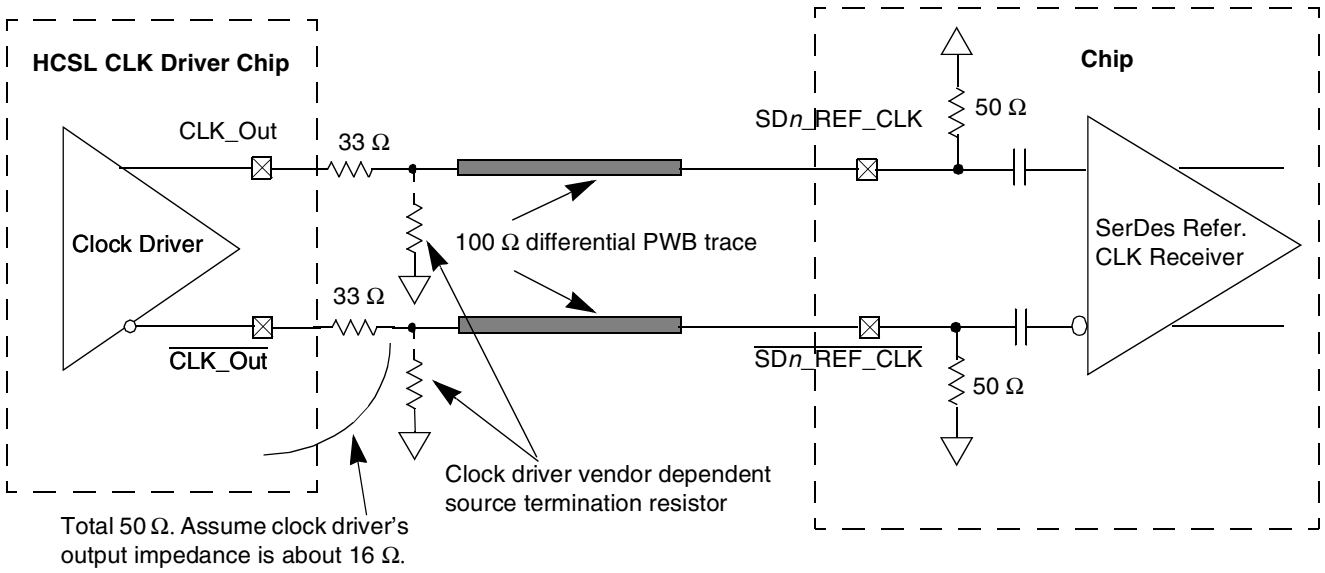


Figure 53. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common-mode voltage is higher than the device SerDes reference clock input's allowed range (100 to 400 mV), AC-coupled connection scheme must be used. It assumes the LVDS

occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SATAprotocols

Table 68. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS} or XV_{DD_SRDS} = 1.0 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SD*n*_REF_CLK) to falling edge rate ($\overline{\text{SD}n\text{\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 57.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD*n*_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 58.

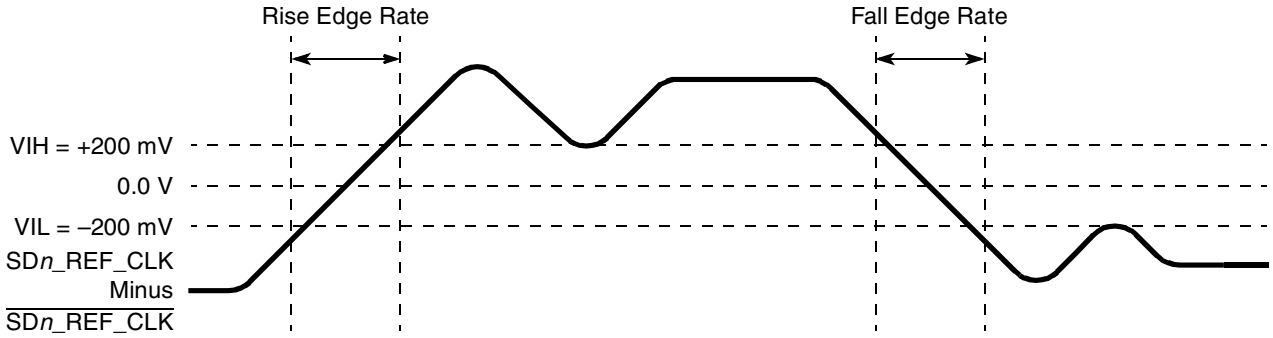


Figure 57. Differential Measurement Points for Rise and Fall Time

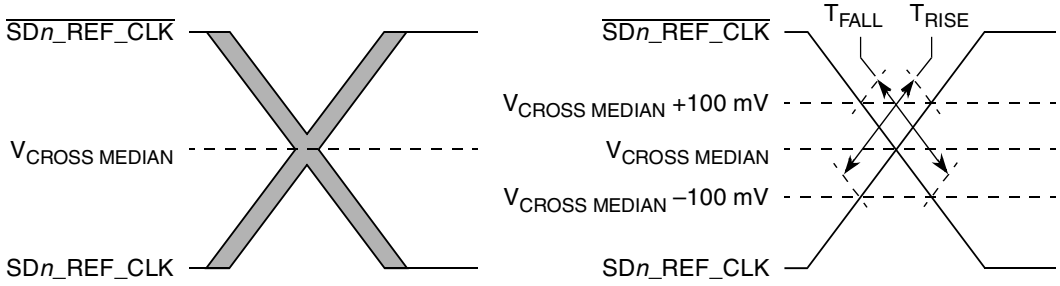


Figure 58. Single-Ended Measurement Points for Rise and Fall Time Matching

Table 69. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MBA2	M3	O	GVDD	—
MCAS_B	W5	O	GVDD	—
MCK_B0	H1	O	GVDD	—
MCK_B1	K1	O	GVDD	—
MCK_B2	V1	O	GVDD	—
MCK_B3	W2	O	GVDD	—
MCK_B4	AA1	O	GVDD	—
MCK_B5	AB2	O	GVDD	—
MCK0	J1	O	GVDD	—
MCK1	L1	O	GVDD	—
MCK2	V2	O	GVDD	—
MCK3	W1	O	GVDD	—
MCK4	Y1	O	GVDD	—
MCK5	AB1	O	GVDD	—
MCKE0	M4	O	GVDD	3
MCKE1	R5	O	GVDD	3
MCS_B0	W3	O	GVDD	—
MCS_B1	P3	O	GVDD	—
MCS_B2	T4	O	GVDD	—
MCS_B3	R4	O	GVDD	—
MDIC0	AH8	I/O	GVDD	9
MDIC1	AJ8	I/O	GVDD	9
MDM0	B6	O	GVDD	—
MDM1	B2	O	GVDD	—
MDM2	E2	O	GVDD	—
MDM3	E1	O	GVDD	—
MDM4	Y6	O	GVDD	—
MDM5	AC6	O	GVDD	—
MDM6	AE6	O	GVDD	—
MDM7	AJ4	O	GVDD	—
MDM8	L6	O	GVDD	—
MDQ0	A8	I/O	GVDD	11
MDQ1	A6	I/O	GVDD	11

Table 69. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
L1_XCOREVSS	AG14, AG15, AG16, AH16, AG18, AG20	SerDes Core GND	—	—
L1_XPADVDD	AE16, AF16, AD18, AE19, AF19	SerDes I/O Power (1.0 or 1.05 V)	—	—
L1_XPADVSS	AF14, AE17, AF20	SerDes I/O GND	—	—
SerDes2 Interface				
L2_SD_IMP_CAL_RX	C19	I	L2_XPADVDD	—
L2_SD_IMP_CAL_TX	C15	I	L2_XPADVDD	—
L2_SD_REF_CLK	B17	I	L2_XPADVDD	—
L2_SD_REF_CLK_B	A17	I	L2_XPADVDD	—
L2_SD_RXA_N	A19	I	L2_XPADVDD	—
L2_SD_RXA_P	B19	I	L2_XPADVDD	—
L2_SD_RXE_N	A15	I	L2_XPADVDD	—
L2_SD_RXE_P	B15	I	L2_XPADVDD	—
L2_SD_TXA_N	D18	O	L2_XPADVDD	—
L2_SD_TXA_P	E18	O	L2_XPADVDD	—
L2_SD_TXE_N	D15	O	L2_XPADVDD	—
L2_SD_TXE_P	E15	O	L2_XPADVDD	—
L2_SDAVDD_0	A16	SerDes PLL Power (1.0 or 1.05 V)	—	—
L2_SDAVSS_0	C17	SerDes PLL GND	—	—
L2_XCOREVDD	A14, B14, D17, B18, B20	SerDes Core Power (1.0 or 1.05 V)	—	—
L2_XCOREVSS	C14, C16, A18, C18, A20, C20	SerDes Core GND	—	—
L2_XPADVDD	D14, E16, F18, D19, E19	SerDes I/O Power (1.0 or 1.05 V)	—	—
L2_XPADVSS	D16, E17, D20	SerDes I/O GND	—	—
SPI Interface				
SPICLK/SD_CLK	AH9	I/O	OVDD	—

Table 75. CSB Frequency Options for Agent Mode (continued)

CFG_CLKIN_DIV at reset[1]	SPMF	*csb_clk* : Input Clock Ratio[1]	Input Clock Frequency (MHz)[2]		
			25	33.33	66.67
			csb_clk Frequency (MHz)		
Low	0111	7 : 1	175	233	
Low	1000	8 : 1	200	267	
Low	1001	9 : 1	225	300	
Low	1010	10 : 1	250	333	
Low	1011	11 : 1	275	367	
Low	1100	12 : 1	300	400	
Low	1101	13 : 1	325		
Low	1110	14 : 1	350		
Low	1111	15 : 1	375		

Notes:
1. CFG_CLKIN_DIV doubles csb_clk if set high.
2. CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

22.2 Core PLL Configuration

RCWLR[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 76 shows the encodings for RCWLR[COREPLL]. COREPLL values that are not listed in Table 76 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider
VCO divider has to be set properly so that the core VCO frequency is in the range of 800–1600 MHz.

Table 76. e300 Core PLL Configuration

RCWLR[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider [1]
0–1	**2–5**	**6**		
nn	**0000**	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	**nnnn**	n	n/a	n/a
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2

This table shows the heat sink thermal resistance for TePBGA II package with heat sinks, simulated in a standard JEDEC environment, per JESD 51-6.

Table 79. Thermal Resistance with Heat Sink in Open Flow (TePBGA II)

Heat Sink Assuming Thermal Grease	Air Flow	Thermal Resistance (°/W)
AAVID 30 × 30 × 9.4 mm Pin Fin	Natural Convection	13.1
	0.5 m/s	10.6
	1 m/s	9.3
	2 m/s	8.2
	4 m/s	7.5
AAVID 31 × 35 × 23 mm Pin Fin	Natural Convection	11.1
	0.5 m/s	8.5
	1 m/s	7.7
	2 m/s	7.2
	4 m/s	6.8
AAVID 43× 41× 16.5mm Pin Fin	Natural Convection	11.3
	0.5 m/s	9.0
	1 m/s	7.8
	2 m/s	7.0
	4 m/s	6.5
Wakefield, 53 × 53 × 25 mm Pin Fin	Natural Convection	9.7
	0.5 m/s	7.7
	1 m/s	6.8
	2 m/s	6.4
	4 m/s	6.1

Heat sink vendors include the following:

Aavid Thermalloy
www.aavidthermalloy.com

Alpha Novatech
www.alphanovatech.com

International Electronic Research Corporation (IERC)
www.ctscorp.com

Millennium Electronics (MEI)
www.mei-thermal.com

Table 84. Document Revision History (continued)

Revision	Date	Substantive Change(s)
2	10/2009	• In Table 3, “Recommended Operating Conditions,” added “Operating temperature range” values. • In Table 5, “Power Dissipation [1],” corrected maximal application for 800/400 MHz to 4.3 W. • In Table 5, “Power Dissipation [1],” added a column for “Typical Application at T_j = 65°C (W)”. • In Table 5, “Power Dissipation [1],” added a column for “Sleep Power at T_j = 65°C (W)”. • In Table 11, removed overbar from CFG_CLKIN_DIV. • In Table 17, “Current Draw Characteristics for MV_{REF},” updated I_{MVREF} maximum value for both DDR1 and DDR2 to 600 and 400 µA, respectively. Also, updated Note 1 and added Note 2. • In Table 20, “DDR1 and DDR2 SDRAM Input AC Timing Specifications,” column headings renamed to “Min” and “Max”. Footnote 2 updated to state “T is the MCK clock period”. • In Table 20, “DDR1 and DDR2 SDRAM Input AC Timing Specifications,” and Table 21, “DDR1 and DDR2 SDRAM Output AC Timing Specifications,” clarified that the frequency parameters are data rates. • In Table 29, “RMII Transmit AC Timing Specifications,” updated t_{RMTDX}l to 2.0 ns. • In Table 57, Gen 1i/1.5G Transmitter AC Specifications,” and Table 59, Gen 2i/3G Transmitter AC Specifications,” corrected titles from “Transmitter” to “Receiver”. • In Table 69, “TePBGA II Pinout Listing,” removed pin THERM0; it is now Reserved. Also added 1.05 V to VDD pin. • In Table 71, “Operating Frequencies for TePBGA II,” corrected “DDR2 memory bus frequency (MCK)” range to 125–200. • In Table 76, “e300 Core PLL Configuration,” added 3.5:1 and 4:1 core_clk: csb_clk ratio options. • In Table 77, “Example Clock Frequency Combinations,” updated column heading to “DDR data rate” . • In Section 19.2, “SPI AC Timing Specifications,” corrected t_{NIKHOX} and t_{NEKHOX} to t_{NIKHOV} and t_{NEKHOV}, respectively.
1	02/2009	• In Table 3, “Recommended Operating Conditions,” added two new rows for 800 MHz, and created two rows for SerDes. In addition, changed 666 to 667 MHz. • In Table 5, “Power Dissipation [1],” added Notes 4 and 5. In addition, changed 666 to 667 MHz. • In Table 13, “DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V,” Table 21, “DDR1 and DDR2 SDRAM Output AC Timing Specifications,” and Table 69, “TePBGA II Pinout Listing,” added footnote to references to MVREF, MDQ, and MDQS, referencing AN3665, *MPC837xE Design Checklist*. • In Table 21, updated t_{DDKHCX} minimum value for 333 MHz to 2.40. • In Table 69, “TePBGA II Pinout Listing,” added footnote to USBDR_STP_SUSPEND and modified footnote 10 and added footnote 15. • In Table 71, “Operating Frequencies for TePBGA II,” changed 667 to 800 MHz for *core_clk*. • In Table 77, “Example Clock Frequency Combinations,” added 800 MHz cells for e300 core. • Updated part numbering information in AF column in Table 81, “Part Numbering Nomenclature.” In addition, modified extended temperature information in notes 1 and 4. • In Table 82, “Available Parts (Core/DDR Data Rate),” added new row for 800/400 MHz.
0	12/2008	Initial public release.