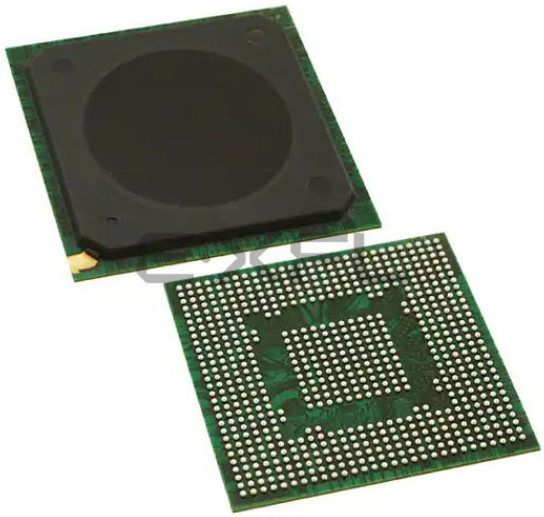

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Security; SEC 3.0
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (4)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 125°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8379evralg

controller, dual I^2C controllers, a 4-channel DMA controller, an enhanced secured digital host controller, and a general-purpose I/O port. This figure shows the block diagram of the chip.

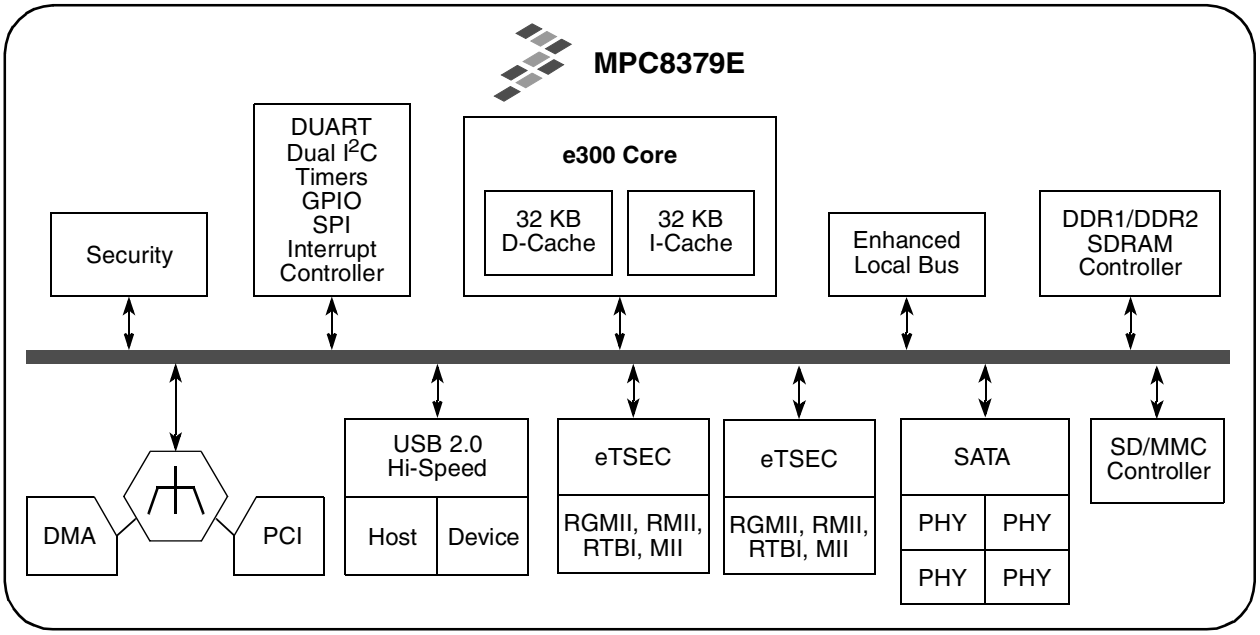

Figure 1. MPC8379E Block Diagram and Features

The following features are supported in the chip:

- e300c4s core built on Power Architecture® technology with 32 KB instruction cache and 32 KB data cache, a floating point unit, and two integer units
- DDR1/DDR2 memory controller supporting a 32/64-bit interface
- Peripheral interfaces, such as a 32-bit PCI interface with up to 66-MHz operation
- 32-bit local bus interface running up to 133-MHz
- USB 2.0 (full/high speed) support
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration
- Optional security engine provides acceleration for control and data plane security protocols

The optional security engine (SEC 3.0) is noted with the extension “E” at the end. It allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

This table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD}/LBV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	L[1,2]_nV_{DD} (1.0 V)	Unit	Comments
DDR I/O 65% utilization 2 pair of clocks	200 MHz data rate, 32-bit	0.28	0.35	—	—	—	—	W	—
	200 MHz data rate, 64-bit	0.41	0.49	—	—	—	—	W	
	266 MHz data rate, 32-bit	0.31	0.4	—	—	—	—	W	
	266 MHz data rate, 64-bit	0.46	0.56	—	—	—	—	W	
	300 MHz data rate, 32-bit	0.33	0.43	—	—	—	—	W	
	300 MHz data rate, 64-bit	0.48	0.6	—	—	—	—	W	
	333 MHz data rate, 32-bit	0.35	0.45	—	—	—	—	W	
	333 MHz data rate, 64-bit	0.51	0.64	—	—	—	—	W	
	400 MHz data rate, 32-bit	0.38	—	—	—	—	—	W	
	400 MHz data rate, 64-bit	0.56	—	—	—	—	—	W	
PCI I/O Load = 30 pf	33 MHz, 32-bit	—	—	0.04	—	—	—	W	—
	66 MHz, 32-bit	—	—	0.07	—	—	—	W	
Local Bus I/O Load = 25 pf	167 MHz, 32-bit	0.09	0.17	0.29	—	—	—	W	—
	133 MHz, 32-bit	0.07	0.14	0.24	—	—	—	W	
	83 MHz, 32-bit	0.05	0.09	0.15	—	—	—	W	
	66 MHz, 32-bit	0.04	0.07	0.13	—	—	—	W	
	50 MHz, 32-bit	0.03	0.06	0.1	—	—	—	W	

Table 16 provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 17. Current Draw Characteristics for MV_{REF}

Parameter	Symbol	Min	Typ	Max	Unit	Note
Current draw for MV_{REF} DDR1 DDR2	I_{MVREF}	 — —	 250 150	 600 400	µA	1, 2

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to the stated maximum current.
2. This current is divided equally between MVREF1 and MVREF2, where half the current flows through each pin.

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when GVDD(typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V

This table provides the input AC timing specifications for the DDR1 SDRAM when GV_{DD}(typ) = 2.5 V.

Table 19. DDR1 SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII/RTBI/RMII DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

8.1.1 MII, RMII, RGMII, and RTBI DC Electrical Characteristics

MII and RMII drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals in Table 25 are based on a 2.5 V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 24. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage 3.3 V	LV_{DD1} LV_{DD2}	3.13	3.47	V	1
Output high voltage (LV_{DD1}/LV_{DD2} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	LV_{DD1}/LV_{DD2} + 0.3	V	—
Output low voltage (LV_{DD1}/LV_{DD2} = Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	LV_{DD1}/LV_{DD2} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD1}, V_{IN} = LV_{DD2})	I_{IH}	—	30	μA	1
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	—

Notes:
1. LV_{DD1} supports eTSEC 1. LV_{DD2} supports eTSEC 2.

Table 27. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock rise time (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

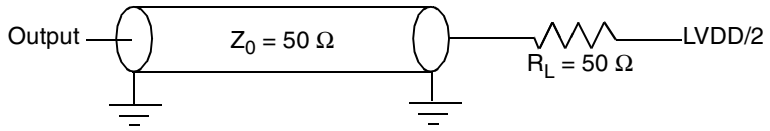

Figure 8. eTSEC AC Test Load

This figure shows the MII receive AC timing diagram.

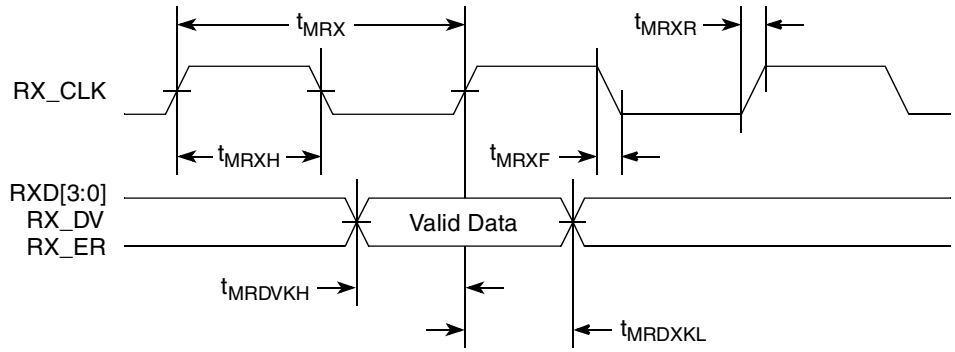

Figure 9. MII Receive AC Timing Diagram

8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 28. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT}	–600	0	600	ps	—
Data to clock input skew (at receiver)	t_{SKRGT}	1.0	—	2.8	ns	2
Clock period	t_{RGT}	7.2	8.0	8.8	ns	3

Table 29. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

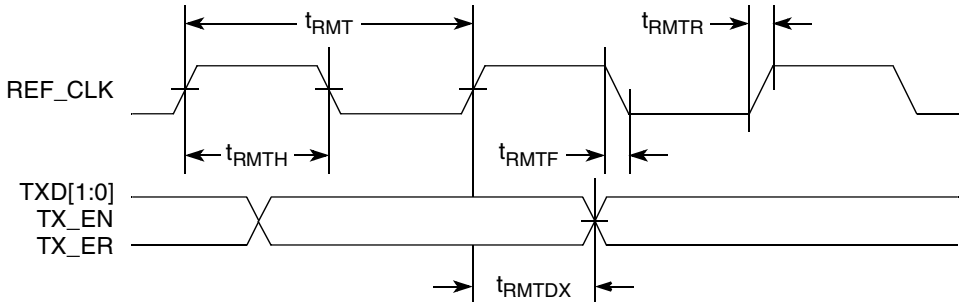

Figure 12. RMII Transmit AC Timing Diagram

8.2.3.2 RMII Receive AC Timing Specifications

This table shows the RMII receive AC timing specifications.

Table 30. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
Input low voltage at 3.3 LV_{DD}	V_{IL}	—	—	0.8	V
Input high voltage at 3.3 LV_{DD}	V_{IH}	2.0	—	—	V
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns

These two figures provide the AC test load and signals for the USB, respectively.

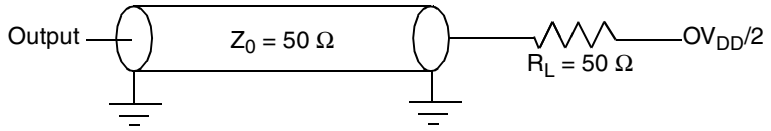

Figure 17. USB AC Test Load

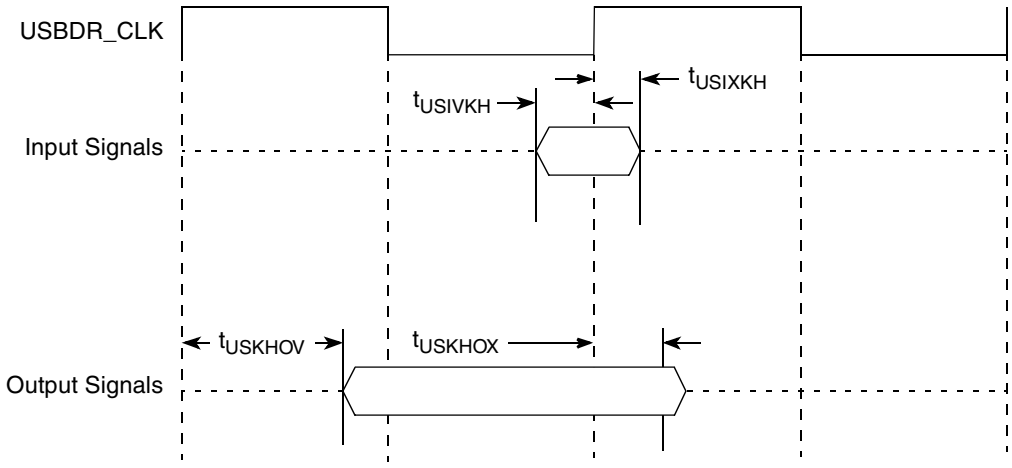

Figure 18. USB Interface Timing Diagram

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the chip.

10.1 Local Bus DC Electrical Characteristics

This tables provide the DC electrical characteristics for the local bus interface.

Table 36. Local Bus DC Electrical Characteristics (LBV_{DD} = 3.3 V)

At recommended operating conditions with LBV_{DD} = 3.3 V.

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage 3.3 V	—		LBV_{DD}	3.135	3.465	V
Output high voltage	I_{OH} = –4.0 mA	LBV_{DD} = Min	V_{OH}	2.40	—	V
Output low voltage	I_{OL} = 4.0 mA	LBV_{DD} = Min	V_{OL}	—	0.50	V
Input high voltage	—	—	V_{IH}	2.0	LBV_{DD} + 0.3	V
Input low voltage	—	—	V_{IL}	–0.3	0.90	V
Input high current	V_{IN} [1] = LBV_{DD}		I_{IH}	—	30	μA
Input low current	V_{IN} [1] = GND		I_{IL}	–30	—	μA

This figures show the local bus signals.

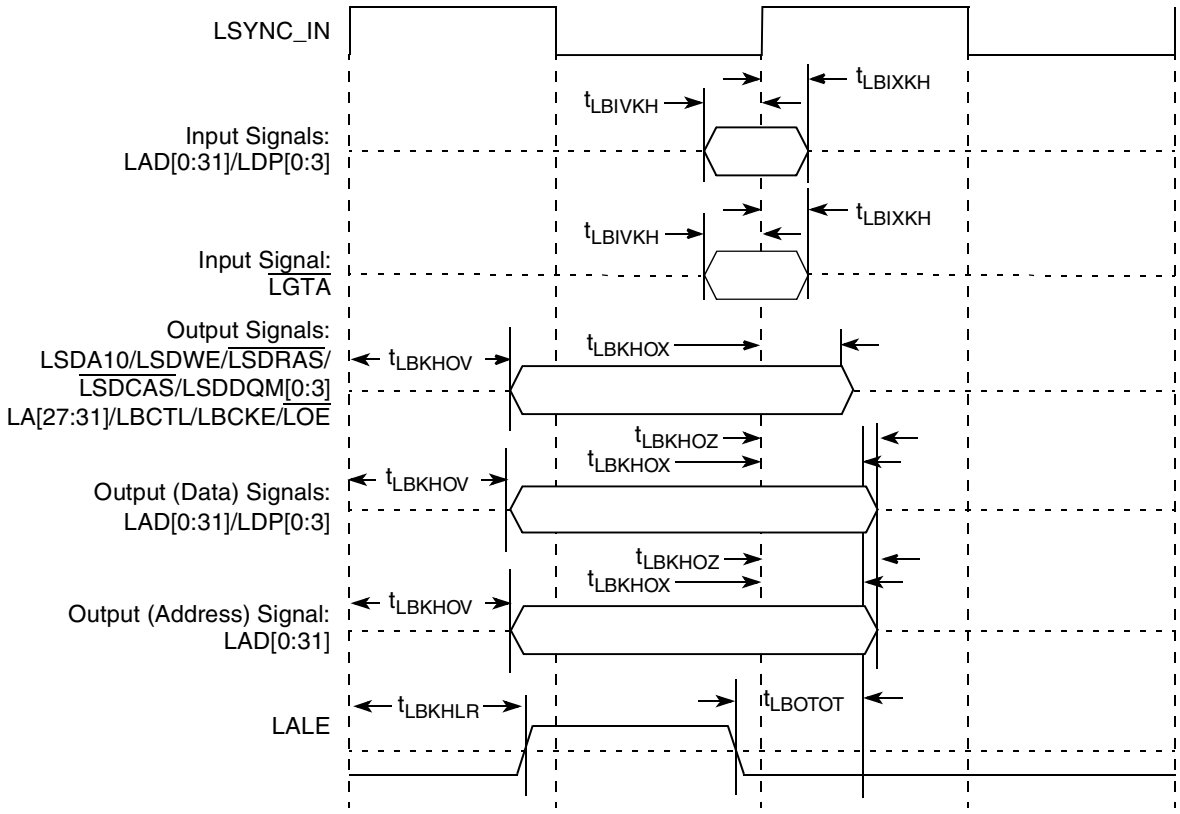

Figure 20. Local Bus Signals, Non-special Signals Only (PLL Enable Mode)

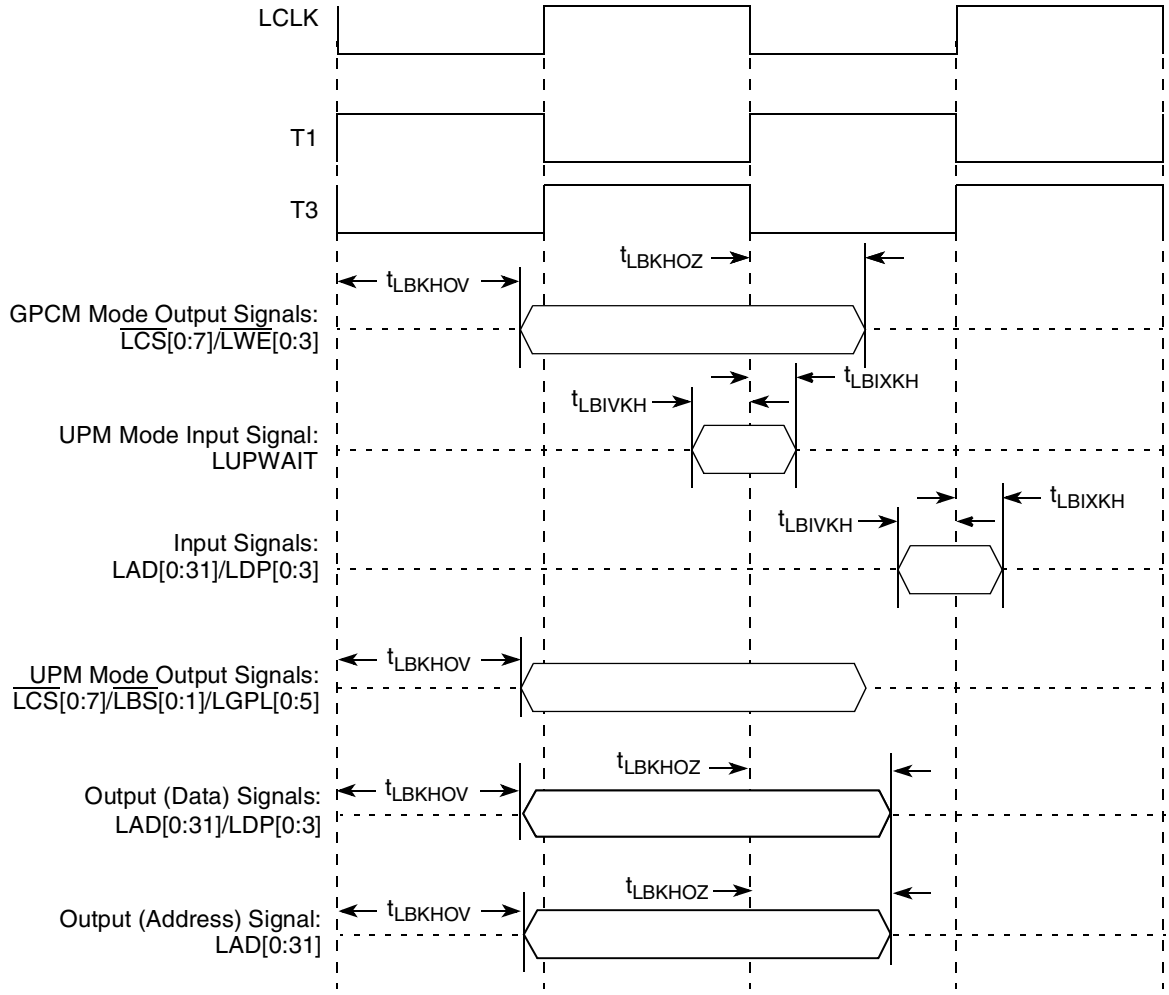

Figure 23. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Bypass Mode)

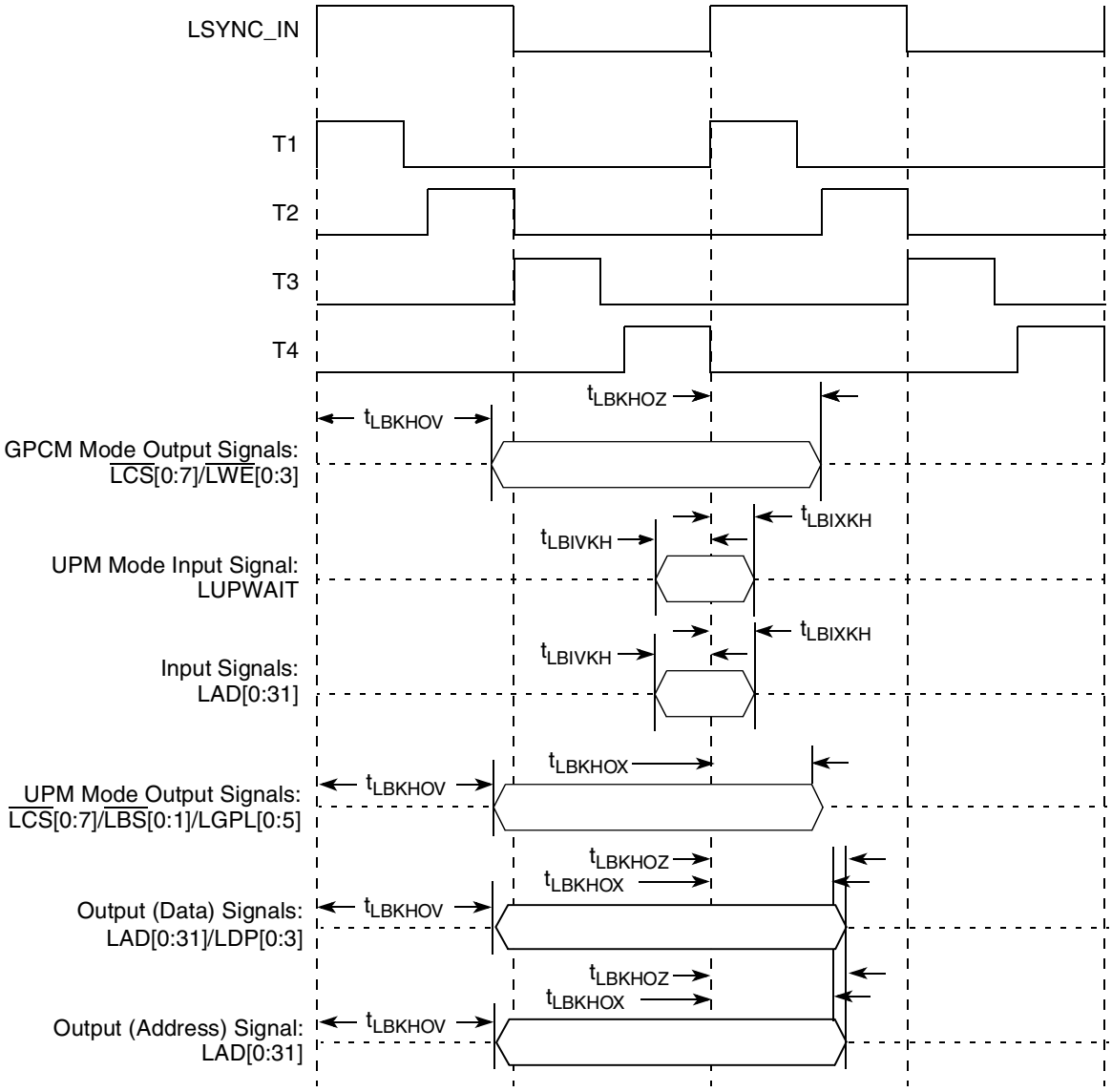

Figure 24. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Enable Mode)

Table 45. JTAG AC Timing Specifications (Independent of CLKIN) [1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 17). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

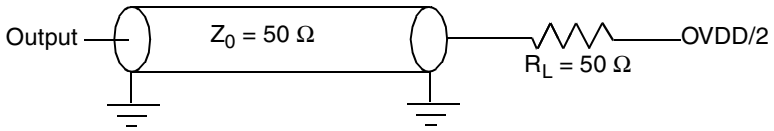

Figure 32. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

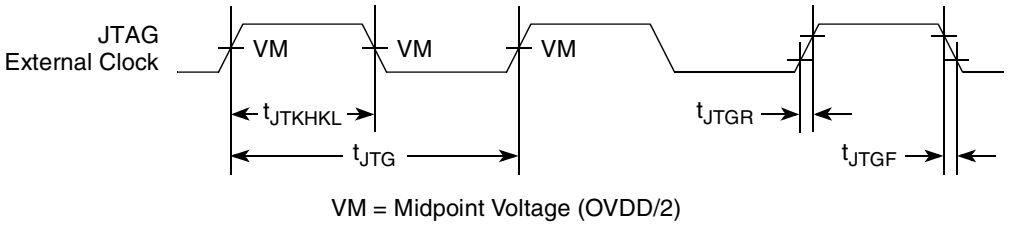

Figure 33. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

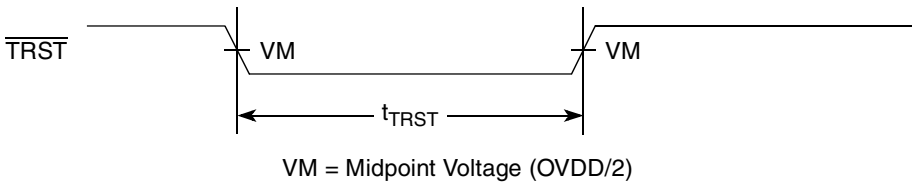

Figure 34. $\overline{\text{TRST}}$ Timing Diagram

13 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface of the chip.

13.1 I^2C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interface of the chip.

Table 46. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 165 mV.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	± 30	µA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8379E PowerQUICC II Pro Integrated Host Processor Reference Manual* for information on the digital filter used.
4. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

13.2 I^2C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interface of the device.

Table 47. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	—
Low period of the SCL clock	t_{I2CL}	1.3	—	µs	—
High period of the SCL clock	t_{I2CH}	0.6	—	µs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs	—
Data setup time	t_{I2DVKH}	100	—	ns	—

Table 47. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol[1]	Min	Max	Unit	Note
Data hold time CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — 0.9	µs	2, 3
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This chip provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

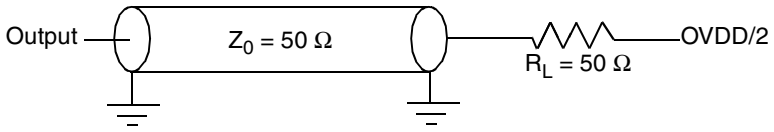

Figure 37. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

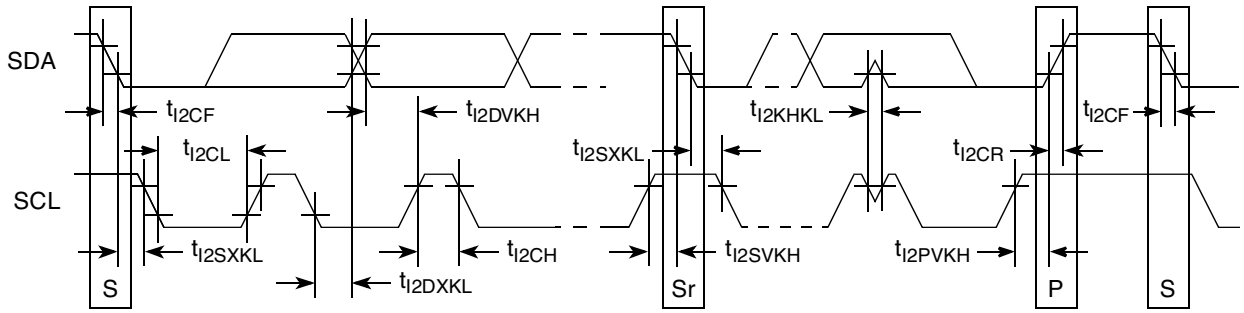

Figure 38. I²C Bus AC Timing Diagram

This figure provides the AC test load for the GPIO.

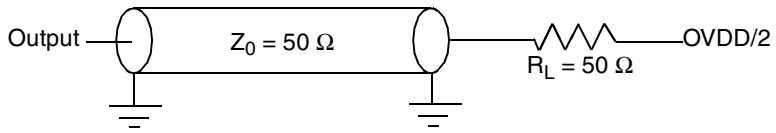

Figure 44. GPIO AC Test Load

18 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the chip.

18.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the chip.

Table 64. IPIC DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	—	I_{IN}	—	±30	μA
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V

Note:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

18.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 65. IPIC Input AC Timing Specifications

Parameter	Symbol	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

19 SPI

This section describes the DC and AC electrical specifications for the SPI of the chip.

output driver features a 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

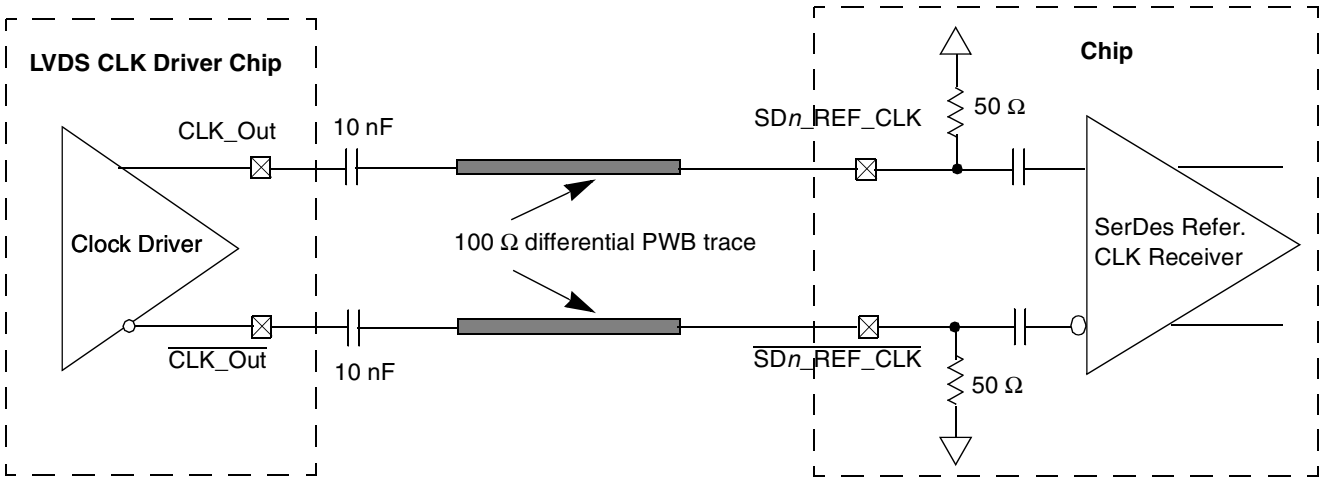

Figure 54. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 55 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with device SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 55 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50 Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the device SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Consult clock

Table 69. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MBA2	M3	O	GVDD	—
MCAS_B	W5	O	GVDD	—
MCK_B0	H1	O	GVDD	—
MCK_B1	K1	O	GVDD	—
MCK_B2	V1	O	GVDD	—
MCK_B3	W2	O	GVDD	—
MCK_B4	AA1	O	GVDD	—
MCK_B5	AB2	O	GVDD	—
MCK0	J1	O	GVDD	—
MCK1	L1	O	GVDD	—
MCK2	V2	O	GVDD	—
MCK3	W1	O	GVDD	—
MCK4	Y1	O	GVDD	—
MCK5	AB1	O	GVDD	—
MCKE0	M4	O	GVDD	3
MCKE1	R5	O	GVDD	3
MCS_B0	W3	O	GVDD	—
MCS_B1	P3	O	GVDD	—
MCS_B2	T4	O	GVDD	—
MCS_B3	R4	O	GVDD	—
MDIC0	AH8	I/O	GVDD	9
MDIC1	AJ8	I/O	GVDD	9
MDM0	B6	O	GVDD	—
MDM1	B2	O	GVDD	—
MDM2	E2	O	GVDD	—
MDM3	E1	O	GVDD	—
MDM4	Y6	O	GVDD	—
MDM5	AC6	O	GVDD	—
MDM6	AE6	O	GVDD	—
MDM7	AJ4	O	GVDD	—
MDM8	L6	O	GVDD	—
MDQ0	A8	I/O	GVDD	11
MDQ1	A6	I/O	GVDD	11

Table 69. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC2_RXD0/GPIO1[16]	AE28	I/O	LVDD2	17
TSEC2_RXD1/GPIO1[15]	AE29	I/O	LVDD2	17
TSEC2_RXD2/GPIO1[14]	AH26	I/O	LVDD2	17
TSEC2_RXD3/GPIO1[13]	AH25	I/O	LVDD2	17
TSEC2_TX_CLK/GPIO2[24]/ TSEC1_TMR_GCLK	AG28	I/O	LVDD2	17
TSEC2_TX_EN/GPIO1[12]/ TSEC1_TMR_ALARM2	AJ26	I/O	LVDD2	17
TSEC2_TX_ER/GPIO1[24]/ TSEC1_TMR_ALARM1	AG26	I/O	LVDD2	17
TSEC2_TXD0/GPIO1[20]	AH28	I/O	LVDD2	17
TSEC2_TXD1/GPIO1[19]/ TSEC1_TMR_PP1	AF27	I/O	LVDD2	17
TSEC2_TXD2/GPIO1[18]/ TSEC1_TMR_PP2	AJ28	I/O	LVDD2	17
TSEC2_TXD3/GPIO1[17]/ TSEC1_TMR_PP3	AF29	I/O	LVDD2	17
GPIO1 Interface				
GPIO1[0]/GTM1_TIN1/ GTM2_TIN2/DREQ0_B	P25	I/O	OVDD	—
GPIO1[1]/GTM1_TGATE1_B/ GTM2_TGATE2_B/DACK0_B	N25	I/O	OVDD	—
GPIO1[2]/GTM1_TOUT1_B/ DDONE0_B	N26	I/O	OVDD	—
GPIO1[3]/GTM1_TIN2/ GTM2_TIN1/DREQ1_B	B9	I/O	OVDD	—
GPIO1[4]/GTM1_TGATE2_B/ GTM2_TGATE1_B/DACK1_B	N29	I/O	OVDD	—
GPIO1[5]/GTM1_TOUT2_B/ GTM2_TOUT1_B/DDONE1_B	M29	I/O	OVDD	—
GPIO1[6]/GTM1_TIN3/ GTM2_TIN4/DREQ2_B	A9	I/O	OVDD	—
GPIO1[7]/GTM1_TGATE3_B/ GTM2_TGATE4_B/DACK2_B	B10	I/O	OVDD	—
GPIO1[8]/GTM1_TOUT3_B/ DDONE2_B	J26	I/O	OVDD	—
GPIO1[9]/GTM1_TIN4/ GTM2_TIN3/DREQ3_B	J24	I/O	OVDD	—

Table 72. System PLL Multiplication Factors

RCWLR[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	× 7 to × 15

As described in Section 22, "Clocking," The LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 74 and Table 75 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

The RCWLR[SVCOD] denotes the system PLL VCO internal frequency as shown in Table 73.

Table 73. System PLL VCO Divider

RCWLR[SVCOD]	VCO Division Factor
00	4
01	8
10	2
11	1

Table 74. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[1]	Input Clock Frequency (MHz)[2]		
			25	33.33	66.67
			csb_clk Frequency (MHz)		
High	0010	2 : 1			133
High	0011	3 : 1			200
High	0100	4 : 1		133	267
High	0101	5 : 1		167	333
High	0110	6 : 1	150	200	400

Table 74. CSB Frequency Options for Host Mode (continued)

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[1]	Input Clock Frequency (MHz)[2]		
			25	33.33	66.67
			csb_clk Frequency (MHz)		
High	0111	7 : 1	175	233	
High	1000	8 : 1	200	267	
High	1001	9 : 1	225	300	
High	1010	10 : 1	250	333	
High	1011	11 : 1	275	367	
High	1100	12 : 1	300	400	
High	1101	13 : 1	325		
High	1110	14 : 1	350		
High	1111	15 : 1	375		

Notes:
1. CFG_CLKIN_DIV select the ratio between CLKIN and PCI_SYNC_OUT.
2. CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 75. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at reset[1]	SPMF	*csb_clk* : Input Clock Ratio[1]	Input Clock Frequency (MHz)[2]		
			25	33.33	66.67
			csb_clk Frequency (MHz)		
Low	0010	2 : 1			133
Low	0011	3 : 1			200
Low	0100	4 : 1		133	267
Low	0101	5 : 1		167	333
Low	0110	6 : 1	150	200	400

Table 76. e300 Core PLL Configuration (continued)

RCWLR[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider [1]
0–1	2–5	6		
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4
10	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8
00	**0011**	1	3.5:1	2
01	**0011**	1	3.5:1	4
10	**0011**	1	3.5:1	8
00	**0100**	0	4:1	2
01	**0100**	0	4:1	4
10	**0100**	0	4:1	8

Notes:
1. Core VCO frequency = Core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 800–1600 MHz.

22.3 Suggested PLL Configurations

This table shows suggested PLL configurations for different input clocks (LBCM = 0).

Table 77. Example Clock Frequency Combinations

								eLBC [1]			e300 Core [1]				
Ref [1]	**LBCM**	**DDRCM**	**SVCOD**	**SPMF**	**Sys VCO[1,2]**	**CSB[1,3]**	**DDR data rate[1,4]**	**/2**	**/4**	**/8**	**× 1**	**× 1.5**	**× 2**	**× 2.5**	**× 3**
25.0	0	1	2	5	500	125	250	62.5	31.3	15.6	—	—	—	—	375
25.0	0	1	2	6	600	150	300	75 [6]	37.5	18.8	—	—	—	375	450
33.3	0	1	2	5	667	167	333	83.3 [6]	41.6	20.8	—	—	333	416	500
33.3	0	1	2	4	533	133	267	66.7	33.3	16.7	—	—	—	333	400