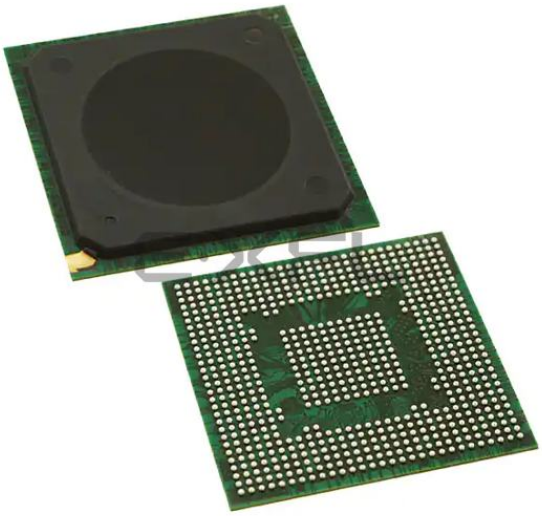

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (4)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 125°C (TA)
Security Features	-
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8379vralg

controller, dual I^2C controllers, a 4-channel DMA controller, an enhanced secured digital host controller, and a general-purpose I/O port. This figure shows the block diagram of the chip.

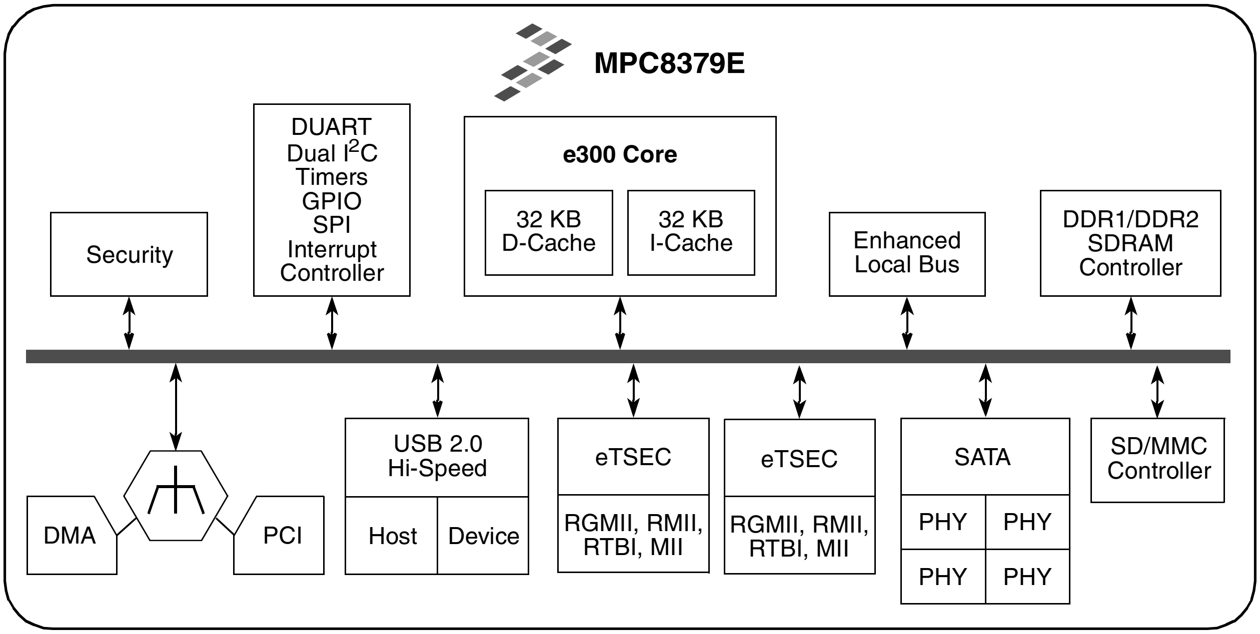


Figure 1. MPC8379E Block Diagram and Features

The following features are supported in the chip:

- e300c4s core built on Power Architecture® technology with 32 KB instruction cache and 32 KB data cache, a floating point unit, and two integer units
- DDR1/DDR2 memory controller supporting a 32/64-bit interface
- Peripheral interfaces, such as a 32-bit PCI interface with up to 66-MHz operation
- 32-bit local bus interface running up to 133-MHz
- USB 2.0 (full/high speed) support
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration
- Optional security engine provides acceleration for control and data plane security protocols

The optional security engine (SEC 3.0) is noted with the extension "E" at the end. It allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

Table 6. Typical I/O Power Dissipation (continued)

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD}/LBV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	L[1,2]_nV_{DD} (1.0 V)	Unit	Comments
eTSEC I/O Load = 25 pf	MII or RMII	—	—	—	0.02	—	—	W	Multiply by number of interfaces used.
	RGMII or RTBI	—	—	—	—	0.05	—	W	—
USB (60MHz Clock)	12 Mbps	—	—	0.01	—	—	—	W	—
	480 Mbps	—	—	0.2	—	—	—	W	
SerDes	per lane	—	—		—	—	0.029	W	—
Other I/O	—	—	—	0.01	—	—	—	W	—

Note: The values given are for typical, and not worst case, switching.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the chip. Note that the PCI_CLK/PCI_SYNC_IN signal or CLKIN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. CLKIN is used when the device is in host mode.

4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_CLK) DC timing specifications for the device.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit	Note
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V	1
Input low voltage	—	V_{IL}	–0.3	0.4	V	1
CLKIN Input current	$0 V \le V_{IN} \le OV_{DD}$	I_{IN}	—	± 10	µA	—
PCI_CLK Input current	$0 V \le V_{IN} \le 0.5 V$ or $OV_{DD} - 0.5 V \le V_{IN} \le OV_{DD}$	I_{IN}	—	± 30	µA	—

Note:
1. In PCI agent mode, this specification does not comply with *PCI 2.3 Specification*.

Table 16 provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 17. Current Draw Characteristics for MV_{REF}

Parameter	Symbol	Min	Typ	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}				μA	1, 2
DDR1		—	250	600		
DDR2		—	150	400		

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to the stated maximum current.
2. This current is divided equally between MVREF1 and MVREF2, where half the current flows through each pin.

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when GVDD(typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V

This table provides the input AC timing specifications for the DDR1 SDRAM when GV_{DD}(typ) = 2.5 V.

Table 19. DDR1 SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V

Table 29. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

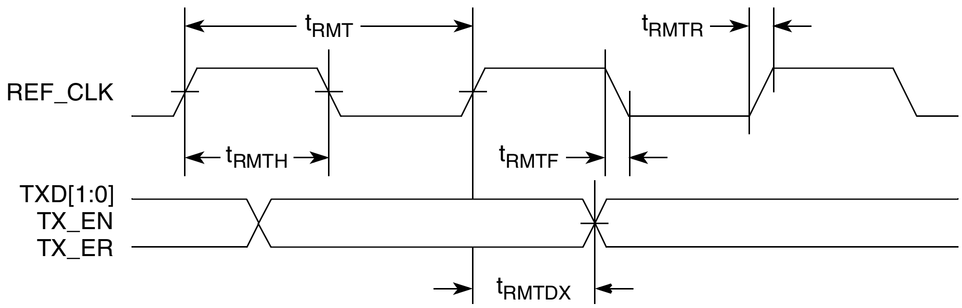


Figure 12. RMII Transmit AC Timing Diagram

8.2.3.2 RMII Receive AC Timing Specifications

This table shows the RMII receive AC timing specifications.

Table 30. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
Input low voltage at 3.3 LV_{DD}	V_{IL}	—	—	0.8	V
Input high voltage at 3.3 LV_{DD}	V_{IH}	2.0	—	—	V
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns

Table 39. Local Bus General Timing Parameters—PLL Enable Mode (continued)

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	3, 8
Output hold from local bus clock for LAD/LDP	t_{LBKHOX}	1	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to rising edge of LSYNC_IN at $LBV_{DD}/2$ and the $0.4 \times LBV_{DD}$ of the signal in question.
3. All signals are measured from $LBV_{DD}/2$ of the rising/falling edge of LSYNC_IN to $0.5 \times LBV_{DD}$ of the signal in question.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when LBCR[AHD] is set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when LBCR[AHD] is not set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when LBCR[AHD] is not set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

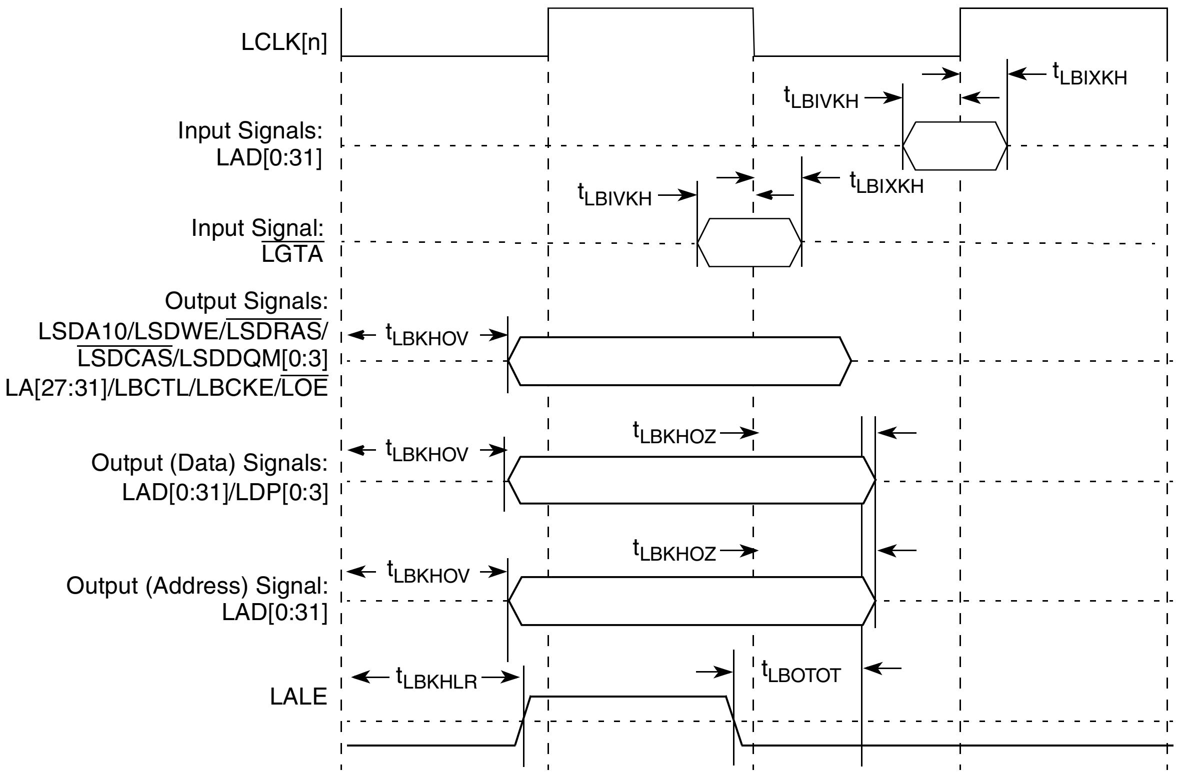


Figure 21. Local Bus Signals, Non-special Signals Only (PLL Bypass Mode)

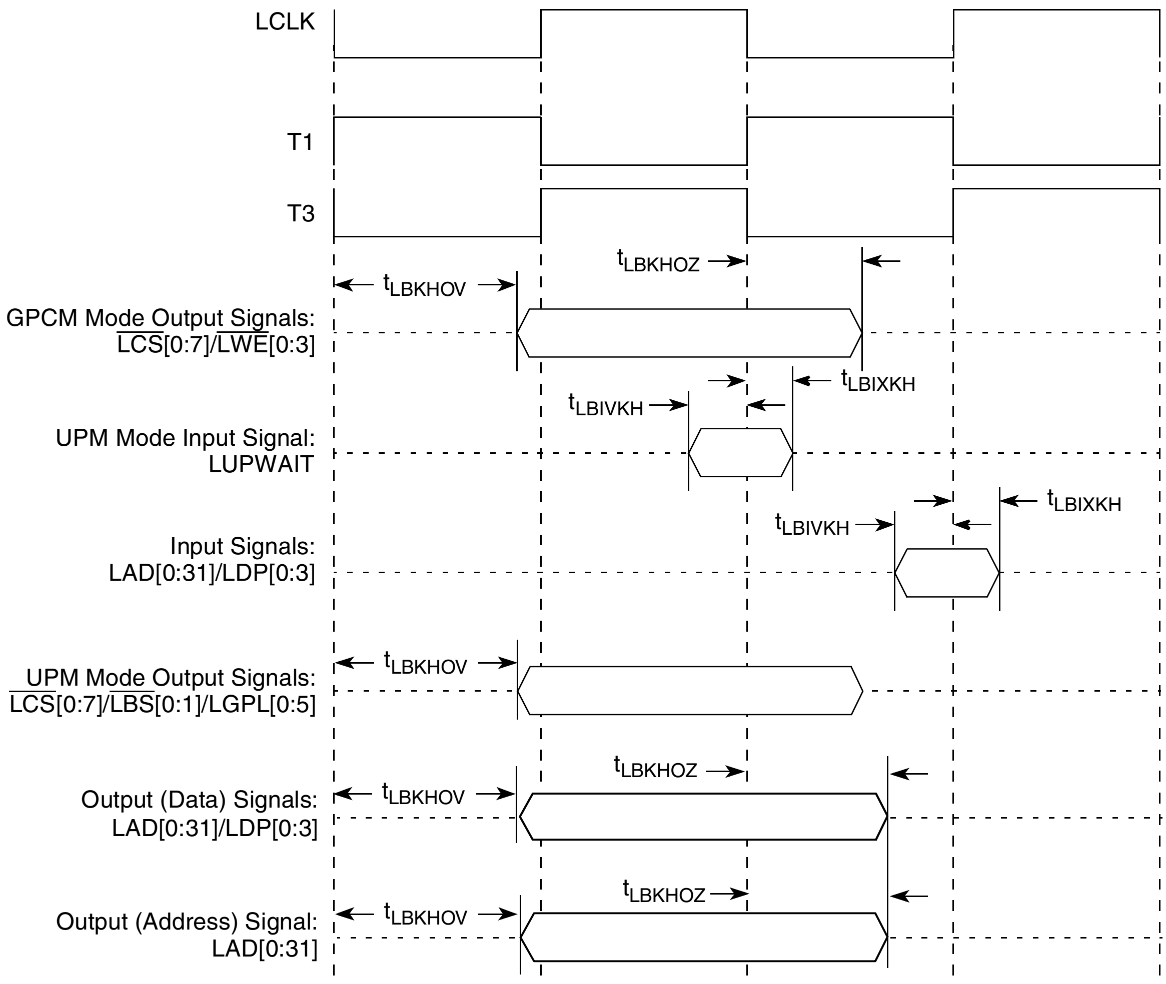


Figure 23. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Bypass Mode)

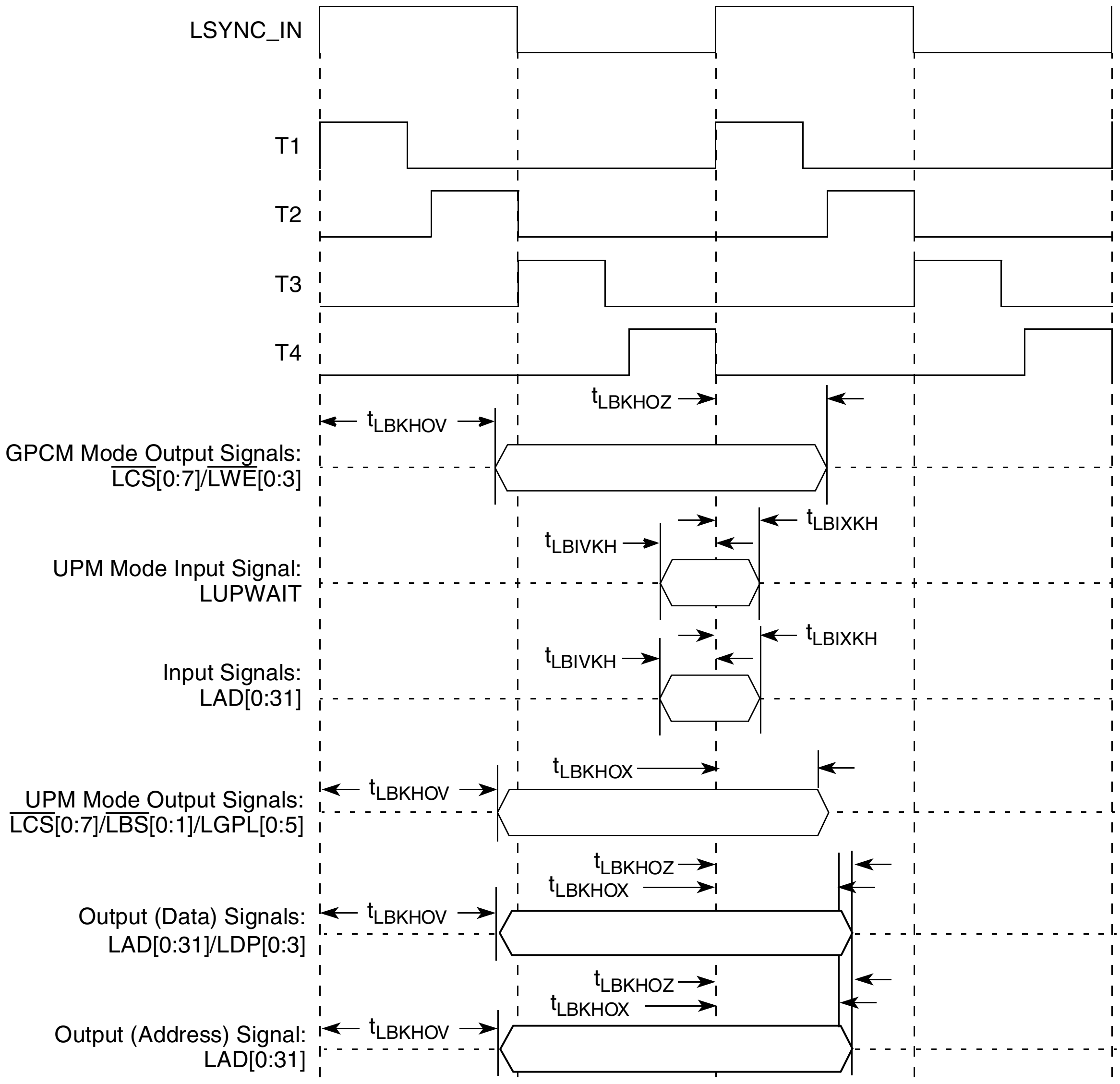


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Enable Mode)

Table 42. eSDHC AC Timing Specifications for Full-Speed Mode (continued)

At recommended operating conditions OV_{DD} = 3.3 V ± 165 mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
Input hold times: SD_CMD, SD_DAT*x*, SD_CD to SD_CLK	$t_{SFSIXKH}$	0	—	ns	2
SD_CLK delay within device	$t_{INT\_CLK\_DLY}$	1.5	—	ns	4
Output valid: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOV}$	—	4	ns	2
Output hold: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOX}$	0	—	—	—
SD card input setup	t_{ISU}	5	—	ns	3
SD card input hold	t_{IH}	5	—	ns	3
SD card output valid	t_{ODLY}	—	14	ns	3
SD card output hold	t_{OH}	0	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

This figure provides the eSDHC clock input timing diagram.

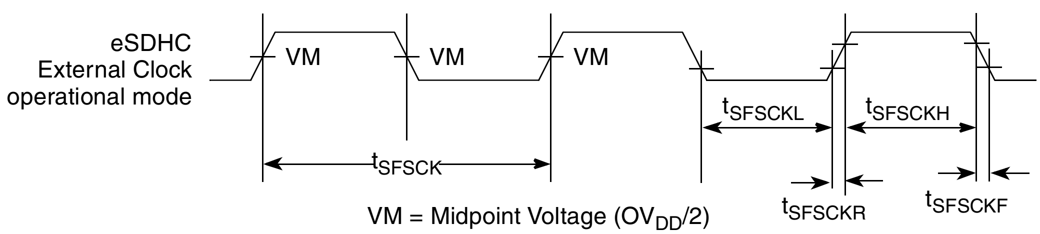


Figure 26. eSDHC Clock Input Timing Diagram

11.2.1 Full-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

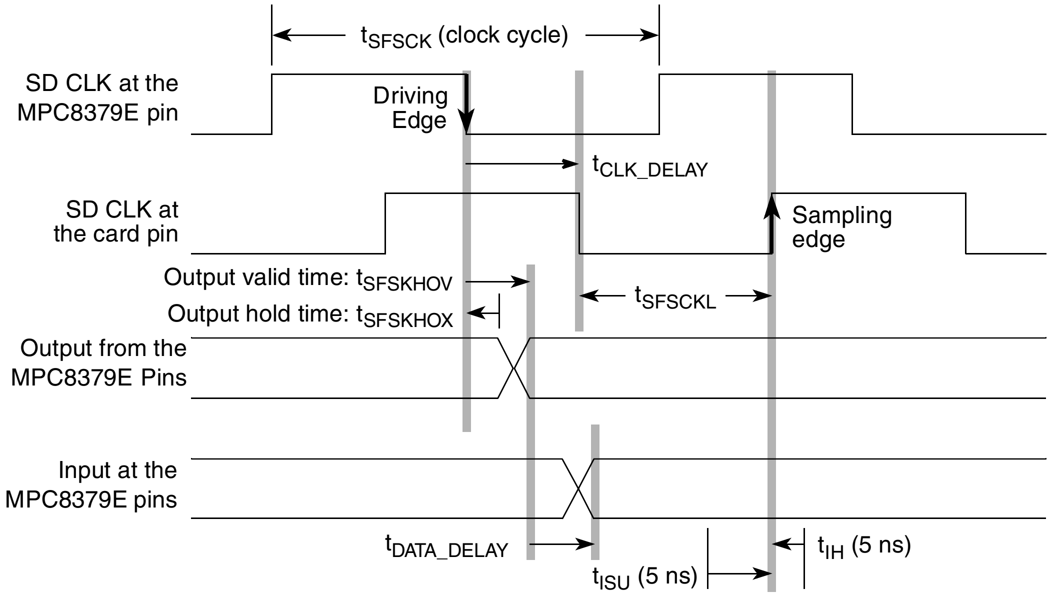


Figure 27. Full Speed Output Path

11.2.1.1 Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} \qquad \text{Eqn. 1}$$

With clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} + t_{CLK\_DELAY} \qquad \text{Eqn. 2}$$

$$t_{DATA\_DELAY} + t_{SFSCKL} < t_{SFSCK} + t_{CLK\_DELAY} - t_{ISU} - t_{SFSKHOV} \qquad \text{Eqn. 3}$$

This means that data can be delayed versus clock up to 11 ns in ideal case of t_{SFSCKL} = 20 ns:

$t_{DATA\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 4$

$t_{DATA\_DELAY} < 11 + t_{CLK\_DELAY}$

11.2.1.2 Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} < t_{SFSCKL} + t_{SFSKHOX} + t_{DATA\_DELAY} - t_{IH} \qquad \text{Eqn. 4}$$

This figure provides the boundary-scan timing diagram.

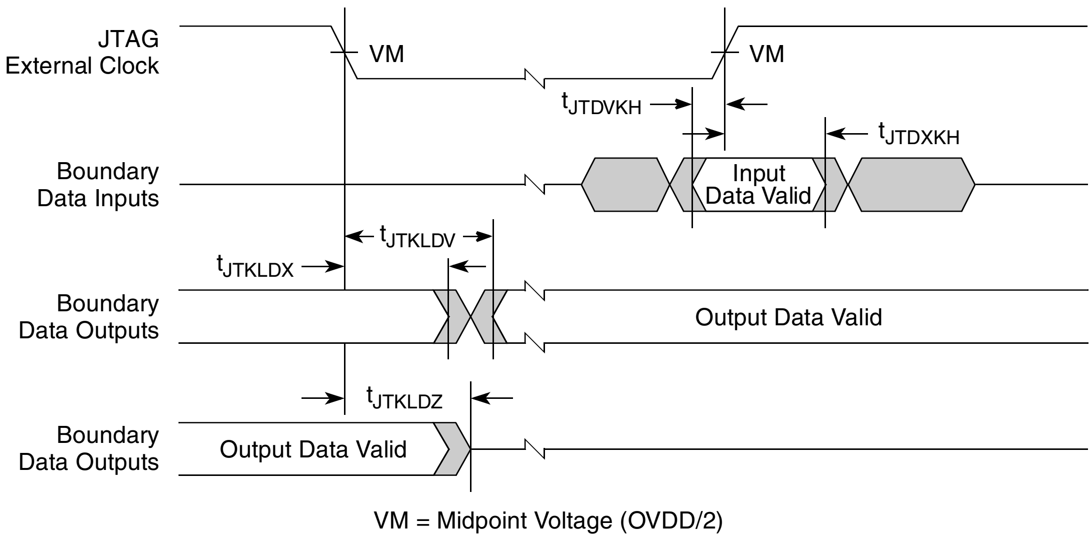


Figure 35. Boundary-Scan Timing Diagram

This figure provides the test access port timing diagram.

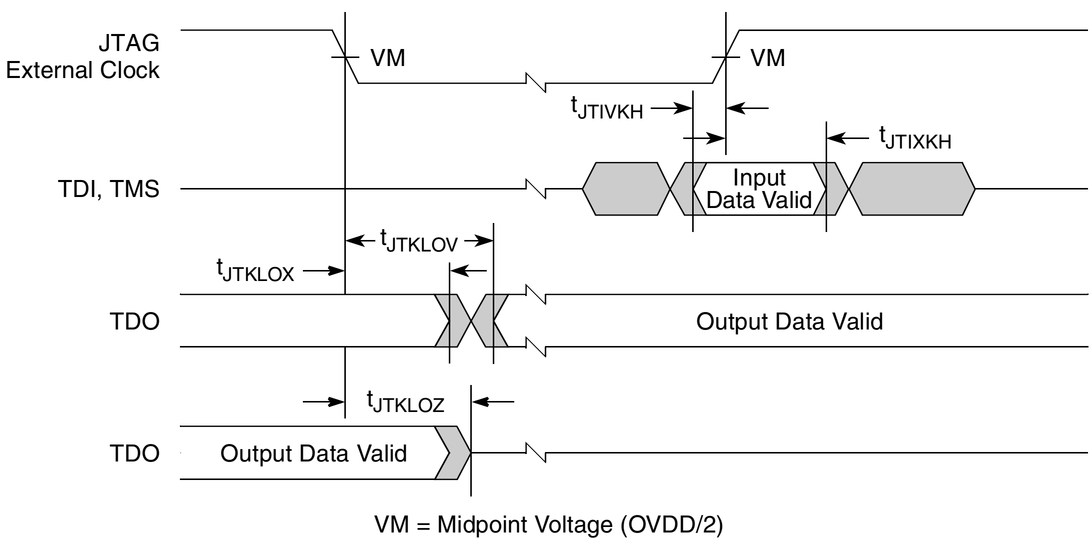


Figure 36. Test Access Port Timing Diagram

This figure provides the AC test load for PCI.

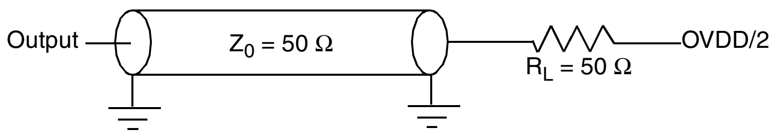


Figure 39. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

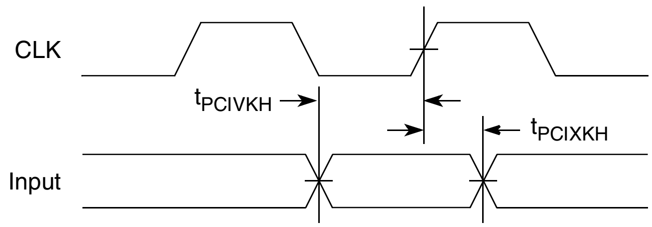


Figure 40. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

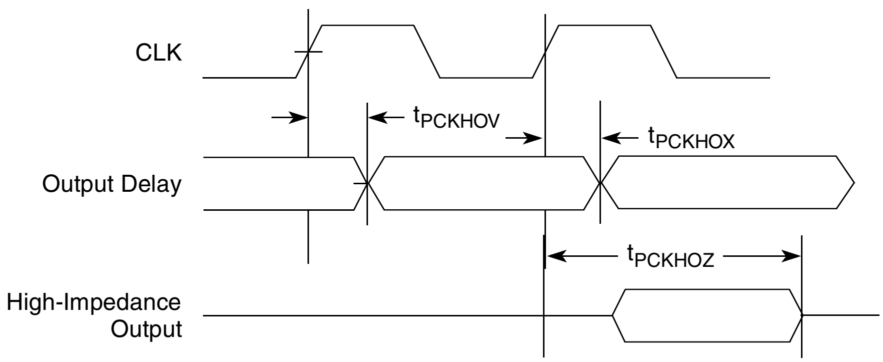


Figure 41. PCI Output AC Timing Measurement Condition

15 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the MPC8379E. Note that the external cabled applications or long backplane applications (Gen1x and Gen2x) are not supported.

occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SATAprotocols

Table 68. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS} or XV_{DD_SRDS} = 1.0 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SD*n*_REF_CLK) to falling edge rate ($\overline{\mathrm{SD}n\_\mathrm{REF}\_\mathrm{CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:
1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\mathrm{SD}n\_\mathrm{REF}\_\mathrm{CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 57.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\mathrm{SD}n\_\mathrm{REF}\_\mathrm{CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\mathrm{SD}n\_\mathrm{REF}\_\mathrm{CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD*n*_REF_CLK should be compared to the Fall Edge Rate of $\overline{\mathrm{SD}n\_\mathrm{REF}\_\mathrm{CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 58.

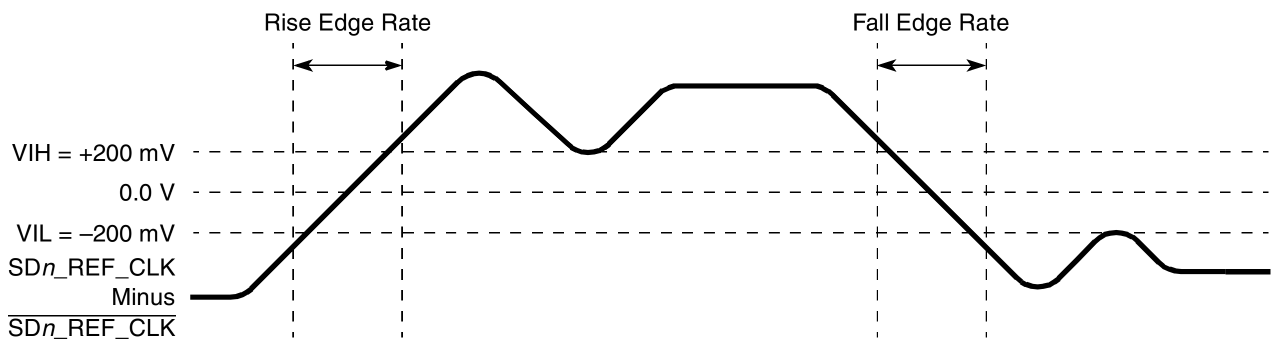


Figure 57. Differential Measurement Points for Rise and Fall Time

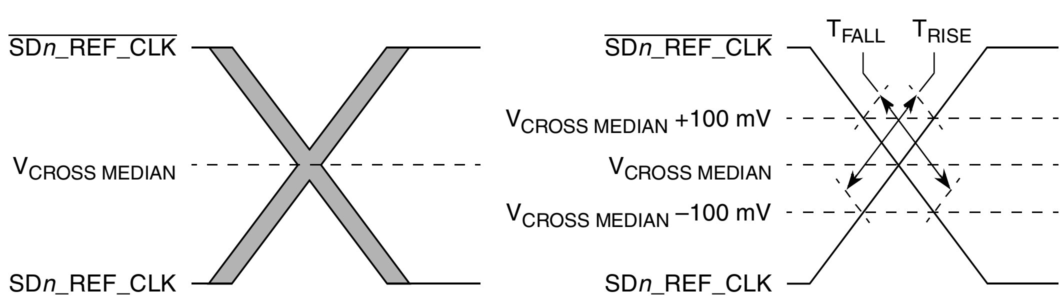


Figure 58. Single-Ended Measurement Points for Rise and Fall Time Matching

Table 69. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQ35	AE1	I/O	GVDD	11
MDQ36	V6	I/O	GVDD	11
MDQ37	Y5	I/O	GVDD	11
MDQ38	AA4	I/O	GVDD	11
MDQ39	AB6	I/O	GVDD	11
MDQ40	AD3	I/O	GVDD	11
MDQ41	AC4	I/O	GVDD	11
MDQ42	AD4	I/O	GVDD	11
MDQ43	AF1	I/O	GVDD	11
MDQ44	AE4	I/O	GVDD	11
MDQ45	AC5	I/O	GVDD	11
MDQ46	AE2	I/O	GVDD	11
MDQ47	AE3	I/O	GVDD	11
MDQ48	AG1	I/O	GVDD	11
MDQ49	AG2	I/O	GVDD	11
MDQ50	AG3	I/O	GVDD	11
MDQ51	AF5	I/O	GVDD	11
MDQ52	AE5	I/O	GVDD	11
MDQ53	AD7	I/O	GVDD	11
MDQ54	AH2	I/O	GVDD	11
MDQ55	AG4	I/O	GVDD	11
MDQ56	AH3	I/O	GVDD	11
MDQ57	AG5	I/O	GVDD	11
MDQ58	AF8	I/O	GVDD	11
MDQ59	AJ5	I/O	GVDD	11
MDQ60	AF6	I/O	GVDD	11
MDQ61	AF7	I/O	GVDD	11
MDQ62	AH6	I/O	GVDD	11
MDQ63	AH7	I/O	GVDD	11
MDQS0	C8	I/O	GVDD	11
MDQS1	C4	I/O	GVDD	11
MDQS2	E3	I/O	GVDD	11
MDQS3	G2	I/O	GVDD	11

Table 69. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC2_RXD0/GPIO1[16]	AE28	I/O	LVDD2	17
TSEC2_RXD1/GPIO1[15]	AE29	I/O	LVDD2	17
TSEC2_RXD2/GPIO1[14]	AH26	I/O	LVDD2	17
TSEC2_RXD3/GPIO1[13]	AH25	I/O	LVDD2	17
TSEC2_TX_CLK/GPIO2[24]/ TSEC1_TMR_GCLK	AG28	I/O	LVDD2	17
TSEC2_TX_EN/GPIO1[12]/ TSEC1_TMR_ALARM2	AJ26	I/O	LVDD2	17
TSEC2_TX_ER/GPIO1[24]/ TSEC1_TMR_ALARM1	AG26	I/O	LVDD2	17
TSEC2_TXD0/GPIO1[20]	AH28	I/O	LVDD2	17
TSEC2_TXD1/GPIO1[19]/ TSEC1_TMR_PP1	AF27	I/O	LVDD2	17
TSEC2_TXD2/GPIO1[18]/ TSEC1_TMR_PP2	AJ28	I/O	LVDD2	17
TSEC2_TXD3/GPIO1[17]/ TSEC1_TMR_PP3	AF29	I/O	LVDD2	17
GPIO1 Interface				
GPIO1[0]/GTM1_TIN1/ GTM2_TIN2/DREQ0_B	P25	I/O	OVDD	—
GPIO1[1]/GTM1_TGATE1_B/ GTM2_TGATE2_B/DACK0_B	N25	I/O	OVDD	—
GPIO1[2]/GTM1_TOUT1_B/ DDONE0_B	N26	I/O	OVDD	—
GPIO1[3]/GTM1_TIN2/ GTM2_TIN1/DREQ1_B	B9	I/O	OVDD	—
GPIO1[4]/GTM1_TGATE2_B/ GTM2_TGATE1_B/DACK1_B	N29	I/O	OVDD	—
GPIO1[5]/GTM1_TOUT2_B/ GTM2_TOUT1_B/DDONE1_B	M29	I/O	OVDD	—
GPIO1[6]/GTM1_TIN3/ GTM2_TIN4/DREQ2_B	A9	I/O	OVDD	—
GPIO1[7]/GTM1_TGATE3_B/ GTM2_TGATE4_B/DACK2_B	B10	I/O	OVDD	—
GPIO1[8]/GTM1_TOUT3_B/ DDONE2_B	J26	I/O	OVDD	—
GPIO1[9]/GTM1_TIN4/ GTM2_TIN3/DREQ3_B	J24	I/O	OVDD	—

Table 69. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
Programmable Interrupt Controller (PIC) Interface				
MCP_OUT_B	AD14	O	OVDD	2
IRQ_B0/MCP_IN_B/GPIO2[12]	F9	I/O	OVDD	—
IRQ_B1/GPIO2[13]	E9	I/O	OVDD	—
IRQ_B2/GPIO2[14]	F10	I/O	OVDD	—
IRQ_B3/GPIO2[15]	D9	I/O	OVDD	—
IRQ_B4/GPIO2[16]/SD_WP	C9	I/O	OVDD	—
IRQ_B5/GPIO2[17]/ USBDR_PWRFAULT	AE10	I/O	OVDD	—
IRQ_B6/GPIO2[18]	AD10	I/O	OVDD	—
IRQ_B7/GPIO2[19]	AD9	I/O	OVDD	—
PMC Interface				
QUIESCE_B	D13	O	OVDD	—
SerDes1 Interface				
L1_SD_IMP_CAL_RX	AJ14	I	L1_XPADVDD	—
L1_SD_IMP_CAL_TX	AG19	I	L1_XPADVDD	—
L1_SD_REF_CLK	AJ17	I	L1_XPADVDD	—
L1_SD_REF_CLK_B	AH17	I	L1_XPADVDD	—
L1_SD_RXA_N	AJ15	I	L1_XPADVDD	—
L1_SD_RXA_P	AH15	I	L1_XPADVDD	—
L1_SD_RXE_N	AJ19	I	L1_XPADVDD	—
L1_SD_RXE_P	AH19	I	L1_XPADVDD	—
L1_SD_TXA_N	AF15	O	L1_XPADVDD	—
L1_SD_TXA_P	AE15	O	L1_XPADVDD	—
L1_SD_TXE_N	AF18	O	L1_XPADVDD	—
L1_SD_TXE_P	AE18	O	L1_XPADVDD	—
L1_SDAVDD_0	AJ18	SerDes PLL Power (1.0 or 1.05 V)	—	—
L1_SDAVSS_0	AG17	SerDes PLL GND	—	—
L1_XCOREVDD	AH14, AJ16, AF17, AH20, AJ20	SerDes Core Power (1.0 or 1.05 V)	—	—

As shown in Figure 61, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{PCI\_SYNC\_IN \times (1 + CFG\_CLKIN\_DIV)\} \times SPMF \quad \text{Eqn. 20}$$

In PCI host mode, PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low register (RCWLR) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, "Reset, Clocking, and Initialization," in the *MPC8379E Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + RCWLR[DDRCM]) \quad \text{Eqn. 21}$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + RCWLR[LBCM]) \quad \text{Eqn. 22}$$

Note that *lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LCLK[0:2]). The eLBC clock divider ratio is controlled by LCRR[CLKDIV].

Some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 70 specifies which units have a configurable clock frequency.

Table 70. Configurable Clock Units

Unit	Default Frequency	Options
eTSEC1, eTSEC2	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
eSDHC and I^2C1[1]	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
Security block	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
USB DR	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
PCI and DMA complex	csb_clk	Off, *csb_clk*
SATA1, 2, 3, 4	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*

[1] This only applies to I^2C1 (I^2C2 clock is not configurable).

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JB} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JB}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

23.2.3 Experimental Determination of Junction Temperature

NOTE

The heat sink cannot be mounted on the package.

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

For the power values the device is expected to operate at, it is anticipated that a heat sink will be required. A preliminary estimate of heat sink performance can be obtained from the following first-cut approach.

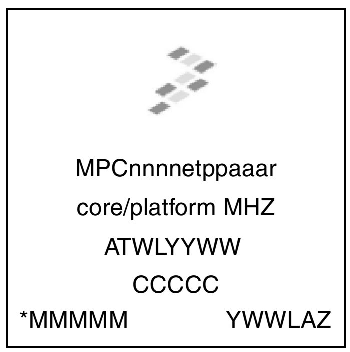
This table shows the SVR and PVR settings by device.

Table 83. SVR and PVR Settings by Product Revision

Device	Package	SVR		PVR	
		Rev 1.0	Rev. 2.1	Rev. 1.0	Rev. 2.1
MPC8377	TePBGA II	0x80C7_0010	0x80C7_0021	0x8086_1010	0x8086_1011
MPC8377E		0x80C6_0010	0x80C6_0021		
MPC8378		0x80C5_0010	0x80C5_0021		
MPC8378E		0x80C4_0010	0x80C4_0021		
MPC8379		0x80C3_0010	0x80C3_0021		
MPC8379E		0x80C2_0010	0x80C2_0021		

25.2 Part Marking

Parts are marked as in the example as shown in this figure.



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Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 64. Freescale Part Marking for TePBGA II Devices

26 Document Revision History

This table provides a revision history for this document.

Table 84. Document Revision History

Revision	Date	Substantive Change(s)
8	05/2012	In Table 15, “DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V,” updated Output leakage current (I_{OZ}) min and max values.
7	10/2011	• In Table 81, “Part Numbering Nomenclature,” updated “Revision Level description”and added footnote 4.
6	07/2011	In Section 2.2, “Power Sequencing,” updated power down sequencing information.

Table 84. Document Revision History (continued)

Revision	Date	Substantive Change(s)
5	07/2011	• In Table 2, "Absolute Maximum Ratings[1]," removed footnote 5 from LB_{IN} to OV_{IN}. Also, corrected footnote 5. • In Table 3, "Recommended Operating Conditions," added footnote 2 to AV_{DD}. • In Figure 2, "Overshoot/Undershoot Voltage for GV_{DD}/LV_{DD}/OV_{DD}/LBV_{DD}," added LBV_{DD}. • In Table 13, "DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V," updated I_{OZ} min/max to –50/50. • In Figure 11, "RGMII and RTBI AC Timing and Multiplexing Diagrams," added distinction between t_{SKRGT_RX} and t_{SKRGT_TX} signals. • In Table 33, "MII Management AC Timing Specifications," updated MDC frequency—removed Min and Max values, added Typical value. Also, updated footnote 2 and removed footnote 3. • In Table 48, "PCI DC Electrical Characteristics," updated V_{IH} min value to 2.0. • In Table 69, "TePBGA II Pinout Listing," added Note to LGPL4/LFRB_B/LGTA_B/LUPWAIT/LPBSE (to be consistent with AN3665, "MPC837xE Design Checklist." • In Table 71, "Operating Frequencies for TePBGA II," added Minimum Operating Frequency for eTSEC, and corrected DDR2 Minimum and Maximum Operating Frequency values.
4	11/2010	• In Table 25, "RGMII and RTBI DC Electrical Characteristics," updated V_{IH} min value to 1.7. • In Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," added row for t_{LBKHLR}. • In Section 10.2, "Local Bus AC Electrical Specifications," and in Section 22, "Clocking," updated LCCR to LCRR. • In Table 69, "TePBGA II Pinout Listing," added SD_WP to pin C9. Also clarified TEST_SEL0 and TEST_SEL1 pins—no change in functionality.
3	03/2010	• Added Section 4.3, "eTSEC Gigabit Reference Clock Timing." • In Table 34, "USB DC Electrical Characteristics," and Table 35, "USB General Timing Parameters (ULPI Mode Only)," added table footnotes . • In Table 39, "Local Bus General Timing Parameters—PLL Enable Mode," and Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," corrected footnotes for $t_{LBOTOT1}$, $t_{LBOTOT2}$, $t_{LBOTOT3}$. • In Figure 22, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Enable Mode)," and Figure 24, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Enable Mode)," shifted "Input Signals: LAD[0:31]/LDP[0:3]" from the falling edge to the rising edge of LSYNC_IN. • In Figure 60, "Mechanical Dimensions and Bottom Surface Nomenclature of the TEPBGA II," added heat spreader. • In Section 24.6, "Pull-Up Resistor Requirements," removed "Ethernet Management MDIO pin" from list of open drain type pins. • In Table 69, "TePBGA II Pinout Listing," updated the Pin Type column for AVDD_C, AVDD_L, and AVDD_P pins. • in Table 69, "TePBGA II Pinout Listing," added Note 17 to eTSEC pins. • In Table 74, "CSB Frequency Options for Host Mode," and Table 75, "CSB Frequency Options for Agent Mode," updated *csb_clk* frequencies available. • In Table 81, "Part Numbering Nomenclature," removed footnote to "e300 core Frequency."