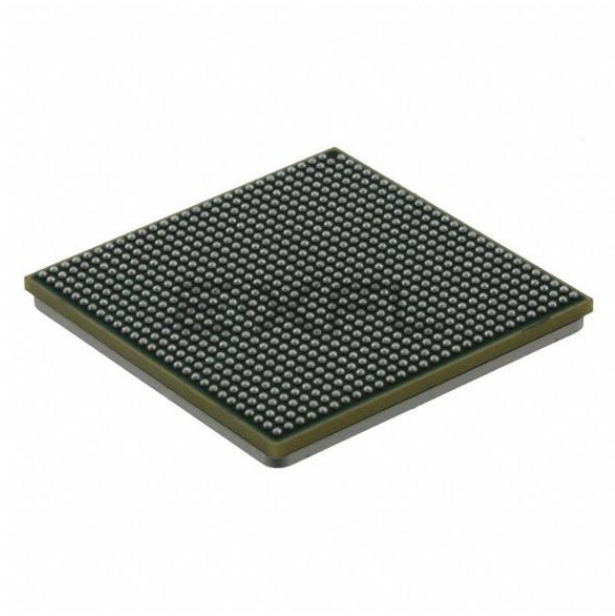

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Six Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8256sag1000b

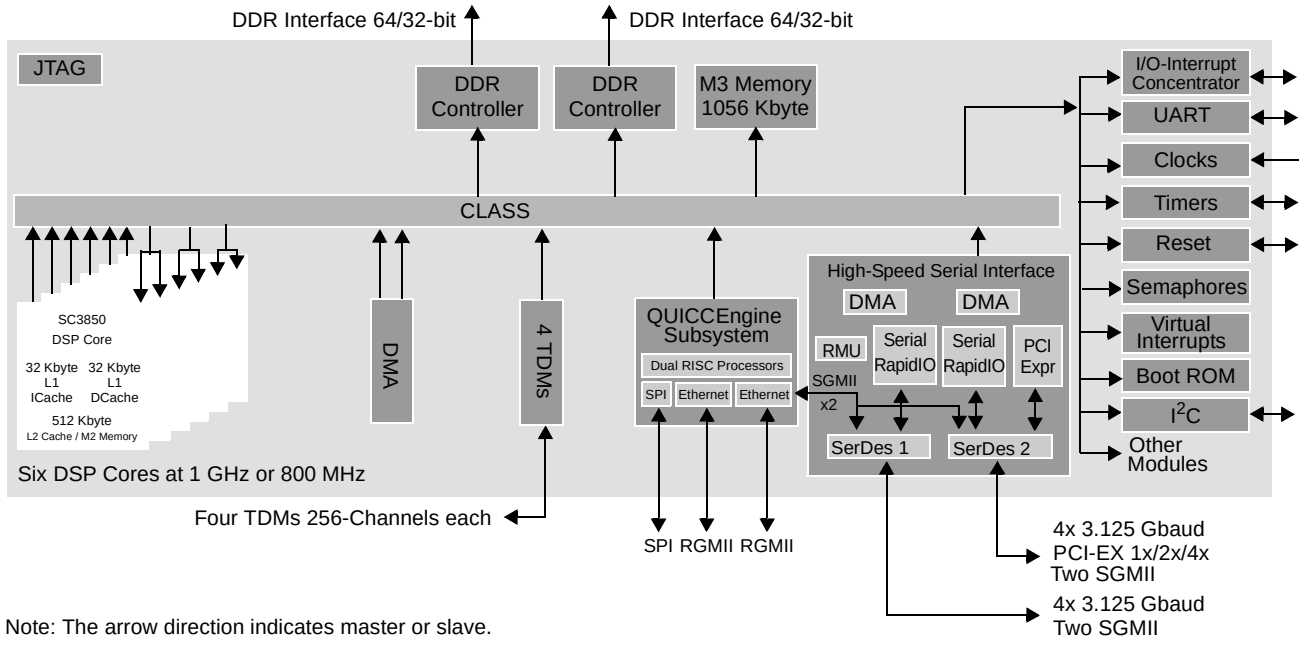


Figure 1. MSC8256 Block Diagram

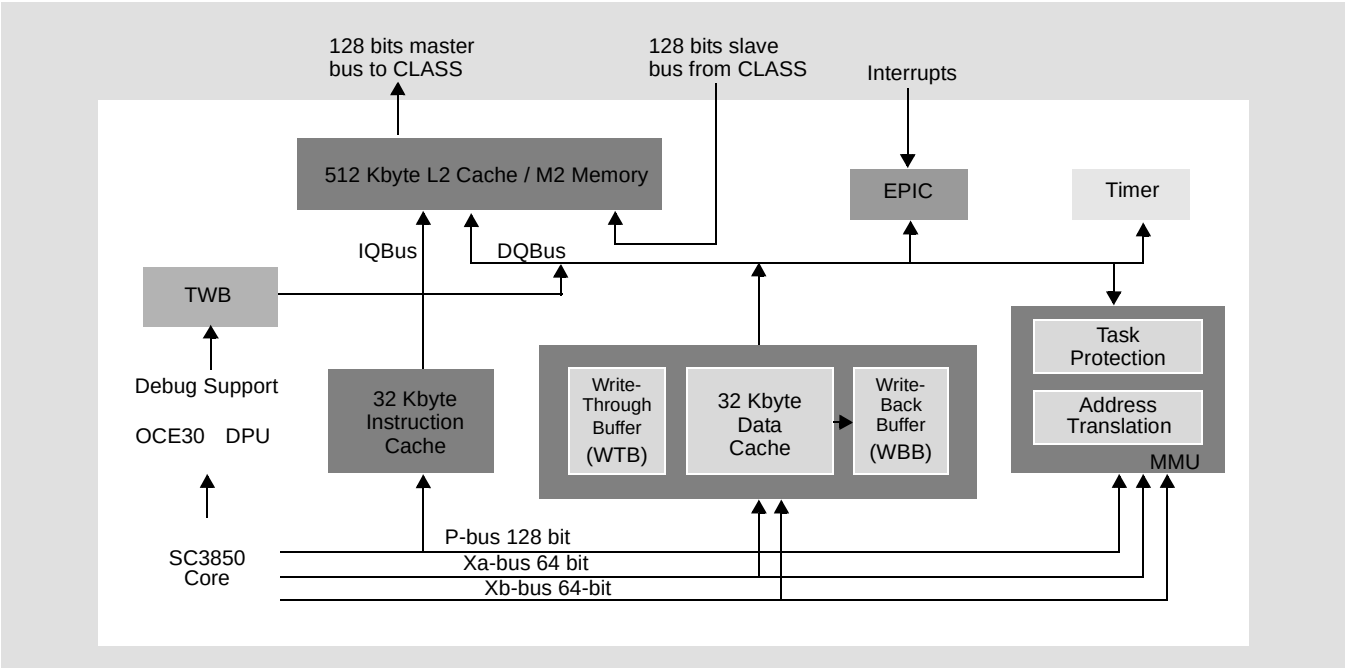


Figure 2. StarCore SC3850 DSP Subsystem Block Diagram

Table 1. Signal List by Ball Number (continued)

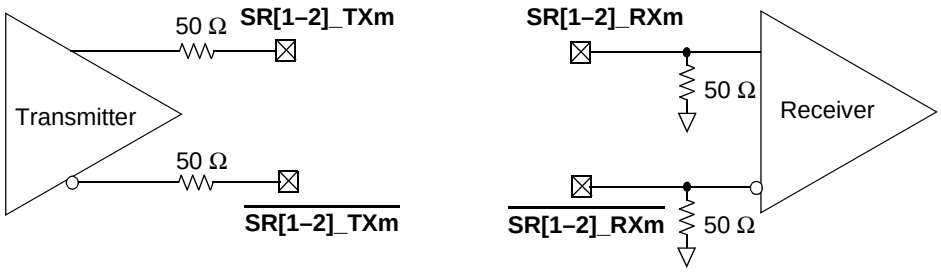
Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
G7	M2CKE0	O	GVDD2
G8	M2A11	O	GVDD2
G9	M2A7	O	GVDD2
G10	$\overline{\text{M2CK2}}$	O	GVDD2
G11	M2APAR_OUT	O	GVDD2
G12	M2ODT1	O	GVDD2
G13	$\overline{\text{M2APAR\_IN}}$	I	GVDD2
G14	M2DQ43	I/O	GVDD2
G15	M2DM5	O	GVDD2
G16	M2DQ44	I/O	GVDD2
G17	M2DQ40	I/O	GVDD2
G18	M2DQ59	I/O	GVDD2
G19	M2DM7	O	GVDD2
G20	M2DQ60	I/O	GVDD2
G21	Reserved	NC	—
G22	Reserved	NC	—
G23	SXPVSS1	Ground	N/A
G24	SXPVDD1	Power	N/A
G25	SR1_IMP_CAL_TX	I	SXCVDD1
G26	SXCVSS1	Ground	N/A
G27	Reserved	NC	—
G28	Reserved	NC	—
H1	GVDD2	Power	N/A
H2	VSS	Ground	N/A
H3	M2DQ18	I/O	GVDD2
H4	GVDD2	Power	N/A
H5	VSS	Ground	N/A
H6	M2DQ20	I/O	GVDD2
H7	GVDD2	Power	N/A
H8	VSS	Ground	N/A
H9	M2A15	O	GVDD2
H10	M2CK2	O	GVDD2
H11	M2MDIC0	I/O	GVDD2
H12	M2VREF	I	GVDD2
H13	M2MDIC1	I/O	GVDD2
H14	M2DQ46	I/O	GVDD2
H15	M2DQ47	I/O	GVDD2
H16	M2DQ45	I/O	GVDD2
H17	M2DQ41	I/O	GVDD2
H18	M2DQ62	I/O	GVDD2
H19	M2DQ63	I/O	GVDD2
H20	M2DQ61	I/O	GVDD2
H21	Reserved	NC	—
H22	Reserved	NC	—
H23	SR1_TXD3/SG2_TX[4]	O	SXPVDD1
H24	$\overline{\text{SR1\_TXD3}}$/$\overline{\text{SG2\_TX}}$[4]	O	SXPVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N24	$\overline{\text{SR2\_TXD2}}$/$\overline{\text{PE\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	$\overline{\text{SR2\_RXD2}}$/$\overline{\text{PE\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD2
N28	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD[9]	Power	VDD
P9	PLL2_AVDD[9]	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	VSS	Ground	N/A
P16	VSS	Ground	N/A
P17	VSS	Ground	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND[9]	Ground	SXCVSS2
P26	SR2_PLL_AVDD[9]	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	$\overline{\text{NMI}}$	I	QVDD
R3	$\overline{\text{NMI\_OUT}}$[6]	O	QVDD
R4	$\overline{\text{HRESET}}$[6,7]	I/O	QVDD
R5	$\overline{\text{INT\_OUT}}$[6]	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD[9]	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

2.5.2.3 SerDes Transmitter and Receiver Reference Circuits

Figure 6 shows the reference circuits for SerDes data lane transmitter and receiver.



Note: The [1–2] indicates the specific SerDes Interface (1 or 2) and the m indicates the specific channel within that interface (0,1,2,3). Actual signals are assigned by the HRCW assignments at reset (see **Chapter 5**, *Reset* in the reference manual for details)

Figure 6. SerDes Transmitter and Receiver Reference Circuits

2.5.3 DC-Level Requirements for SerDes Interfaces

The following subsections define the DC-level requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.5.3.1 DC-Level Requirements for SerDes Reference Clocks

The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 7 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

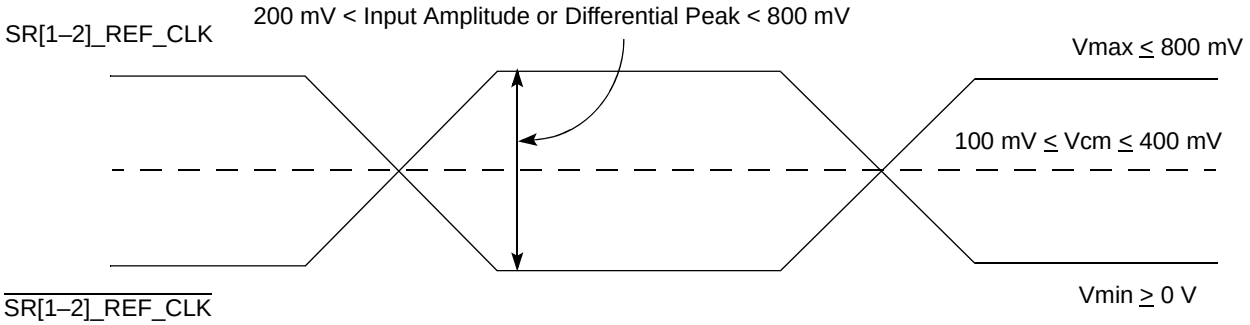


Figure 7. Differential Reference Clock Input DC Requirements (External DC-Coupled)

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC-level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to GND_{SXC}. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage GND_{SXC}. Figure 8 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

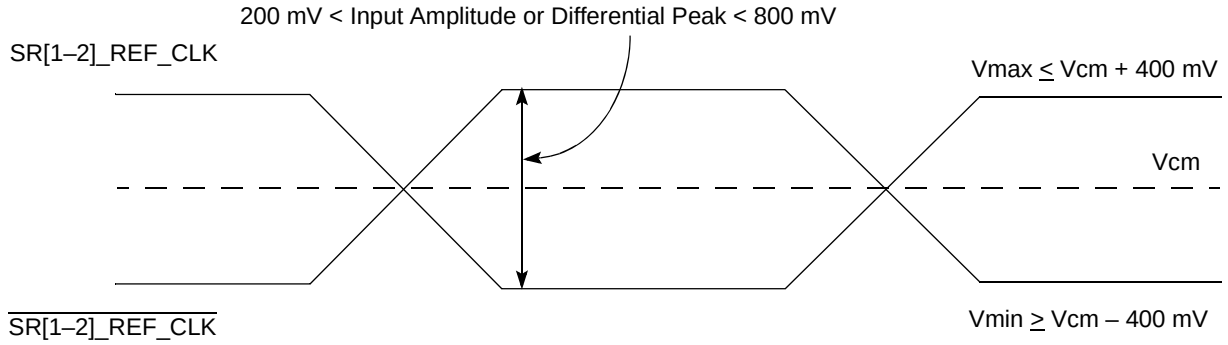


Figure 8. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  — The reference clock can also be single-ended. The SR[1–2]_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SR[1–2]\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SR[1–2]_REF_CLK input average voltage must be between 200 and 400 mV. Figure 9 shows the SerDes reference clock input requirement for single-ended signalling mode.
  — To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SR[1–2]\_REF\_CLK}}$) through the same source impedance as the clock input (SR[1–2]_REF_CLK) in use.

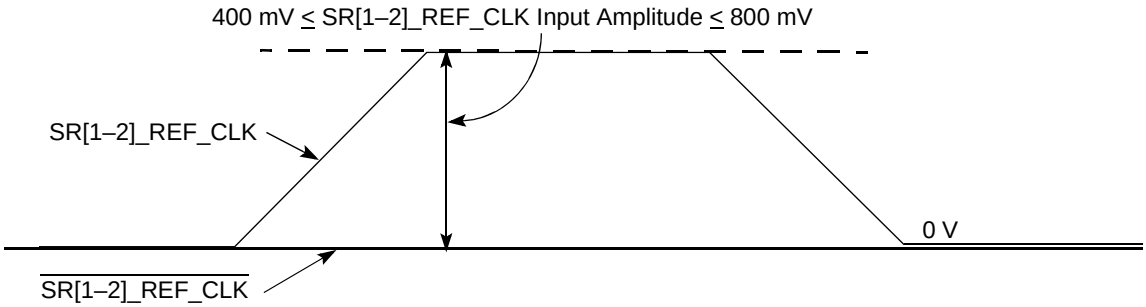


Figure 9. Single-Ended Reference Clock Input DC Requirements

2.5.3.2 DC-Level Requirements for PCI Express Configurations

The DC-level requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8256 supports a 2.5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 1.0a*. The transmitter specifications are defined in Table 11 and the receiver specifications are defined in Table 12.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 11. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	1
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	2
DC differential Tx impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	3
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	4

Notes:
1. $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{TX\text{-}D+} - V_{TX\text{-}D\text{-}}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. Measured at the package pins with a test load of 50 Ω to GND on each pin.
3. Tx DC differential mode low impedance
4. Required Tx D+ as well as D– DC Impedance during all states

Table 12. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX\text{-}DIFFp\text{-}p}$	120	1000	1200	mV	1
DC differential Input Impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	2
DC input impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	3
Powered down DC input impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	—	—	KΩ	4
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	—	175	mV	5

Notes:
1. $V_{RX\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}|$ Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Rx DC differential mode impedance. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
3. Required Rx D+ as well as D– DC Impedance (50 ±20% tolerance). Measured at the package pins with a test load of 50 Ω to GND on each pin. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM), there is a 5 ms transition time before the receiver termination values must be met on all unconfigured lanes of a port.
4. Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
5. $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}|$. Measured at the package pins of the receiver

2.5.3.3 DC-Level Requirements for Serial RapidIO Configurations

This sections provided various DC-level requirements for Serial RapidIO Configurations.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 13. Serial RapidIO Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Long run differential output voltage	V_{DIFFPP}	800	—	1600	mVp-p	—
Short run differential output voltage	V_{DIFFPP}	500	—	1000	mVp-p	—

Note: Voltage relative to COMMON of either signal comprising a differential pair.

2.5.4 RGMII and Other Interface DC Electrical Characteristics

Table 17 describes the DC electrical characteristics for the following interfaces:

- RGMII Ethernet
- SPI
- TDM
- GPIO
- UART
- TIMER
- EE
- I^2C
- Interrupts ($\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$)
- Clock and resets (CLKIN, $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$)
- DMA External Request
- JTAG signals

Table 17. 2.5 V I/O DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input high current ($V_{IN} = V_{DDIO}$)	I_{IN}	—	30	μA	2
Output high voltage (V_{DDIO} = min, I_{OH} = –1.0 mA)	V_{OH}	2.0	VDDIO + 0.3	V	1
Output low voltage (V_{DDIO} = min, I_{OL}= 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	1

Notes: **1.** The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values listed in Table 3.
2. The symbol V_{IN} represents the input voltage of the supply. It is referenced in Table 3.

Table 21. DDR SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MSC8256 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MSC8256.
6. At recommended operating conditions with V_{DDDDR} (1.5 V or 1,8 V) ± 5%.

Note: For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 12 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

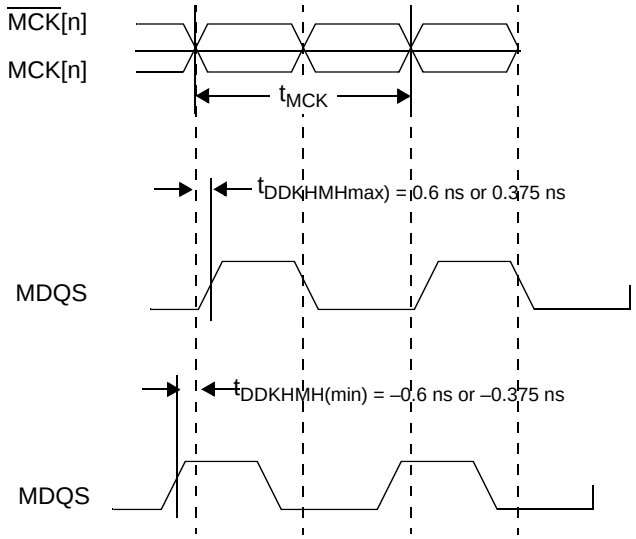


Figure 12. MCK to MDQS Timing

Table 24. SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ Input Clock Requirements (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes

Notes:
1. Caution: Only 100 and 125 have been tested. Other values will not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 1.0a
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SR[1–2]_REF_CLK minus $\overline{\text{SR[1–2]\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 16.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SR[1–2]_REF_CLK and falling edge rate for $\overline{\text{SR[1–2]\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SR[1–2]_REF_CLK rising meets $\overline{\text{SR[1–2]\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SR[1–2]_REF_CLK should be compared to the fall edge rate of $\overline{\text{SR[1–2]\_REF\_CLK}}$; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 17.

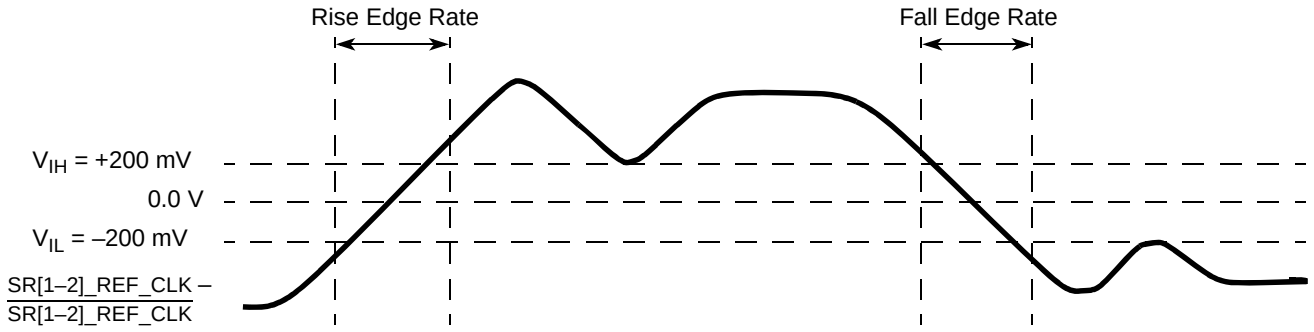


Figure 16. Differential Measurement Points for Rise and Fall Time

Figure 17. Single-Ended Measurement Points for Rise and Fall Time Matching

2.6.2.3 Serial RapidIO AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 27 defines the transmitter AC specifications for the Serial RapidIO interface. The AC timing specifications do not include REF_CLK jitter.

Table 27. Serial RapidIO Transmitter AC Timing Specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Deterministic Jitter	J_D	—	—	0.17	UI p-p
Total Jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps

Table 28 defines the Receiver AC specifications for the Serial RapidIO interface. The AC timing specifications do not include REF_CLK jitter.

Table 28. Serial RapidIO Receiver AC Timing Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	Notes
Deterministic Jitter Tolerance	J_D	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total Jitter Tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit Error Rate	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

Notes:
1. Measured at receiver.
2. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 18. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

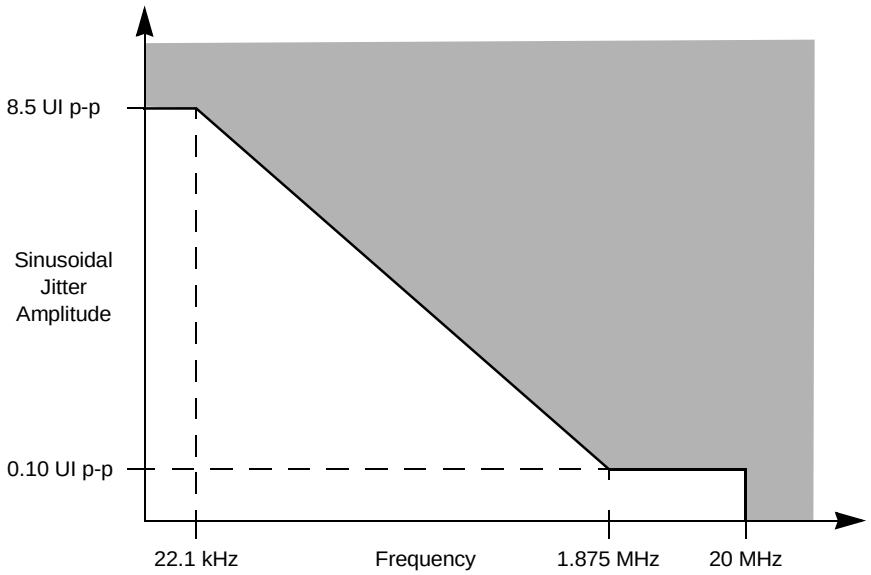


Figure 18. Single Frequency Sinusoidal Jitter Limits

2.6.2.4 SGMII AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SR[1–2]_TX[n] and $\overline{\text{SR[1–2]\_TX}}$[n]) or at the receiver inputs (SR[1–2]_RX[n] and $\overline{\text{SR[1–2]\_RX}}$[n]) as depicted in Figure 19, respectively.

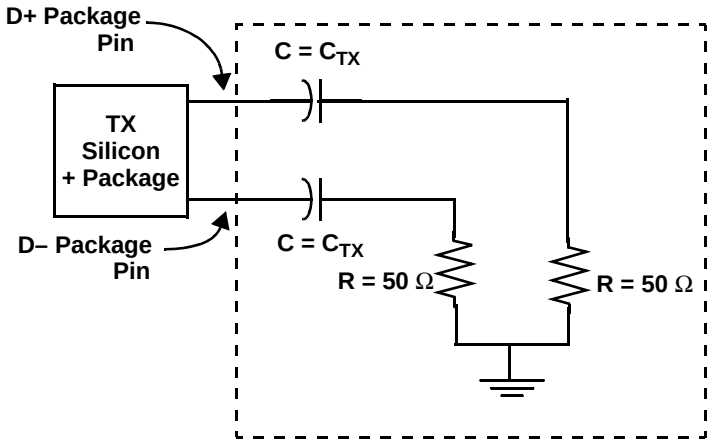


Figure 19. SGMII AC Test/Measurement Load

Table 29 provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include REF_CLK jitter.

Table 29. SGMII Transmit AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	2
Unit Interval	UI	799.92	800	800.08	ps	1

Notes: **1.** See Figure 18 for single frequency sinusoidal jitter limits
2. Each UI is 800 ps ± 100 ppm.

Table 30 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 30. SGMII Receive AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1,2
Bit Error Ratio	BER	—	—	10^{-12}	—	—
Unit Interval	UI	799.92	800.00	800.08	ps	3

Notes: **1.** Measured at receiver.
2. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications. Also see Figure 18.
3. Each UI is 800 ps ± 100 ppm.

2.6.5.2 RGMII AC Timing Specifications

Table 34 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 34. RGMII at 1 Gbps[2] with On-Board Delay[3] AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)[4]	t_{SKEWT}	–-0.5	—	0.5	ns
Data to clock input skew (at receiver) [4]	t_{SKEWR}	1	—	2.6	ns

Notes:
1. At recommended operating conditions with V_{DDIO} of 2.5 V ± 5%.
2. RGMII at 100 Mbps support is guaranteed by design.
3. Program GCR4 as 0x00000000.
4. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.

Table 35 presents the RGMII AC timing specification for applications required non-delayed clock on board.

Table 35. RGMII at 1 Gbps[2] with No On-Board Delay[3] AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)[4]	t_{SKEWT}	–2.6	—	–1.0	ns
Data to clock input skew (at receiver)[4]	t_{SKEWR}	–0.5	—	0.5	ns

Notes:
1. At recommended operating conditions with V_{DDIO} of 2.5 V ± 5%.
2. RGMII at 100 Mbps support is guaranteed by design.
3. GCR4 should be programmed as 0x000CC330.
4. This implies that PC board design requires clocks to be routed with no additional trace delay

Figure 25 shows the RGMII AC timing and multiplexing diagrams.

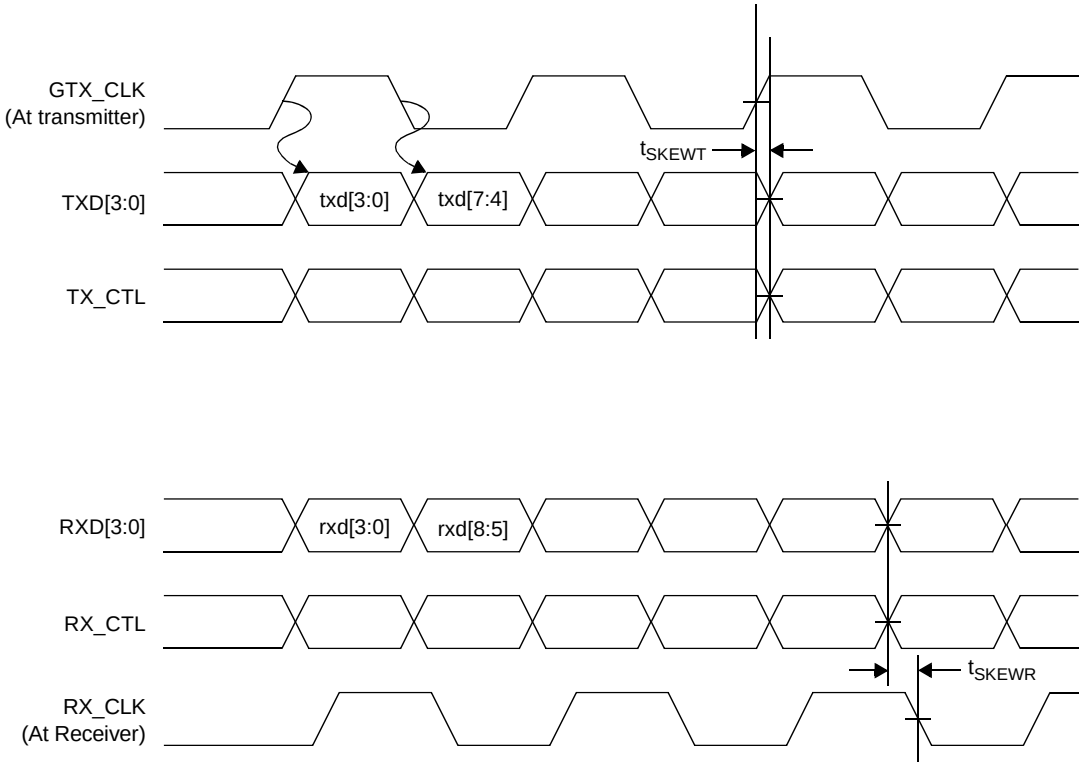


Figure 25. RGMII AC Timing and Multiplexing

Figure 30 shows the boundary scan (JTAG) timing diagram.

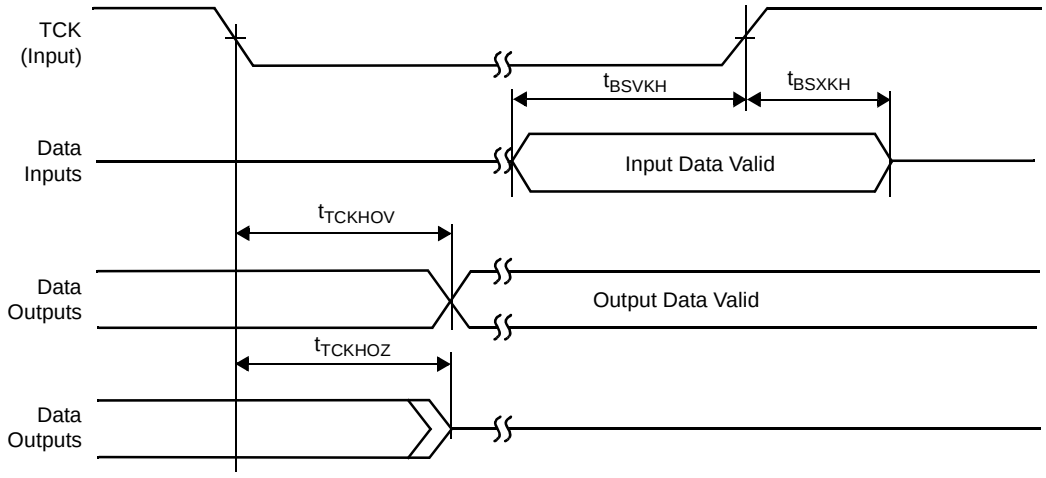


Figure 30. Boundary Scan (JTAG) Timing

Figure 31 shows the test access port timing diagram

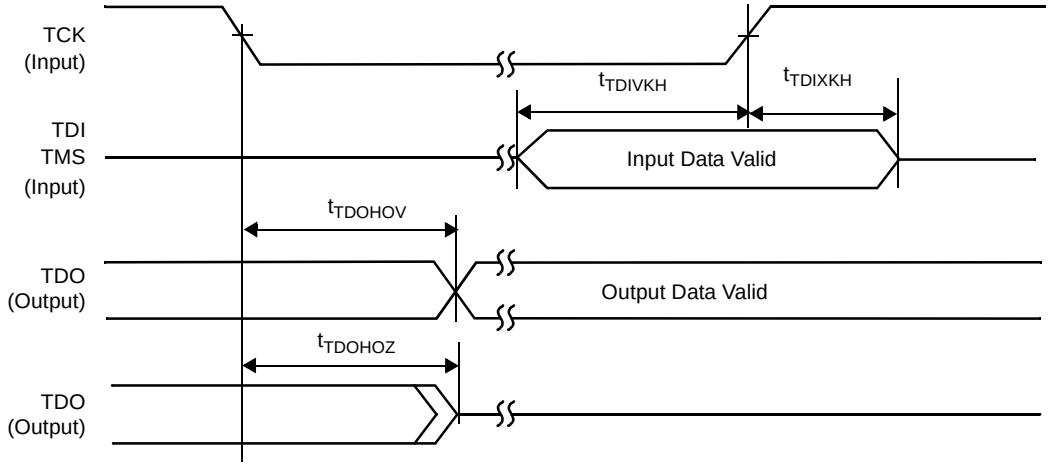


Figure 31. Test Access Port Timing

Figure 32 shows the $\overline{\text{TRST}}$ timing diagram.

Figure 32. $\overline{\text{TRST}}$ Timing

2. After the above rails rise to 90% of their nominal voltage, the following I/O power rails may rise in any sequence (see Figure 34): QVDD, NVDD, GVDD1, and GVDD2.

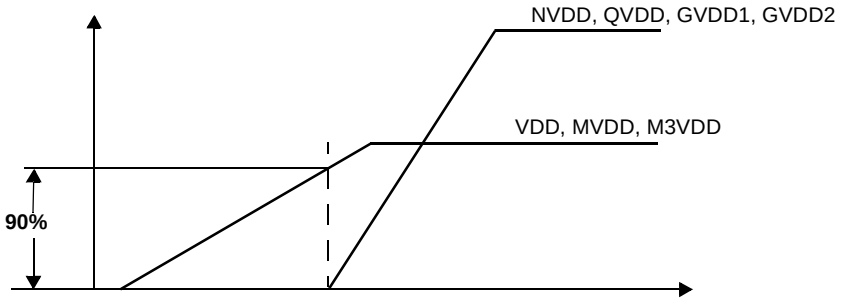


Figure 34. Supply Ramp-Up Sequence

Notes: **1.** If the M3 memory is not used, M3VDD can be tied to GND.
2. If the HSSI port1 is not used, SXCVDD1and SXPVDD1 must be connected to the designated power supplies.
3. If the HSSI port2 is not used, SXCVDD2 and SXPVDD2 must be connected to the designated power supplies.
4. If the DDR port 1 interface is not used, it is recommended that GVDD1 be left unconnected.
5. If the DDR port 2 interface is not used, it is recommended that GVDD2 be left unconnected.

3.1.4 Reset Guidelines

When a debugger is not used, implement the connection scheme shown in Figure 35.

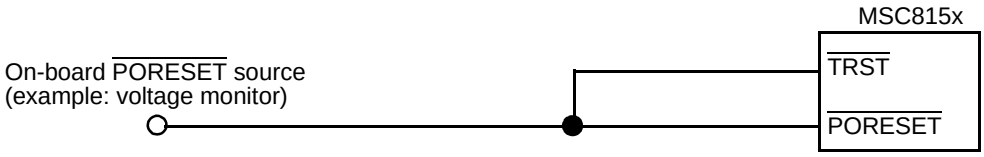


Figure 35. Reset Connection in Functional Application

When a debugger is used, implement the connection scheme shown in Figure 36.

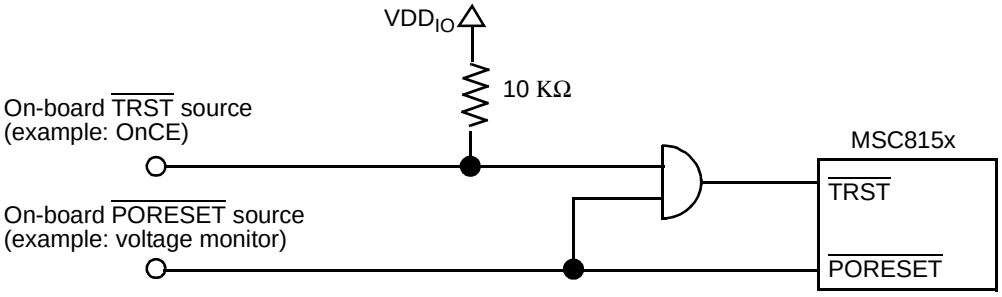


Figure 36. Reset Connection in Debugger Application

3.5 Connectivity Guidelines

Note: Although the package actually uses a ball grid array, the more conventional term pin is used to denote signal connections in this discussion.

First, select the pin multiplexing mode to allocate the required I/O signals. Then use the guidelines presented in the following subsections for board design and connections. The following conventions are used in describing the connectivity requirements:

1. GND indicates using a 10 kΩ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
2. V_{DD} indicates using a 10 kΩ pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
3. Mandatory use of a pull-up or pull-down resistor is clearly indicated as “pull-up/pull-down.” For buses, each pin on the bus should have its own resistor.
4. NC indicates “not connected” and means do not connect anything to the pin.
5. The phrase “in use” indicates a typical pin connection for the required function.

Note: Please see recommendations #1 and #2 as mandatory pull-down or pull-up connection for unused pins in case of subset interface connection.

3.5.1 DDR Memory Related Pins

This section discusses the various scenarios that can be used with either of the MSC8256 DDR ports.

Note: The signal names in Table 40, Table 41 and Table 42 are generic names for a DDR SDRAM interface. For actual pin names refer to Table 1.

3.5.1.1 DDR Interface Is Not Used

Table 40. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Signal Name	Pin Connection
MDQ[0–63]	NC
MDQS[7–0]	NC
$\overline{\text{MDQS[7–0]}}$	NC
MA[15–0]	NC
MCK[0–2]	NC
$\overline{\text{MCK[0–2]}}$	NC
$\overline{\text{MCS[1–0]}}$	NC
MDM[7–0]	NC
MBA[2–0]	NC
$\overline{\text{MCAS}}$	NC
MCKE[1–0]	NC
MODT[1–0]	NC
MMDIC[1–0]	NC
$\overline{\text{MRAS}}$	NC
$\overline{\text{MWE}}$	NC
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS8}}$	NC
MAPAR_OUT	NC
$\overline{\text{MAPAR\_IN}}$	NC
MVREF[3]	NC
GVDD1/GVDD2[3]	NC

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. If the DDR controller is not used, disable the internal DDR clock by setting the appropriate bit in the System Clock Control Register (SCCR) and put all DDR I/O in sleep mode by setting DRx_GCR[DDRx_DOZE] (for DDR controller x). See the *Clocks* and *General Configuration Registers* chapters in the ***MSC8256 Reference Manual*** for details.
3. For MSC8256 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8256, connecting these pins to GND increases device power consumption.

3.5.1.2 DDR Interface Is Used With 32-Bit DDR Memory Only

Table 41 lists unused pin connection when using 32-bit DDR memory. The 32 most significant data lines are not used.

Table 41. Connectivity of DDR Related Pins When Using 32-bit DDR Memory Only

Signal Name	Pin Connection
MDQ[31–0]	in use
MDQ[63–32]	NC
MDQS[3–0]	in use
MDQS[7–4]	NC
$\overline{\text{MDQS[3–0]}}$	in use
$\overline{\text{MDQS[7–4]}}$	NC
MA[15–0]	in use
MCK[2–0]	in use
$\overline{\text{MCK[2–0]}}$	in use
$\overline{\text{MCS[1–0]}}$	in use
MDM[3–0]	in use
MDM[7–4]	NC
MBA[2–0]	in use
$\overline{\text{MCAS}}$	in use
MCKE[1–0]	in use
MODT[1–0]	in use
MMDIC[1–0]	in use
$\overline{\text{MRAS}}$	in use
$\overline{\text{MWE}}$	in use
MVREF	in use
GVDD1/GVDD2	in use

Notes: **1.** For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. For MSC8256 Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8256, connecting these pins to GND increases device power consumption.

3.5.1.3 ECC Unused Pin Connections

When the error code correction mechanism is not used in any 32- or 64-bit DDR configuration, refer to Table 42 to determine the correct pin connections.

Table 42. Connectivity of Unused ECC Mechanism Pins

Signal Name	Pin connection
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS8}}$	NC

Notes: **1.** For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. For MSC8256 Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8256, connecting these pins to GND increases device power consumption.

Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDM***n***TCLK	GND
TDMnT***x***DAT	GND
TDM***n***TSYN	GND
V_{DDIO}	2.5 V

Notes: **1.** ***x*** = {0, 1, 2,3}
2. In case of subset of TDM interface usage please make sure to disable unused TDM modules. See *TDM* chapter in the ***MSC8256 Reference Manual*** for details.

3.5.5 Miscellaneous Pins

Table 49 lists the board connections for the pins not required by the system design. Table 49 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 49. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[31–0]	NC
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT\_OUT}}$	NC
$\overline{\text{IRQ}}$[15–0]	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$	NC
RC[21–0]	GND
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[4–0]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	See **Section 3.1** for guidelines.
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
DDN[1–0]	See the GPIO connectivity guidelines in this table.
DRQ[1–0]	See the GPIO connectivity guidelines in this table.
$\overline{\text{RCW\_LSEL\_0}}$	GND
$\overline{\text{RCW\_LSEL\_1}}$	GND
$\overline{\text{RCW\_LSEL\_2}}$	GND
$\overline{\text{RCW\_LSEL\_3}}$	GND
V_{DDIO}	2.5 V

Note: For details on configuration, see the *MSC8256 Reference Manual*. For additional information, refer to the *MSC815x and MSC825x DSP Family Design Checklist*.

3.6 Guide to Selecting Connections for Remote Power Supply Sensing

To assure consistency of input power levels, some applications use a practice of connecting the remote sense signal input of an on-board power supply to one of power supply pins of the IC device. The advantage of using this connection is the ability to compensate for the slow components of the IR drop caused by resistive supply current path from on-board power supply to the pins layer on the package. However, because of specific device requirements, not every ball connection can be selected as the remote sense pin. Some of these pins must be connected to the appropriate power supply or ground to ensure correct device functionality. Some connections supply critical power to a specific high usage area of the IC die; using such a connection as a non-supply pin could impact necessary supply current during high current events. The following balls can be used as the board supply remote sense output without degrading the power and ground supply quality:

- *VDD:* W10, T19
- *VSS:* J18, Y10
- *M3VDD:* None

Do not use any other connections for remote sensing. Use of any other connections for this purpose can result in application and device failure.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Spheres	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number
MSC8256	Flip Chip Plastic Ball Grid Array (FC-PBGA)	Lead-free	1.0 V	0° C to 105°C	1000	MSC8256SVT1000B
				–40° C to 105°C	1000	MSC8256TVT1000B
				0° C to 105°C	800	MSC8256SVT800B
				–40° C to 105°C	800	MSC8256TVT800B