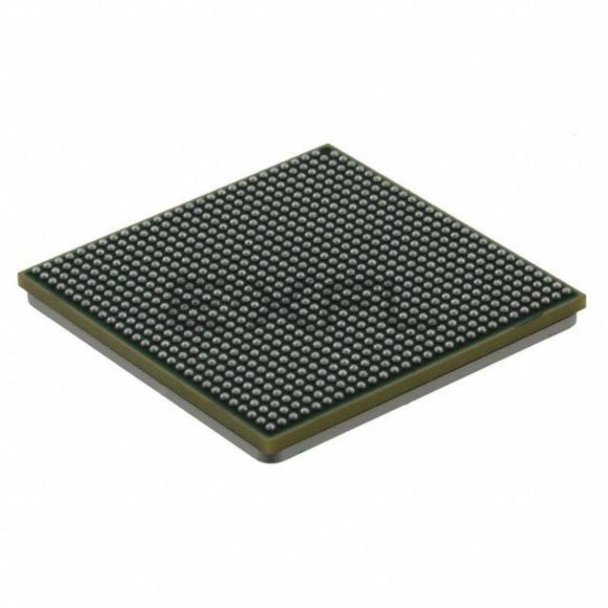

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Six Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	800MHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8256tvt800b

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
E17	M2DQ56	I/O	GVDD2
E18	M2DQ57	I/O	GVDD2
E19	$\overline{\text{M2DQS7}}$	I/O	GVDD2
E20	Reserved	NC	—
E21	Reserved	NC	—
E22	Reserved	NC	—
E23	SXPVDD1	Power	N/A
E24	SXPVSS1	Ground	N/A
E25	SR1_PLL_AGND[9]	Ground	SXCVSS1
E26	SR1_PLL_AVDD[9]	Power	SXCVDD1
E27	SXCVSS1	Ground	N/A
E28	SXCVDD1	Power	N/A
F1	VSS	Ground	N/A
F2	GVDD2	Power	N/A
F3	M2DQ16	I/O	GVDD2
F4	VSS	Ground	N/A
F5	GVDD2	Power	N/A
F6	M2DQ17	I/O	GVDD2
F7	VSS	Ground	N/A
F8	GVDD2	Power	N/A
F9	M2BA2	O	GVDD2
F10	VSS	Ground	N/A
F11	GVDD2	Power	N/A
F12	M2A4	O	GVDD2
F13	VSS	Ground	N/A
F14	GVDD2	Power	N/A
F15	M2DQ42	I/O	GVDD2
F16	VSS	Ground	N/A
F17	GVDD2	Power	N/A
F18	M2DQ58	I/O	GVDD2
F19	M2DQS7	I/O	GVDD2
F20	GVDD2	Power	N/A
F21	SXPVDD1	Power	N/A
F22	SXPVSS1	Ground	N/A
F23	SR1_TXD2/SG1_TX[4]	O	SXPVDD1
F24	$\overline{\text{SR1\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD1
F25	SXCVDD1	Power	N/A
F26	SXCVSS1	Ground	N/A
F27	$\overline{\text{SR1\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD1
F28	SR1_RXD2/SG1_RX[4]	I	SXCVDD1
G1	$\overline{\text{M2DQS2}}$	I/O	GVDD2
G2	M2DQS2	I/O	GVDD2
G3	M2DQ19	I/O	GVDD2
G4	M2DM2	O	GVDD2
G5	M2DQ21	I/O	GVDD2
G6	M2DQ22	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N24	$\overline{\text{SR2\_TXD2}}$/$\overline{\text{PE\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	$\overline{\text{SR2\_RXD2}}$/$\overline{\text{PE\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD2
N28	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD[9]	Power	VDD
P9	PLL2_AVDD[9]	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	VSS	Ground	N/A
P16	VSS	Ground	N/A
P17	VSS	Ground	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND[9]	Ground	SXCVSS2
P26	SR2_PLL_AVDD[9]	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	$\overline{\text{NMI}}$	I	QVDD
R3	$\overline{\text{NMI\_OUT}}$[6]	O	QVDD
R4	$\overline{\text{HRESET}}$[6,7]	I/O	QVDD
R5	$\overline{\text{INT\_OUT}}$[6]	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD[9]	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
V21	$\overline{\text{RCW\_LSEL\_3}}$/RC20	I/O	NVDD
V22	$\overline{\text{RCW\_LSEL\_2}}$/RC19	I/O	NVDD
V23	SXPVDD2	Power	N/A
V24	SXPVSS2	Ground	N/A
V25	$\overline{\text{RCW\_LSEL\_1}}$/RC18	I/O	NVDD
V26	RC21	I	NVDD
V27	SXCVDD2	Power	N/A
V28	SXCVSS2	Ground	N/A
W1	VSS	Ground	N/A
W2	GVDD1	Power	N/A
W3	M1DM1	O	GVDD1
W4	VSS	Ground	N/A
W5	GVDD1	Power	N/A
W6	M1DQ0	I/O	GVDD1
W7	VSS	Ground	N/A
W8	GVDD1	Power	N/A
W9	M1DQ5	I/O	GVDD1
W10	VDD	Power	N/A
W11	VSS	Ground	N/A
W12	VDD	Power	N/A
W13	VSS	Ground	N/A
W14	VDD	Power	N/A
W15	VSS	Ground	N/A
W16	VDD	Power	N/A
W17	VSS	Ground	N/A
W18	VDD	Power	N/A
W19	VSS	Ground	N/A
W20	VSS	Ground	N/A
W21	$\overline{\text{RCW\_LSEL0}}$/RC17	I/O	NVDD
W22	GPIO19/SPI_MISO[5,8]	I/O	NVDD
W23	VSS	Ground	N/A
W24	NVDD	Power	N/A
W25	GPIO11/$\overline{\text{IRQ11}}$/RC11[5,8]	I/O	NVDD
W26	GPIO3/DRQ1/$\overline{\text{IRQ3}}$/RC3[5,8]	I/O	NVDD
W27	GPIO7/$\overline{\text{IRQ7}}$/RC7[5,8]	I/O	NVDD
W28	GPIO2/$\overline{\text{IRQ2}}$/RC2[5,8]	I/O	NVDD
Y1	M1DQS1	I/O	GVDD1
Y2	$\overline{\text{M1DQS1}}$	I/O	GVDD1
Y3	M1DQ10	I/O	GVDD1
Y4	M1DQ11	I/O	GVDD1
Y5	M1DQ14	I/O	GVDD1
Y6	M1DQ23	I/O	GVDD1
Y7	M1ODT0	O	GVDD1
Y8	M1A12	O	GVDD1
Y9	M1A14	O	GVDD1
Y10	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AB1	$\overline{\text{M1DQS2}}$	I/O	GVDD1
AB2	M1DQS2	I/O	GVDD1
AB3	M1DQ19	I/O	GVDD1
AB4	M1DM2	O	GVDD1
AB5	M1DQ21	I/O	GVDD1
AB6	M1DQ22	I/O	GVDD1
AB7	M1CKE0	O	GVDD1
AB8	M1A11	O	GVDD1
AB9	M1A7	O	GVDD1
AB10	$\overline{\text{M1CK2}}$	O	GVDD1
AB11	M1APAR_OUT	O	GVDD1
AB12	M1ODT1	O	GVDD1
AB13	$\overline{\text{M1APAR\_IN}}$	I	GVDD1
AB14	M1DQ43	I/O	GVDD1
AB15	M1DM5	O	GVDD1
AB16	M1DQ44	I/O	GVDD1
AB17	M1DQ40	I/O	GVDD1
AB18	M1DQ59	I/O	GVDD1
AB19	M1DM7	O	GVDD1
AB20	M1DQ60	I/O	GVDD1
AB21	VSS	Ground	N/A
AB22	GPIO31/I2C_SDA[5,8]	I/O	NVDD
AB23	GPIO27/TMR4/RCW_SRC0[5,8]	I/O	NVDD
AB24	GPIO25/TMR2/RCW_SRC1[5,8]	I/O	NVDD
AB25	GPIO24/TMR1/RCW_SRC2[5,8]	I/O	NVDD
AB26	GPIO10/$\overline{\text{IRQ10}}$/RC10[5,8]	I/O	NVDD
AB27	GPIO5/$\overline{\text{IRQ5}}$/RC5[5,8]	I/O	NVDD
AB28	GPIO0/$\overline{\text{IRQ0}}$/RC0[5,8]	I/O	NVDD
AC1	VSS	Ground	N/A
AC2	GVDD1	Power	N/A
AC3	M1DQ16	I/O	GVDD1
AC4	VSS	Ground	N/A
AC5	GVDD1	Power	N/A
AC6	M1DQ17	I/O	GVDD1
AC7	VSS	Ground	N/A
AC8	GVDD1	Power	N/A
AC9	M1BA2	O	GVDD1
AC10	VSS	Ground	N/A
AC11	GVDD1	Power	N/A
AC12	M1A4	O	GVDD1
AC13	VSS	Ground	N/A
AC14	GVDD1	Power	N/A
AC15	M1DQ42	I/O	GVDD1
AC16	VSS	Ground	N/A
AC17	GVDD1	Power	N/A
AC18	M1DQ58	I/O	GVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AE9	M1A8	O	GVDD1
AE10	GVDD1	Power	N/A
AE11	VSS	Ground	N/A
AE12	M1A0	O	GVDD1
AE13	GVDD1	Power	N/A
AE14	VSS	Ground	N/A
AE15	M1DQ39	I/O	GVDD1
AE16	GVDD1	Power	N/A
AE17	VSS	Ground	N/A
AE18	M1DQ54	I/O	GVDD1
AE19	GVDD1	Power	N/A
AE20	VSS	Ground	N/A
AE21	GPIO29/UART_TXD[5,8]	I/O	NVDD
AE22	TDM1TCK/GE2_RX_CLK[3]	I	NVDD
AE23	TDM1RSN/GE2_RX_CTL[3]	I/O	NVDD
AE24	VSS	Ground	N/A
AE25	TDM3RCK/GE1_GTX_CLK[3]	I/O	NVDD
AE26	TDM3TSN/GE1_RX_CLK[3]	I/O	NVDD
AE27	TDM2RSN/GE1_TD2[3]	I/O	NVDD
AE28	TDM2RDT/GE1_TD1[3]	I/O	NVDD
AF1	M1DQ28	I/O	GVDD1
AF2	M1DM3	O	GVDD1
AF3	M1DQ26	I/O	GVDD1
AF4	M1ECC4	I/O	GVDD1
AF5	M1DM8	O	GVDD1
AF6	M1ECC2	I/O	GVDD1
AF7	M1CKE1	O	GVDD1
AF8	M1CK0	O	GVDD1
AF9	$\overline{\text{M1CK0}}$	O	GVDD1
AF10	M1BA1	O	GVDD1
AF11	M1A1	O	GVDD1
AF12	$\overline{\text{M1WE}}$	O	GVDD1
AF13	M1DQ37	I/O	GVDD1
AF14	M1DM4	O	GVDD1
AF15	M1DQ36	I/O	GVDD1
AF16	M1DQ32	I/O	GVDD1
AF17	M1DQ55	I/O	GVDD1
AF18	M1DM6	O	GVDD1
AF19	M1DQ53	I/O	GVDD1
AF20	M1DQ52	I/O	GVDD1
AF21	GPIO28/UART_RXD[5,8]	I/O	NVDD
AF22	TDM0RSN/GE2_TD2[3]	I/O	NVDD
AF23	TDM0TDT/GE2_TD3[3]	I/O	NVDD
AF24	NVDD	Power	N/A
AF25	TDM2TSN/GE1_TX_CTL[3]	I/O	NVDD
AF26	GE1_RX_CTL	I	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AF27	TDM2TDT/GE1_TX_CLK[3]	I/O	NVDD
AF28	TDM3RSN/GE1_RD1[3]	I/O	NVDD
AG1	M1DQ24	I/O	GVDD1
AG2	GVDD1	Power	N/A
AG3	M1DQ25	I/O	GVDD1
AG4	VSS	Ground	N/A
AG5	GVDD1	Power	N/A
AG6	M1ECC1	I/O	GVDD1
AG7	VSS	Ground	N/A
AG8	GVDD1	Power	N/A
AG9	M1A13	O	GVDD1
AG10	VSS	Ground	N/A
AG11	GVDD1	Power	N/A
AG12	$\overline{\mathrm{M1CS1}}$	O	GVDD1
AG13	VSS	Ground	N/A
AG14	GVDD1	Power	N/A
AG15	M1DQ35	I/O	GVDD1
AG16	VSS	Ground	N/A
AG17	GVDD1	Power	N/A
AG18	M1DQ51	I/O	GVDD1
AG19	VSS	Ground	N/A
AG20	GVDD1	Power	N/A
AG21	NVDD	Power	N/A
AG22	TDM1TSN/GE2_TD1[3]	I/O	NVDD
AG23	TDM1RDT/GE2_TX_CLK[3]	I/O	NVDD
AG24	TDM0TCK/GE2_GTX_CLK[3]	I/O	NVDD
AG25	TDM1TDT/GE2_TD0[3]	I/O	NVDD
AG26	VSS	Ground	N/A
AG27	NVDD	Power	N/A
AG28	TDM3RDT/GE1_RD0[3]	I/O	NVDD
AH1	Reserved.	NC	—
AH2	$\overline{\mathrm{M1DQS3}}$	I/O	GVDD1
AH3	M1DQS3	I/O	GVDD1
AH4	M1ECC0	I/O	GVDD1
AH5	$\overline{\mathrm{M1DQS8}}$	I/O	GVDD1
AH6	M1DQS8	I/O	GVDD1
AH7	M1A5	O	GVDD1
AH8	$\overline{\mathrm{M1CK1}}$	O	GVDD1
AH9	M1CK1	O	GVDD1
AH10	$\overline{\mathrm{M1CS0}}$	O	GVDD1
AH11	M1BA0	O	GVDD1
AH12	$\overline{\mathrm{M1CAS}}$	O	GVDD1
AH13	M1DQ34	I/O	GVDD1
AH14	$\overline{\mathrm{M1DQS4}}$	I/O	GVDD1
AH15	M1DQS4	I/O	GVDD1
AH16	M1DQ50	I/O	GVDD1

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8256 Reference Manual*.

2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8256.

Table 2. Absolute Maximum Ratings

Rating	Power Rail Name	Symbol	Value	Unit
Core supply voltage • Cores 0–5	VDD	V_{DD}	–0.3 to 1.1	V
PLL supply voltage[3]		V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	–0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1	V V V
M3 memory supply voltage	M3VDD	V_{DDM3}	–0.3 to 1.1	V
DDR memory supply voltage	GVDD1, GVDD2	V_{DDDDR}		
• DDR2 mode			–0.3 to 1.98	V
• DDR3 mode			–0.3 to 1.65	V
DDR reference voltage	MVREF	MV_{REF}	–0.3 to 0.51 × V_{DDDDR}	V
Input DDR voltage		V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
I/O voltage excluding DDR and RapidIO lines	NVDD, QVDD	V_{DDIO}	–0.3 to 2.625	V
Input I/O voltage		V_{INIO}	–0.3 to V_{DDIO} + 0.3	V
RapidIO pad voltage	SXPVDD1, SXPVDD2	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O core voltage	SXCVDD1, SXCVDD2	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O PLL voltage[3]		$V_{DDRIOPLL}$	–0.3 to 1.21	V
Input RapidIO I/O voltage		V_{INRIO}	–0.3 to V_{DDSXC} + 0.3	V
Operating temperature		T_J	–40 to 105	°C
Storage temperature range		T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 3**.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8256 (see Figure 37 and Figure 38)

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR2 SDRAM.

Note: At recommended operating conditions (see Table 3) with V_{DDDDR} = 1.8 V.

Table 6. DDR2 SDRAM Interface DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V	2, 3, 4
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$V_{DDDDR} + 0.3$	V	5
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6
Output high current (V_{OUT} (VOH) = 1.37 V)	I_{OH}	–13.4	—	mA	7
Output low current (V_{OUT} (VOL) = 0.33 V)	I_{OL}	13.4	—	mA	7

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} supply voltage at all times. The DRAM and memory controller can use the same or different sources.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} with a minimum value of MV_{REF} – 0.4 and a maximum value of MV_{REF} + 0.04 V. V_{TT} should track variations in the DC-level of MV_{REF}.
4. The voltage regulator for MV_{REF} must be able to supply up to 300 μA.
5. Input capacitance load for DQ, DQS, and DQS signals are available in the IBIS models.
6. Output leakage is measured with all outputs are disabled, $0\text{ V} \leq V_{OUT} \leq V_{DDDDR}$.
7. Refer to the IBIS model for the complete output IV curve characteristics.

2.5.1.2 DDR3 (1.5V) SDRAM DC Electrical Characteristics

Table 7 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Note: At recommended operating conditions (see Table 3) with V_{DDDDR} = 1.5 V.

Table 7. DDR3 SDRAM Interface DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V	2,3,4
Input high voltage	V_{IH}	$MV_{REF} + 0.100$	V_{DDDDR}	V	5
Input low voltage	V_{IL}	GND	$MV_{REF} - 0.100$	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times. The DRAM and memory controller can use the same or different sources.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$ and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±1% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} with a minimum value of MV_{REF} – 0.4 and a maximum value of MV_{REF} + 0.04 V. V_{TT} should track variations in the DC-level of MV_{REF}.
4. The voltage regulator for MV_{REF} must be able to supply up to 250 μA.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ signals are available in the IBIS models.
6. Output leakage is measured with all outputs are disabled, $0\text{ V} \leq V_{OUT} \leq V_{DDDDR}$.

2.5.1.3 DDR2/DDR3 SDRAM Capacitance

Table 8 provides the DDR controller interface capacitance for DDR2 and DDR3 memory.

Note: At recommended operating conditions (see Table 3) with V_{DDDDR} = 1.8 V for DDR2 memory or V_{DDDDR} = 1.5 V for DDR3 memory.

Table 8. DDR2/DDR3 SDRAM Capacitance

Parameter	Symbol	Min	Max	Unit
I/O capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{IO}	6	8	pF
Delta I/O capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{DIO}	—	0.5	pF
Note: Guaranteed by FAB process and micro-construction.				

2.5.1.4 DDR Reference Current Draw

Table 9 lists the current draw characteristics for MV_{REF}.

Note: Values when used at recommended operating conditions (see Table 3).

Table 9. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV_{REFn}	I_{MVREFn}	—		
• DDR2 SDRAM			300	µA
• DDR3 SDRAM			250	µA

2.5.2 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The MSC8256 features an HSSI that includes two 4-channel SerDes ports used for high-speed serial interface applications (PCI Express, Serial RapidIO interfaces, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 2.6.2, “HSSI AC Timing Specifications.”

2.5.2.1 Signal Term Definitions

The SerDes interface uses differential signalling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 4 shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 4 shows the waveform for either a transmitter output (SR[1–2]_TX and

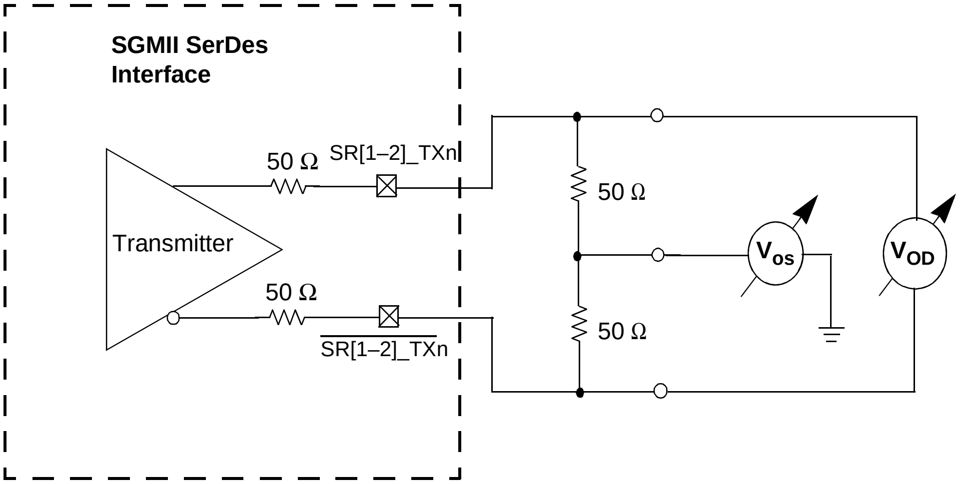

Figure 10. SGMII Transmitter DC Measurement Circuit

Table 16 describes the SGMII SerDes receiver AC-coupled DC electrical characteristics.

Table 16. SGMII DC Receiver Electrical Characteristics[5]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC Input voltage range		—	N/A			—	1
Input differential voltage	SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2		175	—			
Loss of signal threshold	SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2	VLOS	30	—	100	mV	3, 4
	SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1 SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	W	—

Notes:
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in the PCI Express interface. Refer to the PCI Express Differential Receiver (RX) Input Specifications section of the *PCI Express Specification* document. for details.
4. The values for SGMII1 and SGMII2 are selected in the SRDS control registers.
5. The supply voltage is 1.0 V.

Figure 11 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

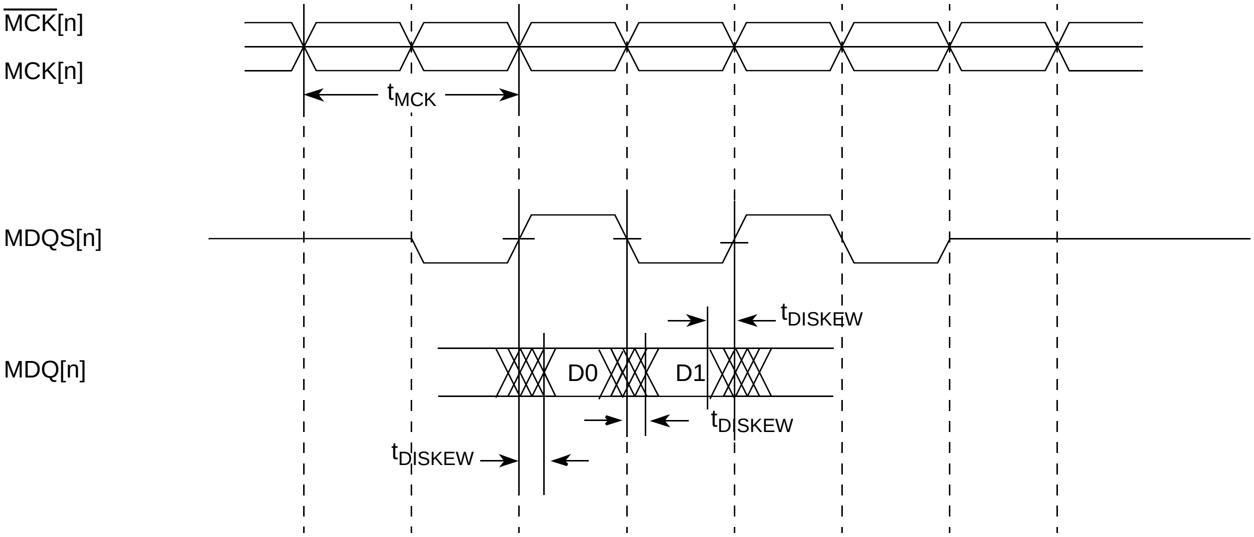

Figure 11. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

2.6.1.2 DDR SDRAM Output AC Timing Specifications

Table 21 provides the output AC timing specifications for the DDR SDRAM interface.

Table 21. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHAS}	 0.917 1.10	 — —	 ns ns	3
ADDR/CMD output hold with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHAX}	 0.767 1.02	 — —	 ns ns	3
$\overline{\text{MCSn}}$ output setup with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHCS}	 0.917 1.10	 — —	 ns ns	3
$\overline{\text{MCSn}}$ output hold with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHCX}	 0.767 1.02	 — —	 ns ns	3
MCK to MDQS Skew • 800 MHz data rate • 667 MHz data rate	t_{DDKHMH}	 –0.4 –0.6	 0.375 0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS • 800 MHz • 667 MHz	t_{DDKHDS}, t_{DDKLDS}	 300 375	 — —	 ps ps	5
MDQ/MECC/MDM output hold with respect to MDQS • 800 MHz • 667 MHz	t_{DDKHDX}, t_{DDKLDX}	 300 375	 — —	 ps ps	5
MDQS preamble	t_{DDKHMP}	$-0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$-0.4 \times t_{MCK}$	$-0.6 \times t_{MCK}$	ns	—

2.6.2.2 PCI Express AC Physical Layer Specifications

The AC requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8256 supports a 2.5 Gbps PCI Express interface defined by the *PCI Express Base Specification*, *Revision 1.0a*. The transmitter specifications are defined in Table 25 and the receiver specifications are defined in Table 26. The parameters are specified at the component pins. the AC timing specifications do not include REF_CLK jitter.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 25. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit interval	UI	399.88	400.00	400.12	ps	1
Minimum Tx eye width	$T_{TX\text{-}EYE}$	0.70	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median.	$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	—	—	0.15	UI	3, 4
AC coupling capacitor	C_{TX}	75	—	200	nF	5

Notes:
1. Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. No test load is necessarily associated with this value.
2. The maximum transmitter jitter can be derived as $T_{TX\text{-}MAX\text{-}JITTER} = 1 – T_{TX\text{-}EYE} = 0.3$ UI.
3. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 8 and measured over any 250 consecutive Tx UIs. A $T_{TX\text{-}EYE} = 0.70$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX} = 0.30$ UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data.
4. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.
5. All transmitters shall be AC-coupled. The AC coupling is required either within the media or within the transmitting component itself. The SerDes transmitter does not have built-in Tx capacitance. An external AC coupling capacitor is required.

Table 26. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	1
Minimum receiver eye width	$T_{RX\text{-}EYE}$	0.4	—	—	UI	2, 3, 4
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	—	—	0.3	UI	3, 4, 5

Notes:
1. Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. No test load is necessarily associated with this value.
2. The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX\text{-}MAX\text{-}JITTER} = 1 – T_{RX\text{-}EYE} = 0.6$ UI.
3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 8 should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
4. A $T_{RX\text{-}EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
5. Jitter is defined as the measurement variation of the crossing points ($V_{RX\text{-}DIFFp\text{-}p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.6.2.3 Serial RapidIO AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 27 defines the transmitter AC specifications for the Serial RapidIO interface. The AC timing specifications do not include REF_CLK jitter.

Table 27. Serial RapidIO Transmitter AC Timing Specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Deterministic Jitter	J_D	—	—	0.17	UI p-p
Total Jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps

Table 28 defines the Receiver AC specifications for the Serial RapidIO interface. The AC timing specifications do not include REF_CLK jitter.

Table 28. Serial RapidIO Receiver AC Timing Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	Notes
Deterministic Jitter Tolerance	J_D	0.37	—	—	UI p-p	1
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total Jitter Tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit Error Rate	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100ppm	800	800 + 100ppm	ps	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—

Notes:
1. Measured at receiver.
2. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 18. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

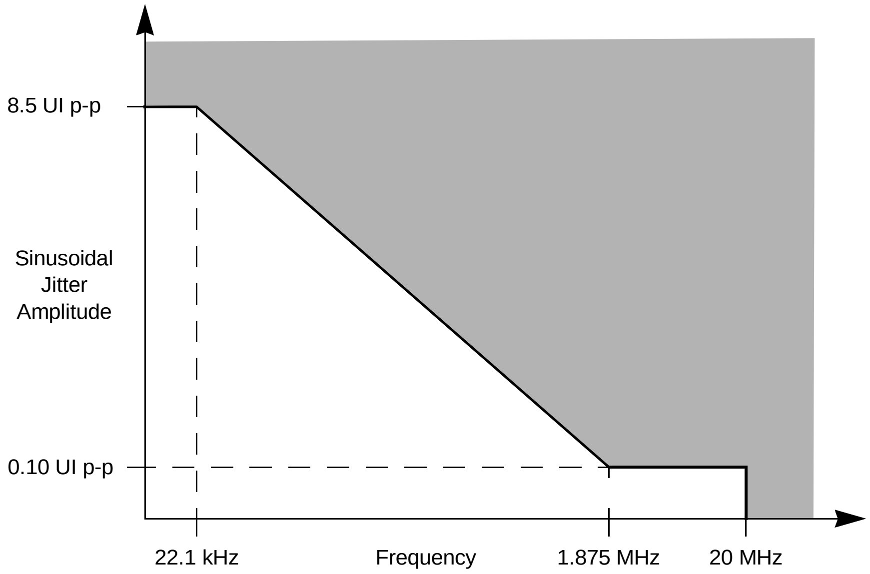

Figure 18. Single Frequency Sinusoidal Jitter Limits

Figure 30 shows the boundary scan (JTAG) timing diagram.

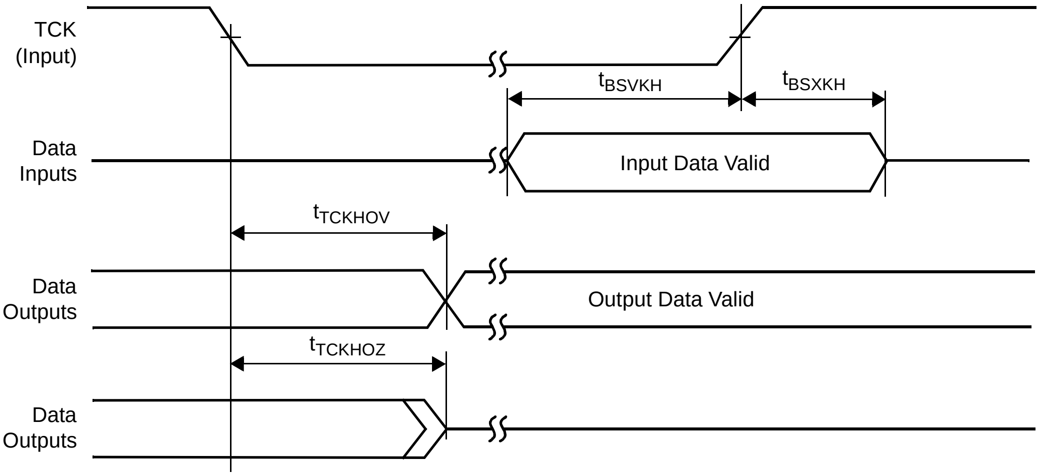

Figure 30. Boundary Scan (JTAG) Timing

Figure 31 shows the test access port timing diagram

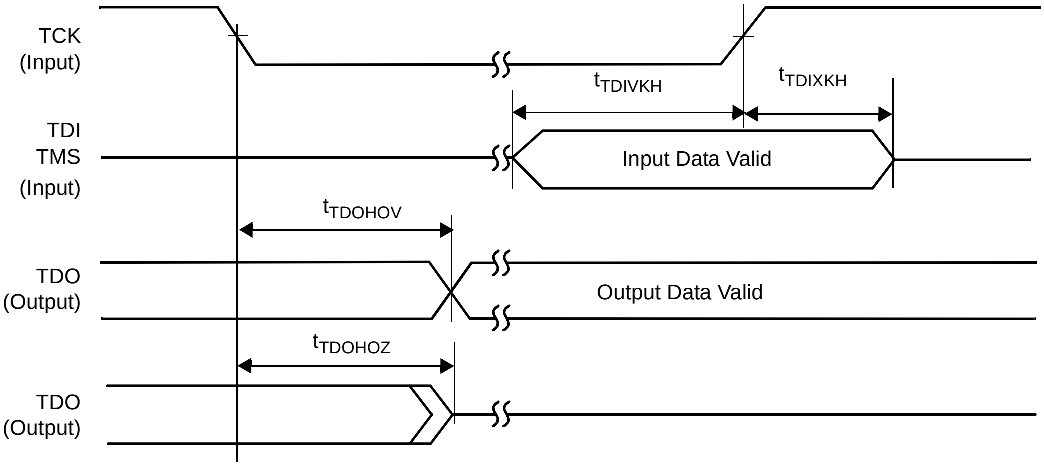

Figure 31. Test Access Port Timing

Figure 32 shows the $\overline{\text{TRST}}$ timing diagram.

Figure 32. $\overline{\text{TRST}}$ Timing

2. After the above rails rise to 90% of their nominal voltage, the following I/O power rails may rise in any sequence (see Figure 34): QVDD, NVDD, GVDD1, and GVDD2.

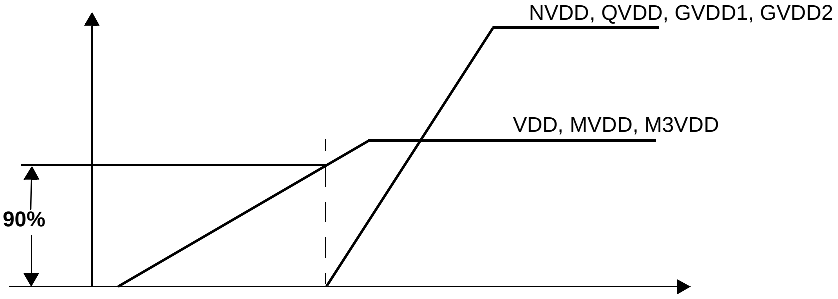

Figure 34. Supply Ramp-Up Sequence

Notes:
1. If the M3 memory is not used, M3VDD can be tied to GND.
2. If the HSSI port1 is not used, SXCVDD1and SXPVDD1 must be connected to the designated power supplies.
3. If the HSSI port2 is not used, SXCVDD2 and SXPVDD2 must be connected to the designated power supplies.
4. If the DDR port 1 interface is not used, it is recommended that GVDD1 be left unconnected.
5. If the DDR port 2 interface is not used, it is recommended that GVDD2 be left unconnected.

3.1.4 Reset Guidelines

When a debugger is not used, implement the connection scheme shown in Figure 35.

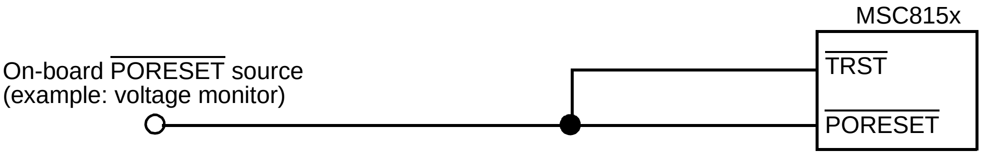

Figure 35. Reset Connection in Functional Application

When a debugger is used, implement the connection scheme shown in Figure 36.

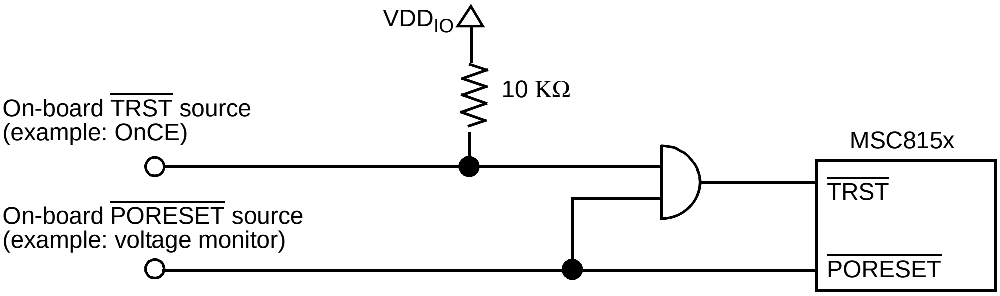

Figure 36. Reset Connection in Debugger Application

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

  Rterm = Rim – Rbuf

  where Rim = trace characteristic impedance

  Rbuf = clock buffer internal impedance.

3.4 SGMII AC-Coupled Serial Link Connection Example

Figure 39 shows an example of a 4-wire AC-coupled serial link connection. For additional layout suggestions, see *AN3556 MSC815x High Speed Serial Interface Hardware Design Considerations*, available on the Freescale website or from your local sales office or representative.

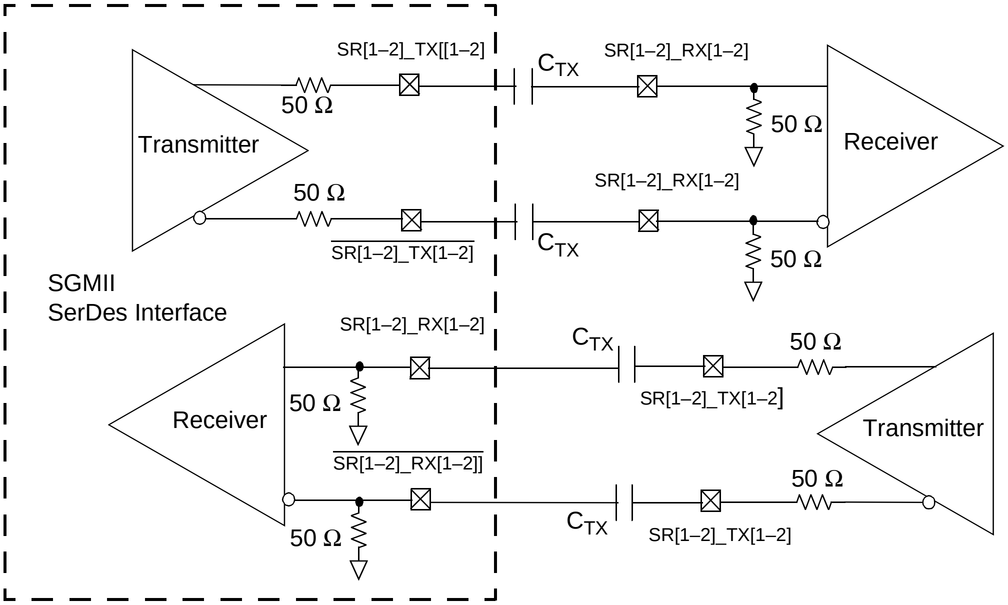

Figure 39. 4-Wire AC-Coupled SGMII Serial Link Connection Example

3.5 Connectivity Guidelines

Note: Although the package actually uses a ball grid array, the more conventional term pin is used to denote signal connections in this discussion.

First, select the pin multiplexing mode to allocate the required I/O signals. Then use the guidelines presented in the following subsections for board design and connections. The following conventions are used in describing the connectivity requirements:

1. GND indicates using a 10 kΩ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
2. V_{DD} indicates using a 10 kΩ pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50 mA through the I/O supply that adds to overall power consumption.
3. Mandatory use of a pull-up or pull-down resistor is clearly indicated as “pull-up/pull-down.” For buses, each pin on the bus should have its own resistor.
4. NC indicates “not connected” and means do not connect anything to the pin.
5. The phrase “in use” indicates a typical pin connection for the required function.

Note: Please see recommendations #1 and #2 as mandatory pull-down or pull-up connection for unused pins in case of subset interface connection.

3.5.1 DDR Memory Related Pins

This section discusses the various scenarios that can be used with either of the MSC8256 DDR ports.

Note: The signal names in Table 40, Table 41 and Table 42 are generic names for a DDR SDRAM interface. For actual pin names refer to Table 1.

3.5.1.1 DDR Interface Is Not Used

Table 40. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Signal Name	Pin Connection
MDQ[0–63]	NC
MDQS[7–0]	NC
$\overline{\text{MDQS[7–0]}}$	NC
MA[15–0]	NC
MCK[0–2]	NC
$\overline{\text{MCK[0–2]}}$	NC
$\overline{\text{MCS[1–0]}}$	NC
MDM[7–0]	NC
MBA[2–0]	NC
$\overline{\text{MCAS}}$	NC
MCKE[1–0]	NC
MODT[1–0]	NC
MMDIC[1–0]	NC
$\overline{\text{MRAS}}$	NC
$\overline{\text{MWE}}$	NC
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS8}}$	NC
MAPAR_OUT	NC
$\overline{\text{MAPAR\_IN}}$	NC
MVREF[3]	NC
GVDD1/GVDD2[3]	NC

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. If the DDR controller is not used, disable the internal DDR clock by setting the appropriate bit in the System Clock Control Register (SCCR) and put all DDR I/O in sleep mode by setting DRx_GCR[DDRx_DOZE] (for DDR controller x). See the *Clocks* and *General Configuration Registers* chapters in the ***MSC8256 Reference Manual*** for details.
3. For MSC8256 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8256, connecting these pins to GND increases device power consumption.

6 Product Documentation

Following is a general list of supporting documentation:

- *MSC8256 Technical Data Sheet* (MSC8256). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8256 device.
- *MSC8256 Reference Manual* (MSC8256RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8256 device.
- *QUICC Engine Block Reference Manual with Protocol Interworking* (QEIWRM). Provides detailed information regarding the QUICC Engine technology including functional description, registers, and programming information.
- *SC3850 DSP Core Reference Manual*. Covers the SC3850 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8156SC3850 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

7 Revision History

Table 50 provides a revision history for this data sheet.

Table 50. Document Revision History

Rev.	Date	Description
0	Apr 2010	• Initial public release.
1	Dec 2010	• Updated Table 16. • Updated **Section 3.1.2**, *Power-On Ramp Time*. • Updated **Section 4**, *Ordering Information*.
2	Mar 2011	• Updated Table 8. • Updated Table 15. • Updated Table 17. • Updated Table 33. • Updated Table 35. • Updated Table 39.
3	May 2011	• Updated Table 1. Changed the pin types for the following: – F25 from ground to power. – F26 from power to ground. – T6 from power to O.
4	Oct 2011	• Updated Table 34 and Table 35 to reflect 1 Gbps and 100 Mbps data rate instead of 1 GHz and 100 MHz.
5	Dec 2011	• Added note 4 to Table 39.