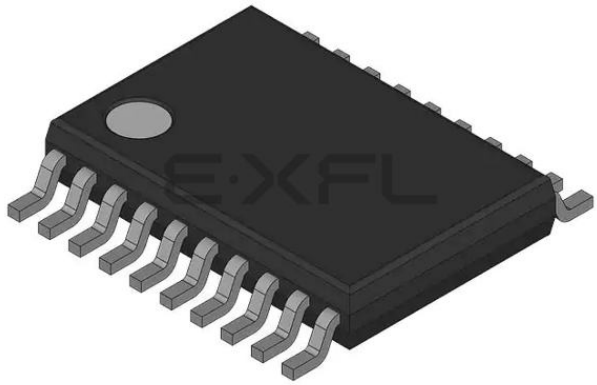

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08el16ctj

Chapter 1
Device Overview

The MC9S08EL32 Series and MC9S08SL16 Series are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

1.1 Devices in the MC9S08EL32 Series and MC9S08SL16 Series

Table 1-1 summarizes the feature set available in the MC9S08EL32 Series and MC9S08SL16 Series of MCUs.

Table 1-1. MC9S08EL32 Series and MC9S08SL16 Series Features by MCU and Package

Feature	9S08EL32		9S08EL16		9S08SL16		9S08SL8	
FLASH size (bytes)	32768		16384		16384		8192	
RAM size (bytes)	1024				512			
EEPROM size (bytes)	512				256			
Pin quantity	28	20	28	20	28	20	28	20
Package type	TSSOP	TSSOP	TSSOP	TSSOP	TSSOP	TSSOP	TSSOP	TSSOP
Port Interrupts	16	12	16	12	16	12	16	12
ACMP1	yes				yes			
ACMP2	yes	no	yes	no	no			
ADC channels	16	12	16	12	16	12	16	12
DBG	yes				yes			
ICS	yes				yes			
IIC	yes				yes			
RTC	yes				yes			
SCI	yes				yes			
SLIC	yes				yes			
SPI	yes				yes			
TPM1 channels	4				2			
TPM2 channels	2				2			
XOSC	yes				yes			

2.2 Recommended System Connections

Figure 2-3 shows pin connections that are common to MC9S08EL32 Series and MC9S08SL16 Series application systems.

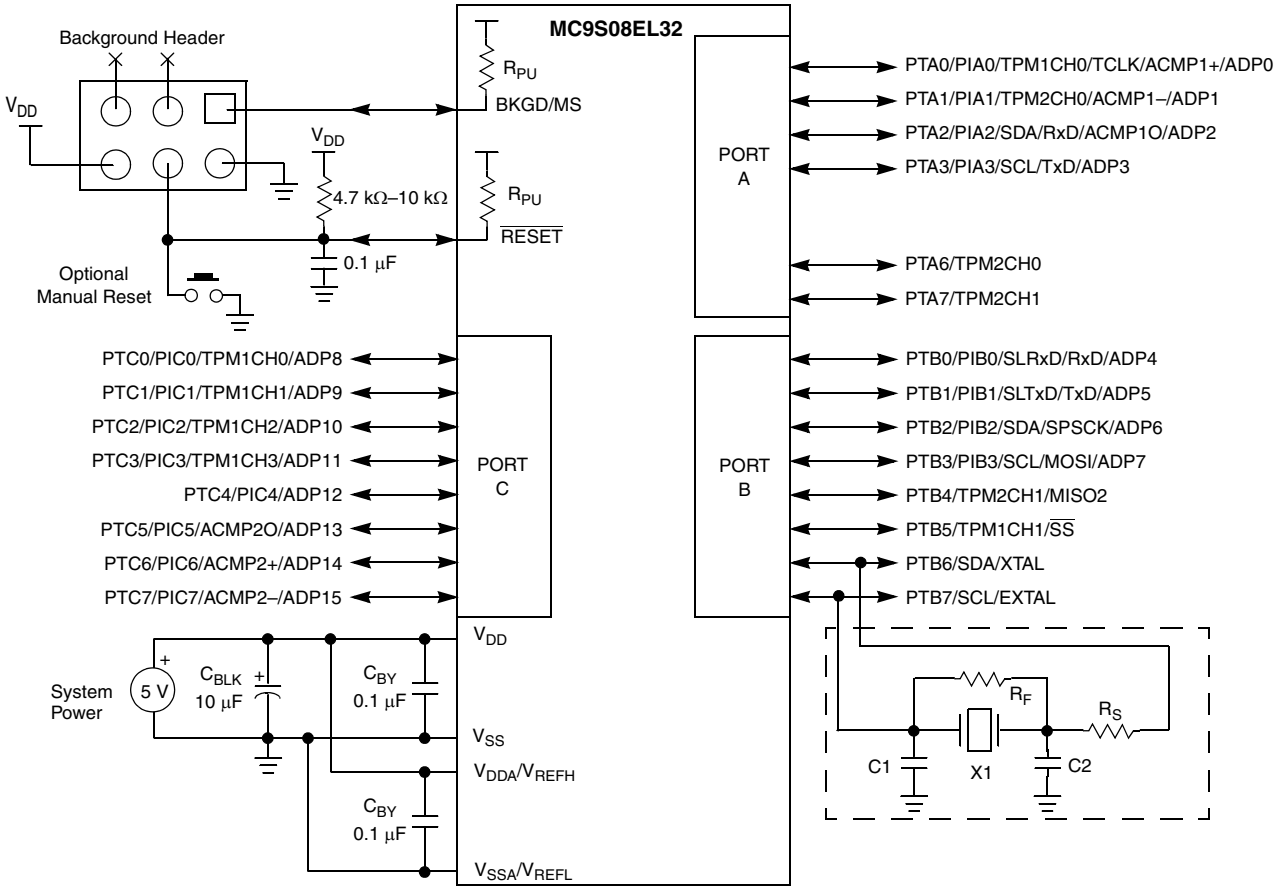


Figure 2-3. Basic System Connections

2.2.1 Power

V_{DD} and V_{SS} are the primary power supply pins for the MCU. This voltage source supplies power to all I/O buffer circuitry and to an internal voltage regulator. The internal voltage regulator provides a regulated lower-voltage source to the CPU and other internal circuitry of the MCU.

Typically, application systems have two separate capacitors across the power pins. In this case, there should be a bulk electrolytic capacitor, such as a 10-µF tantalum capacitor, to provide bulk charge storage for the overall system and a 0.1-µF ceramic bypass capacitor located as near to the MCU power pins as practical to suppress high-frequency noise. Each pin must have a bypass capacitor for best noise suppression.

V_{DDA} and V_{SSA} are the analog power supply pins for the MCU. This voltage source supplies power to the ADC module. A 0.1-µF ceramic bypass capacitor should be located as near to the MCU power pins as practical to suppress high-frequency noise. The V_{REFH} and V_{REFL} pins are the voltage reference high and voltage reference low inputs, respectively, for the ADC module.

Table 3-2. Stop Mode Behavior

Peripheral	Mode	
	Stop2	Stop3
CPU	Off	Standby
RAM	Standby	Standby
FLASH/EEPROM	Off	Standby
Parallel Port Registers	Off	Standby
ACMPx	Off	Optionally On[1]
ADC	Off	Optionally On[2]
ICS	Off	Optionally On[3]
IIC	Off	Standby
RTC	Off	Optionally On[4]
SCI	Off	Standby
SLIC	Off	Standby
SPI	Off	Standby
TPMx	Off	Standby
Voltage Regulator	Standby	Standby
XOSC	Off	Optionally On[5]
I/O Pins	States Held	States Held

1 LVD must be enabled, else in standby.

2 Asynchronous ADC clock and LVD must be enabled, else in standby.

3 IRCLKEN and IREFSTEN must be set in ICSC1, else in standby.

4 RTC must be enabled, else in standby.

5 ERCLKEN and EREFSTEN must be set in ICSC2, else in standby. For high frequency range (RANGE in ICSC2 set), the LVD must be enabled in stop3.

High-page registers, shown in Table 4-3, are accessed much less often than other I/O and control registers so they have been located outside the direct addressable memory space, starting at 0x1800.

Table 4-3. High-Page Register Summary (Sheet 1 of 2)

Address	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
0x1800	SRS	POR	PIN	COP	ILOP	ILAD	0	LVD	0
0x1801	SBDFR	0	0	0	0	0	0	0	BDFR
0x1802	SOPT1	COPT		STOPE	SCIPS	IICPS		0	0
0x1803	SOPT2	COPCLKS	COPW	0	ACIC	T2CH1PS	T2CH0PS	T1CH1PS	T1CH0PS
0x1804 – 0x1805	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
0x1806	SDIDH	—	—	—	—	ID11	ID10	ID9	ID8
0x1807	SDIDL	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0x1808	Reserved	—	—	—	—	—	—	—	—
0x1809	SPMSC1	LVWF	LVWACK	LVWIE	LVDRE	LVDSE	LVDE	0	BGBE
0x180A	SPMSC2	0	0	LVDV	LVWV	PPDF	PPDACK	—	PPDC
0x180B– 0x180F	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
0x1810	DBGCAH	Bit 15	14	13	12	11	10	9	Bit 8
0x1811	DBGCAL	Bit 7	6	5	4	3	2	1	Bit 0
0x1812	DBGCBH	Bit 15	14	13	12	11	10	9	Bit 8
0x1813	DBGCBL	Bit 7	6	5	4	3	2	1	Bit 0
0x1814	DBGFH	Bit 15	14	13	12	11	10	9	Bit 8
0x1815	DBGFL	Bit 7	6	5	4	3	2	1	Bit 0
0x1816	DBGC	DBGEN	ARM	TAG	BRKEN	RWA	RWAEN	RWB	RWBEN
0x1817	DBGT	TRGSEL	BEGIN	0	0	TRG3	TRG2	TRG1	TRG0
0x1818	DBGS	AF	BF	ARMF	0	CNT3	CNT2	CNT1	CNT0
0x1819– 0x181F	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
0x1820	FCDIV	DIVLD	PRDIV8	DIV					
0x1821	FOPT	KEYEN	FNORED	EPGMOD	0	0	0	SEC	
0x1822	Reserved	0	0	0	0	0	0	0	0
0x1823	FCNFG	0	EPGSEL	KEYACC	0	0	0	0	0
0x1824	FPROT	EPS		FPS					FPOP
0x1825	FSTAT	FCBEF	FCCF	FPVIOL	FACCERR	0	FBLANK	0	0
0x1826	FCMD	FCMD							
0x1827– 0x183F	Reserved	— —	— —	— —	— —	— —	— —	— —	— —
0x1840	PTAPE	PTAPE7	PTAPE6	0	0	PTAPE3	PTAPE2	PTAPE1	PTAPE0
0x1841	PTASE	PTASE7	PTASE6	0	0	PTASE3	PTASE2	PTASE1	PTASE0
0x1842	PTADS	PTADS7	PTADS6	0	0	PTADS3	PTADS2	PTADS1	PTADS0
0x1843	Reserved	—	—	—	—	—	—	—	—
0x1844	PTASC	0	0	0	0	PTAIF	PTAACK	PTAIE	PTAMOD

7.3 Addressing Modes

Addressing modes define the way the CPU accesses operands and data. In the HCS08, all memory, status and control registers, and input/output (I/O) ports share a single 64-Kbyte linear address space so a 16-bit binary address can uniquely identify any memory location. This arrangement means that the same instructions that access variables in RAM can also be used to access I/O and control registers or nonvolatile program space.

Some instructions use more than one addressing mode. For instance, move instructions use one addressing mode to specify the source operand and a second addressing mode to specify the destination address. Instructions such as BRCLR, BRSET, CBEQ, and DBNZ use one addressing mode to specify the location of an operand for a test and then use relative addressing mode to specify the branch destination address when the tested condition is true. For BRCLR, BRSET, CBEQ, and DBNZ, the addressing mode listed in the instruction set tables is the addressing mode needed to access the operand to be tested, and relative addressing mode is implied for the branch destination.

7.3.1 Inherent Addressing Mode (INH)

In this addressing mode, operands needed to complete the instruction (if any) are located within CPU registers so the CPU does not need to access memory to get any operands.

7.3.2 Relative Addressing Mode (REL)

Relative addressing mode is used to specify the destination location for branch instructions. A signed 8-bit offset value is located in the memory location immediately following the opcode. During execution, if the branch condition is true, the signed offset is sign-extended to a 16-bit value and is added to the current contents of the program counter, which causes program execution to continue at the branch destination address.

7.3.3 Immediate Addressing Mode (IMM)

In immediate addressing mode, the operand needed to complete the instruction is included in the object code immediately following the instruction opcode in memory. In the case of a 16-bit immediate operand, the high-order byte is located in the next memory location after the opcode, and the low-order byte is located in the next memory location after that.

7.3.4 Direct Addressing Mode (DIR)

In direct addressing mode, the instruction includes the low-order eight bits of an address in the direct page (0x0000–0x00FF). During execution a 16-bit address is formed by concatenating an implied 0x00 for the high-order half of the address and the direct address from the instruction to get the 16-bit address where the desired operand is located. This is faster and more memory efficient than specifying a complete 16-bit address for the operand.

Table 8-5. ICS Status and Control Register Field Descriptions (continued)

Field	Description
1	**OSC Initialization** — If the external reference clock is selected by ERCLKEN or by the ICS being in FEE, FBE, or FBELP mode, and if EREFS is set, then this bit is set after the initialization cycles of the external oscillator clock have completed. This bit is only cleared when either ERCLKEN or EREFS are cleared.
0	**ICS Fine Trim** — The FTRIM bit controls the smallest adjustment of the internal reference clock frequency. Setting FTRIM will increase the period and clearing FTRIM will decrease the period by the smallest amount possible.

8.4 Functional Description

8.4.1 Operational Modes

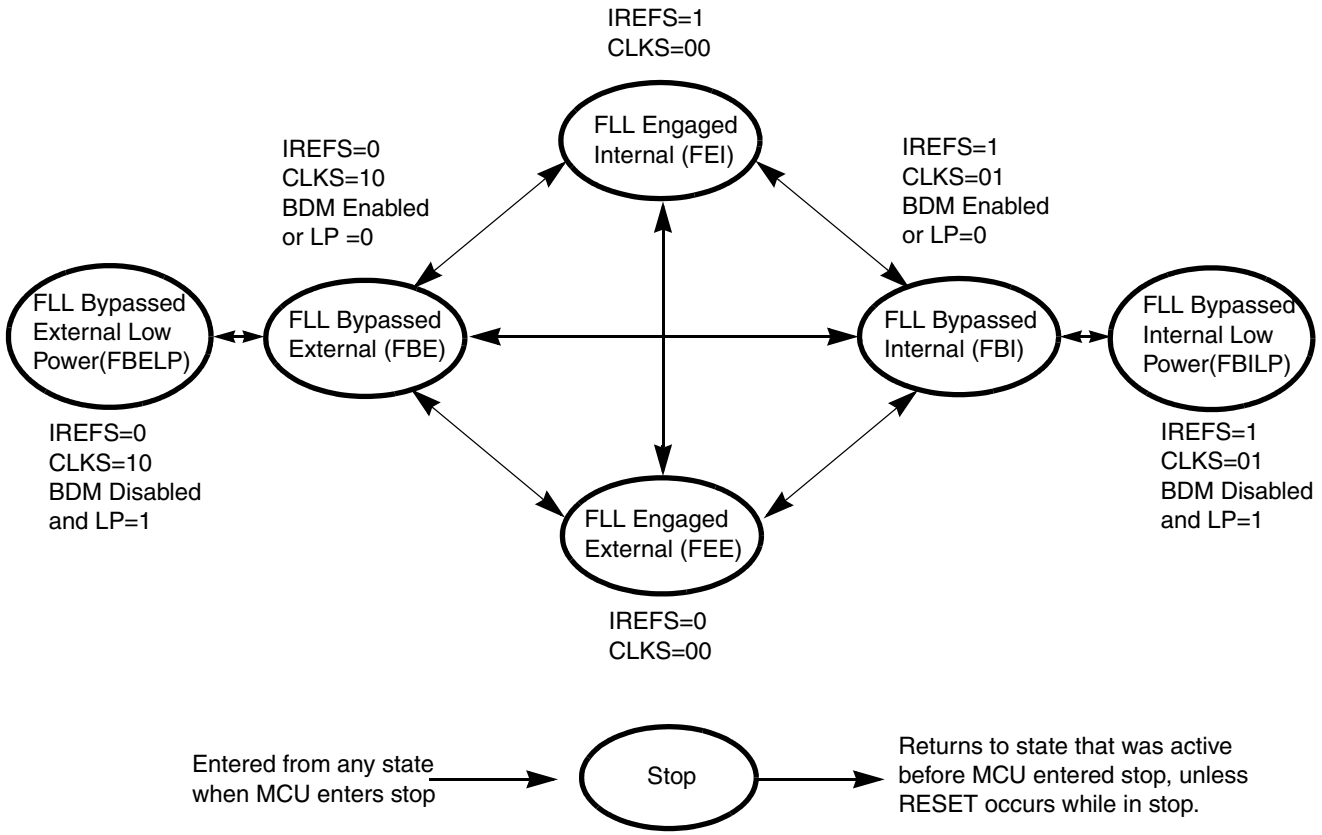


Figure 8-7. Clock Switching Modes

The seven states of the ICS are shown as a state diagram and are described below. The arrows indicate the allowed movements between the states.

8.4.1.1 FLL Engaged Internal (FEI)

FLL engaged internal (FEI) is the default mode of operation and is entered when all the following conditions occur:

9.1.3 Features

The ACMP has the following features:

- Full rail to rail supply operation.
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output.
- Option to compare to fixed internal bandgap reference voltage.
- Option to allow comparator output to be visible on a pin, ACMPxO.
- Can operate in stop3 mode

9.1.4 Modes of Operation

This section defines the ACMP operation in wait, stop and background debug modes.

9.1.4.1 ACMP in Wait Mode

The ACMP continues to run in wait mode if enabled before executing the WAIT instruction. Therefore, the ACMP can be used to bring the MCU out of wait mode if the ACMP interrupt, ACIE is enabled. For lowest possible current consumption, the ACMP should be disabled by software if not required as an interrupt source during wait mode.

9.1.4.2 ACMP in Stop Modes

9.1.4.2.1 Stop3 Mode Operation

The ACMP continues to operate in Stop3 mode if enabled and compare operation remains active. If ACOPE is enabled, comparator output operates as in the normal operating mode and comparator output is placed onto the external pin. The MCU is brought out of stop when a compare event occurs and ACIE is enabled; ACF flag sets accordingly.

If stop is exited with a reset, the ACMP will be put into its reset state.

9.1.4.2.2 Stop2 and Stop1 Mode Operation

During either Stop2 and Stop1 mode, the ACMP module will be fully powered down. Upon wake-up from Stop2 or Stop1 mode, the ACMP module will be in the reset state.

9.1.4.3 ACMP in Active Background Mode

When the microcontroller is in active background mode, the ACMP will continue to operate normally.

Figure 10-1 shows the MC9S08EL32 with the ADC module highlighted.

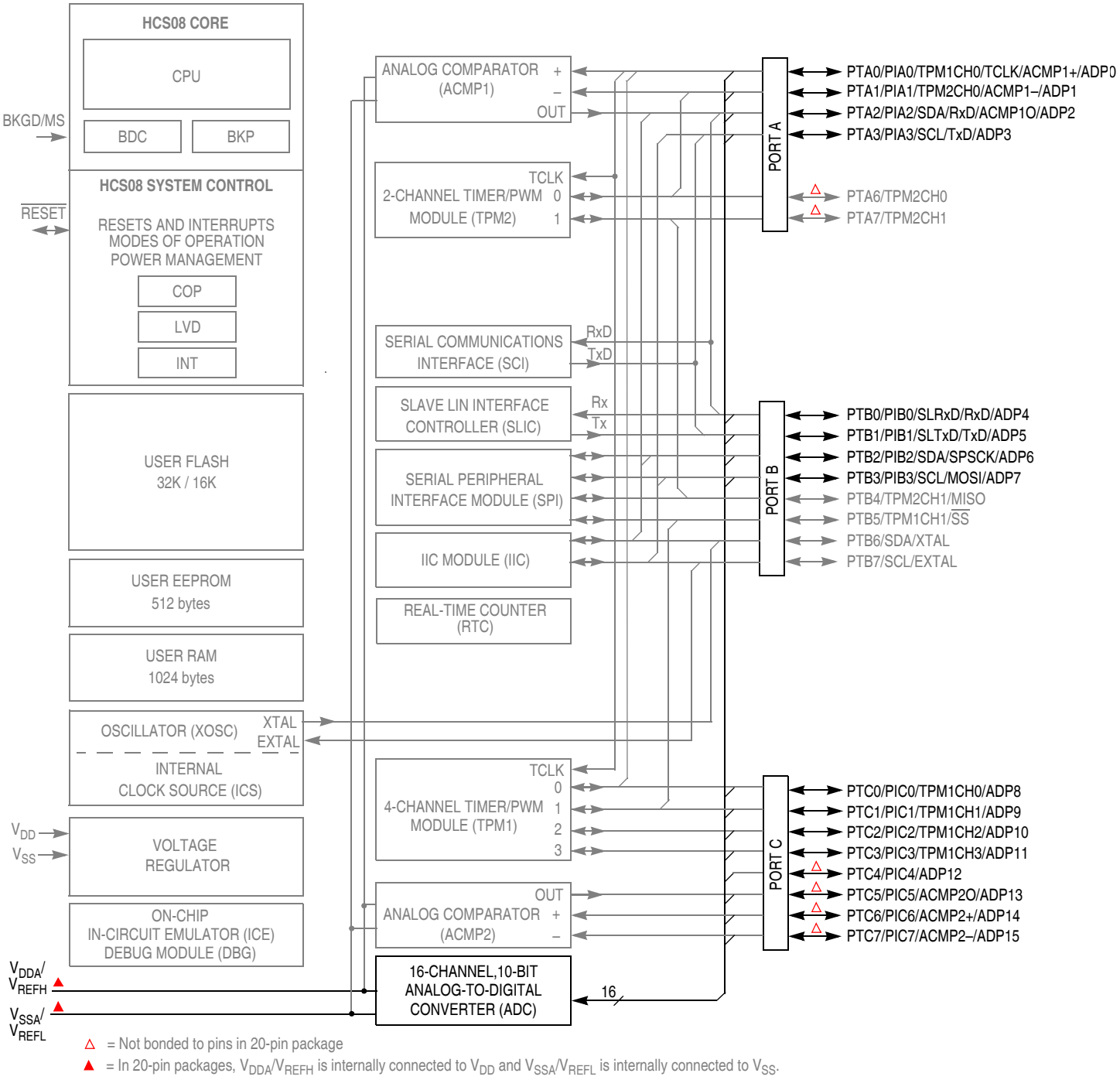


Figure 10-1. MC9S08EL32 Block Diagram Highlighting ADC Block and Pins

Chapter 12
Slave LIN Interface Controller (S08SLICV1)

12.1 Introduction

The slave LIN interface controller (SLIC) is designed to provide slave node connectivity on a local interconnect network (LIN) sub-bus. LIN is an open-standard serial protocol developed for the automotive industry to connect sensors, motors, and actuators.

	7	6	5	4	3	2	1	0
R	SLCACT	0	INITACK	0	0	0	0	SLCF
W								
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 12-8. SLIC Status Register (SLCS)

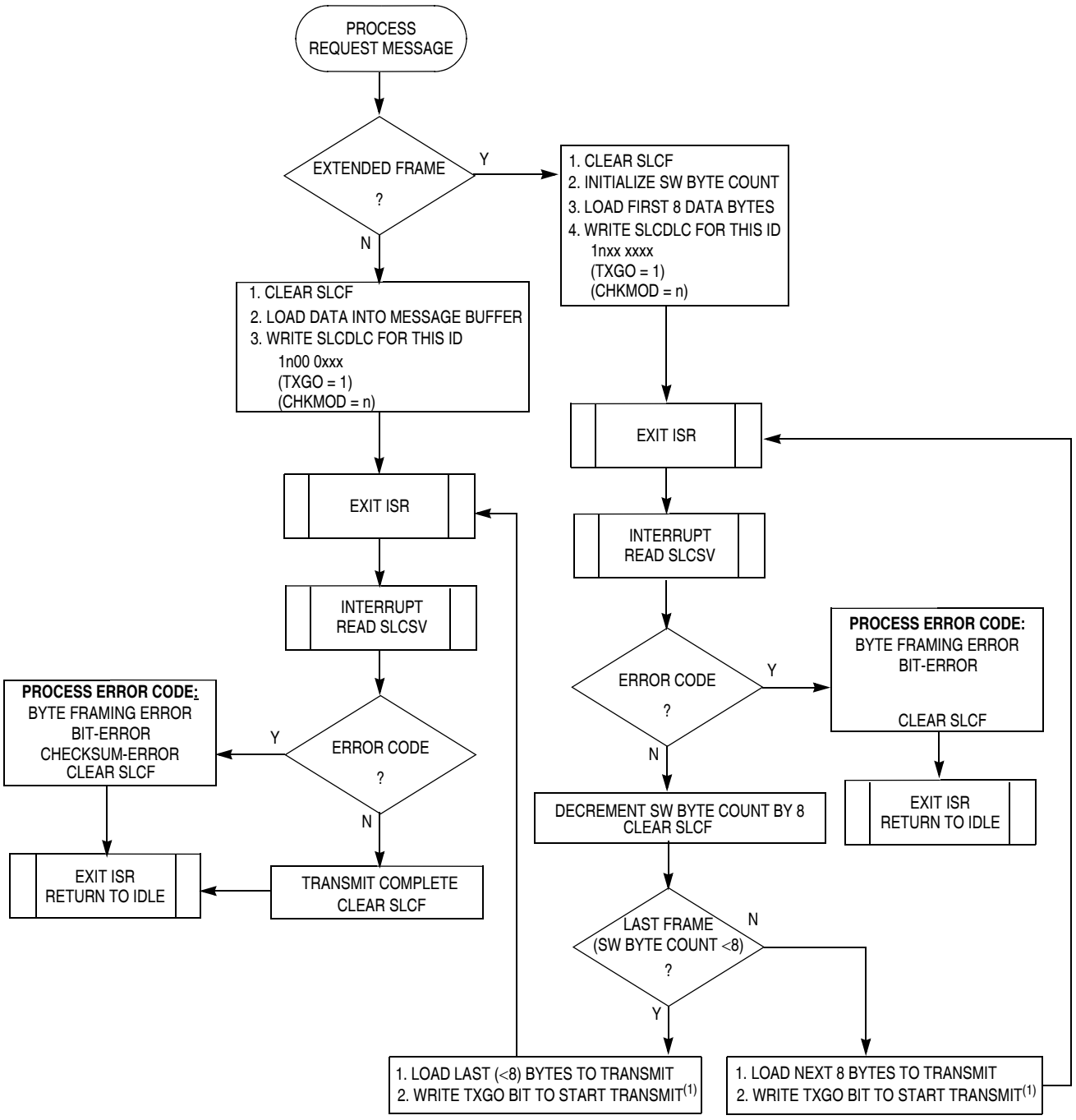
Table 12-6. SLCS Field Descriptions

Field	Description
7 SLCACT[1]	**SLIC Active (Oscillator Trim Blocking Semaphore)** — SLCACT is used to indicate if it is safe to trim the oscillator based upon current SLIC activity in LIN mode. This bit indicates that the SLIC module might be currently receiving a message header, synchronization byte, ID byte, or sending or receiving data bytes. This bit is read-only. This bit has no meaning in BTM mode (BTM =1). 0 SLIC module not active (safe to trim oscillator) SLCACT is cleared by the SLIC module only upon assertion of the RX Message Buffer Full Checksum OK (SLCSV = 0x10) or the TX Message Buffer Empty Checksum Transmitted (SLCSV = 0x08) interrupt sources. 1 SLIC module activity (not safe to trim oscillator) SLCACT is automatically set to 1 if a falling edge is seen on the SLCRX pin and has successfully been passed through the digital RX filter. This edge is the potential beginning of a LIN message frame.
5 INITACK	**Initialization Mode Acknowledge** — INITACK indicates whether the SLIC module is in the reset mode as a result of writing INITREQ in SLCC1. INITACK = 1 causes all SLIC register bits (except SLCWCM: write once) to be held in their reset state and become not writable until INITACK has been cleared. Clear INITACK by clearing INITREQ in SLCC1. After INITACK is cleared, the SLIC module proceeds to SLIC DISABLED mode (see Figure 12-2) in which the other SLIC register bits are writable and can be configured to the desired SLIC operating mode. INITACK is a read-only bit. 0 Normal operation 1 SLIC module is in reset state
0 SLCF	**SLIC Interrupt Flag** — The SLCF interrupt flag indicates if a SLIC module interrupt is pending. If set, the SLCSV is then used to determine what interrupt is pending. This flag is cleared by writing a 1 to the bit. If additional interrupt sources are pending, the bit will be automatically set to 1 again by the SLIC. 0 No SLIC interrupt pending 1 SLIC interrupt pending

[1] SLCACT may not be clear during all idle times of the bus. For example, if IMSG was used to ignore the data interrupts of an extended message frame, SLCACT will remain set until another LIN message is received and either the RX Message Buffer Full Checksum OK (SLCSV = 0x10) or the TX Message Buffer Empty Checksum Transmitted (SLCSV = 0x08) interrupt sources are asserted and cleared. When clear, SLCACT always indicates times when the SLIC module is not active, but it is possible for the SLIC module to be not active with SLCACT set. SLCACT has no meaning in BTM mode.

12.3.5 SLIC State Vector Register (SLCSV)

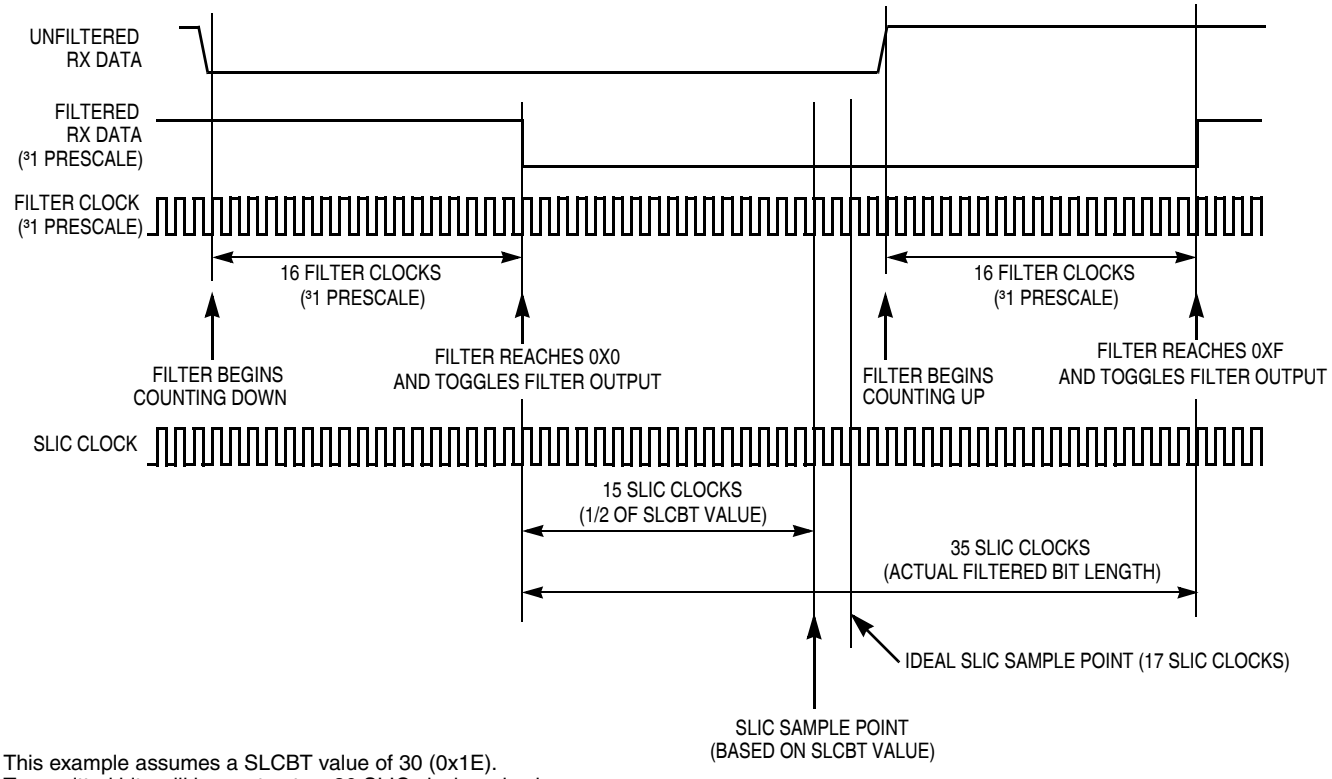
SLIC state vector register (SLCSV) is provided to substantially decrease the CPU overhead associated with servicing interrupts while under operation of a LIN protocol. It provides an index offset that is directly related to the LIN module's current state, which can be used with a user supplied jump table to rapidly enter an interrupt service routine. This eliminates the need for the user to maintain a duplicate state machine in software.



Note 1. When writing TXGO bit only, ensure that CHKMOD and data length values are not accidentally modified.

Figure 12-16. Handling Request LIN Message Frames

The next SLIC interrupt which occurs, if unmasked, will indicate the end of the request message frame and will either indicate that the frame was properly transmitted or that an error was encountered during transmission. Refer to Section 12.6.9.4, “Possible Errors on Request Message Data,” for more detailed explanation of these possible errors. This interrupt also signals to the application that the message frame is complete and all data bytes and the checksum value have been properly transmitted onto the bus.



This example assumes a SLCBT value of 30 (0x1E).
Transmitted bits will be sent out as 30 SLIC clock cycles long.

The proper closest SLCBT setting would be 34 (0x22),
which gives the ideal sample point of 17 SLIC clocks and
transmitted bits are 34 SLIC clocks long.

Figure 12-21. BTM Mode Receive Byte Sampling Example

The error also comes into effect with transmitted bit times. Using the previous example with a SLCBT value of 34, transmitted bits will appear as 34 SLIC clock periods long. This is one SLIC clock short of the proper length. Depending on the frequency of the SLIC clock, one period of the SLIC clock might be a large or a small fraction of one ideal bit time. Raising the frequency of the SLIC clock will reduce this error relative to the ideal bit time, improving the resolution of the SLIC clock relative to the bit rate of the bus. In any case, the error is still one SLIC clock cycle. Raising the SLIC clock frequency, however, requires programming a higher value for SLCBT to maintain the same target bit rate.

Smaller values of SLCBT combined with higher values of the SLIC clock frequency (smaller clock period) will give faster bit rates, but the SLIC clock period becomes an increasingly significant portion of one bit time.

Because BTM mode does not perform any synchronization and relies on the accuracy of the data provided by the user software to set its sample point and generate transmitted bits, the constraint on maximum speeds is only limited to the limits imposed by the digital filter delay and the SLIC input clock. Because the digital filter delay cannot be less than 16 SLIC clock cycles, the fastest possible pulse which would pass the filter is 16 clock periods at 8 MHz, or 500,000 bits/second. The values shown in Table 12-14 are the same values shown in Table 12-15 and indicate the absolute fastest bit rates which could just pass the minimum digital filter settings (prescaler = divide by 1) under perfect conditions.

15.3.1 RTC Status and Control Register (RTCSC)

RTCSC contains the real-time interrupt status flag (RTIF), the clock select bits (RTCLKS), the real-time interrupt enable bit (RTIE), and the prescaler select bits (RTCPS).

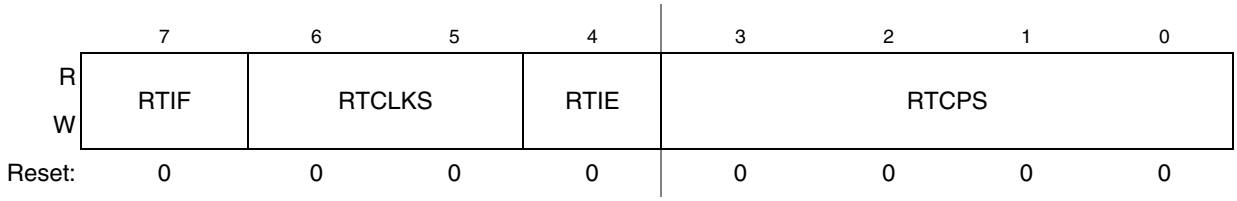


Figure 15-3. RTC Status and Control Register (RTCSC)

Table 15-2. RTCSC Field Descriptions

Field	Description
7 RTIF	Real-Time Interrupt Flag This status bit indicates the RTC counter register reached the value in the RTC modulo register. Writing a logic 0 has no effect. Writing a logic 1 clears the bit and the real-time interrupt request. Reset clears RTIF. 0 RTC counter has not reached the value in the RTC modulo register. 1 RTC counter has reached the value in the RTC modulo register.
6–5 RTCLKS	Real-Time Clock Source Select. These two read/write bits select the clock source input to the RTC prescaler. Changing the clock source clears the prescaler and RTCCNT counters. When selecting a clock source, ensure that the clock source is properly enabled (if applicable) to ensure correct operation of the RTC. Reset clears RTCLKS. 00 Real-time clock source is the 1-kHz low power oscillator (LPO) 01 Real-time clock source is the external clock (ERCLK) 1x Real-time clock source is the internal clock (IRCLK)
4 RTIE	Real-Time Interrupt Enable. This read/write bit enables real-time interrupts. If RTIE is set, then an interrupt is generated when RTIF is set. Reset clears RTIE. 0 Real-time interrupt requests are disabled. Use software polling. 1 Real-time interrupt requests are enabled.
3–0 RTCPS	Real-Time Clock Prescaler Select. These four read/write bits select binary-based or decimal-based divide-by values for the clock source. See Table 15-3. Changing the prescaler value clears the prescaler and RTCCNT counters. Reset clears RTCPS.

Table 15-3. RTC Prescaler Divide-by values

RTCLKS[0]	RTCPS															
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
0	Off	2^3	2^5	2^6	2^7	2^8	2^9	2^{10}	1	2	2^2	10	2^4	10^2	$5x10^2$	10^3
1	Off	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}	10^3	$2x10^3$	$5x10^3$	10^4	$2x10^4$	$5x10^4$	10^5	$2x10^5$

16.1.1 Features

The TPM includes these distinctive features:

- One to eight channels:
  - Each channel may be input capture, output compare, or edge-aligned PWM
  - Rising-Edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
  - Selectable polarity on PWM outputs
- Module may be configured for buffered, center-aligned pulse-width-modulation (CPWM) on all channels
- Timer clock source selectable as prescaled bus clock, fixed system clock, or an external clock pin
  - Prescale taps for divide-by 1, 2, 4, 8, 16, 32, 64, or 128
  - Fixed system clock source are synchronized to the bus clock by an on-chip synchronization circuit
  - External clock pin may be shared with any timer channel pin or a separated input pin
- 16-bit free-running or modulo up/down count operation
- Timer system enable
- One interrupt per channel plus terminal count interrupt

16.1.2 Modes of Operation

In general, TPM channels may be independently configured to operate in input capture, output compare, or edge-aligned PWM modes. A control bit allows the whole TPM (all channels) to switch to center-aligned PWM mode. When center-aligned PWM mode is selected, input capture, output compare, and edge-aligned PWM functions are not available on any channels of this TPM module.

When the microcontroller is in active BDM background or BDM foreground mode, the TPM temporarily suspends all counting until the microcontroller returns to normal user operating mode. During stop mode, all system clocks, including the main oscillator, are stopped; therefore, the TPM is effectively disabled until clocks resume. During wait mode, the TPM continues to operate normally. Provided the TPM does not need to produce a real time reference or provide the interrupt source(s) needed to wake the MCU from wait mode, the user can save power by disabling TPM functions before entering wait mode.

- Input capture mode

  When a selected edge event occurs on the associated MCU pin, the current value of the 16-bit timer counter is captured into the channel value register and an interrupt flag bit is set. Rising edges, falling edges, any edge, or no edge (disable channel) may be selected as the active edge which triggers the input capture.
- Output compare mode

  When the value in the timer counter register matches the channel value register, an interrupt flag bit is set, and a selected output action is forced on the associated MCU pin. The output compare action may be selected to force the pin to zero, force the pin to one, toggle the pin, or ignore the pin (used for software timing functions).

Table 16-3. TPMxSC Field Descriptions (continued)

Field	Description
4–3 CLKS[B:A]	Clock source selects. As shown in Table 16-4, this 2-bit field is used to disable the TPM system or select one of three clock sources to drive the counter prescaler. The fixed system clock source is only meaningful in systems with a PLL-based or FLL-based system clock. When there is no PLL or FLL, the fixed-system clock source is the same as the bus rate clock. The external source is synchronized to the bus clock by TPM module, and the fixed system clock source (when a PLL or FLL is present) is synchronized to the bus clock by an on-chip synchronization circuit. When a PLL or FLL is present but not enabled, the fixed-system clock source is the same as the bus-rate clock.
2–0 PS[2:0]	Prescale factor select. This 3-bit field selects one of 8 division factors for the TPM clock input as shown in Table 16-5. This prescaler is located after any clock source synchronization or clock source selection so it affects the clock source selected to drive the TPM system. The new prescale factor will affect the clock source on the next system clock cycle after the new value is updated into the register bits.

Table 16-4. TPM-Clock-Source Selection

CLKSB:CLKSA	TPM Clock Source to Prescaler Input
00	No clock selected (TPM counter disable)
01	Bus rate clock
10	Fixed system clock
11	External source

Table 16-5. Prescale Factor Selection

PS2:PS1:PS0	TPM Clock Source Divided-by
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

16.3.2 TPM-Counter Registers (TPMxCNTH:TPMxCNTL)

The two read-only TPM counter registers contain the high and low bytes of the value in the TPM counter. Reading either byte (TPMxCNTH or TPMxCNTL) latches the contents of both bytes into a buffer where they remain latched until the other half is read. This allows coherent 16-bit reads in either big-endian or little-endian order which makes this more friendly to various compiler implementations. The coherency mechanism is automatically restarted by an MCU reset or any write to the timer status/control register (TPMxSC).

(becomes unlatched) when the TPMxCnSC register is written (whether BDM mode is active or not). Any write to the channel registers will be ignored during the input capture mode.

When BDM is active, the coherency mechanism is frozen (unless reset by writing to TPMxCnSC register) such that the buffer latches remain in the state they were in when the BDM became active, even if one or both halves of the channel register are read while BDM is active. This assures that if the user was in the middle of reading a 16-bit register when BDM became active, it will read the appropriate value from the other half of the 16-bit value after returning to normal execution. The value read from the TPMxCnVH and TPMxCnVL registers in BDM mode is the value of these registers and not the value of their read buffer.

In output compare or PWM modes, writing to either byte (TPMxCnVH or TPMxCnVL) latches the value into a buffer. After both bytes are written, they are transferred as a coherent 16-bit value into the timer-channel registers according to the value of CLKSB:CLKSA bits and the selected mode, so:

- If (CLKSB:CLKSA = 0:0), then the registers are updated when the second byte is written.
- If (CLKSB:CLKSA not = 0:0 and in output compare mode) then the registers are updated after the second byte is written and on the next change of the TPM counter (end of the prescaler counting).
- If (CLKSB:CLKSA not = 0:0 and in EPWM or CPWM modes), then the registers are updated after the both bytes were written, and the TPM counter changes from (TPMxMODH:TPMxMODL - 1) to (TPMxMODH:TPMxMODL). If the TPM counter is a free-running counter then the update is made when the TPM counter changes from 0xFFFE to 0xFFFF.

The latching mechanism may be manually reset by writing to the TPMxCnSC register (whether BDM mode is active or not). This latching mechanism allows coherent 16-bit writes in either big-endian or little-endian order which is friendly to various compiler implementations.

When BDM is active, the coherency mechanism is frozen such that the buffer latches remain in the state they were in when the BDM became active even if one or both halves of the channel register are written while BDM is active. Any write to the channel registers bypasses the buffer latches and directly write to the channel register while BDM is active. The values written to the channel register while BDM is active are used for PWM & output compare operation once normal execution resumes. Writes to the channel registers while BDM is active do not interfere with partial completion of a coherency sequence. After the coherency mechanism has been fully exercised, the channel registers are updated using the buffered values written (while BDM was not active) by the user.

16.4 Functional Description

All TPM functions are associated with a central 16-bit counter which allows flexible selection of the clock source and prescale factor. There is also a 16-bit modulo register associated with the main counter.

The CPWMS control bit chooses between center-aligned PWM operation for all channels in the TPM (CPWMS=1) or general purpose timing functions (CPWMS=0) where each channel can independently be configured to operate in input capture, output compare, or edge-aligned PWM mode. The CPWMS control bit is located in the main TPM status and control register because it affects all channels within the TPM and influences the way the main counter operates. (In CPWM mode, the counter changes to an up/down mode rather than the up-counting mode used for general purpose timer functions.)

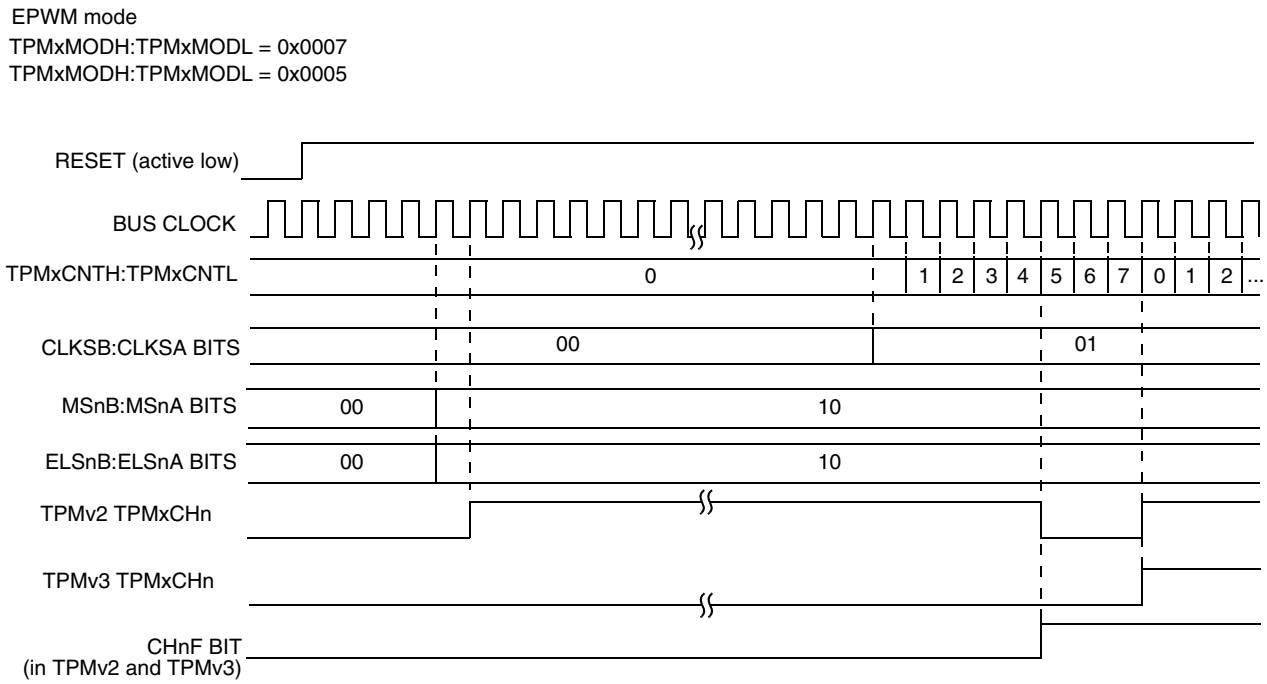


Figure 0-1. Generation of high-true EPWM signal by TPM v2 and v3 after the reset

the host must perform ((8 – CNT) – 1) dummy reads of the FIFO to advance it to the first significant entry in the FIFO.

In most trigger modes, the information stored in the FIFO consists of 16-bit change-of-flow addresses. In these cases, read DBGFH then DBGFL to get one coherent word of information out of the FIFO. Reading DBGFL (the low-order byte of the FIFO data port) causes the FIFO to shift so the next word of information is available at the FIFO data port. In the event-only trigger modes (see Section 17.3.5, “Trigger Modes”), 8-bit data information is stored into the FIFO. In these cases, the high-order half of the FIFO (DBGFH) is not used and data is read out of the FIFO by simply reading DBGFL. Each time DBGFL is read, the FIFO is shifted so the next data value is available through the FIFO data port at DBGFL.

In trigger modes where the FIFO is storing change-of-flow addresses, there is a delay between CPU addresses and the input side of the FIFO. Because of this delay, if the trigger event itself is a change-of-flow address or a change-of-flow address appears during the next two bus cycles after a trigger event starts the FIFO, it will not be saved into the FIFO. In the case of an end-trace, if the trigger event is a change-of-flow, it will be saved as the last change-of-flow entry for that debug run.

The FIFO can also be used to generate a profile of executed instruction addresses when the debugger is not armed. When ARM = 0, reading DBGFL causes the address of the most-recently fetched opcode to be saved in the FIFO. To use the profiling feature, a host debugger would read addresses out of the FIFO by reading DBGFH then DBGFL at regular periodic intervals. The first eight values would be discarded because they correspond to the eight DBGFL reads needed to initially fill the FIFO. Additional periodic reads of DBGFH and DBGFL return delayed information about executed instructions so the host debugger can develop a profile of executed instruction addresses.

17.3.3 Change-of-Flow Information

To minimize the amount of information stored in the FIFO, only information related to instructions that cause a change to the normal sequential execution of instructions is stored. With knowledge of the source and object code program stored in the target system, an external debugger system can reconstruct the path of execution through many instructions from the change-of-flow information stored in the FIFO.

For conditional branch instructions where the branch is taken (branch condition was true), the source address is stored (the address of the conditional branch opcode). Because BRA and BRN instructions are not conditional, these events do not cause change-of-flow information to be stored in the FIFO.

Indirect JMP and JSR instructions use the current contents of the H:X index register pair to determine the destination address, so the debug system stores the run-time destination address for any indirect JMP or JSR. For interrupts, RTI, or RTS, the destination address is stored in the FIFO as change-of-flow information.

17.3.4 Tag vs. Force Breakpoints and Triggers

Tagging is a term that refers to identifying an instruction opcode as it is fetched into the instruction queue, but not taking any other action until and unless that instruction is actually executed by the CPU. This distinction is important because any change-of-flow from a jump, branch, subroutine call, or interrupt causes some instructions that have been fetched into the instruction queue to be thrown away without being executed.

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2 Junction to Ambient Natural Convection

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. A-1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. A-2}$$

Solving Equation A-1 and Equation A-2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. A-3}$$

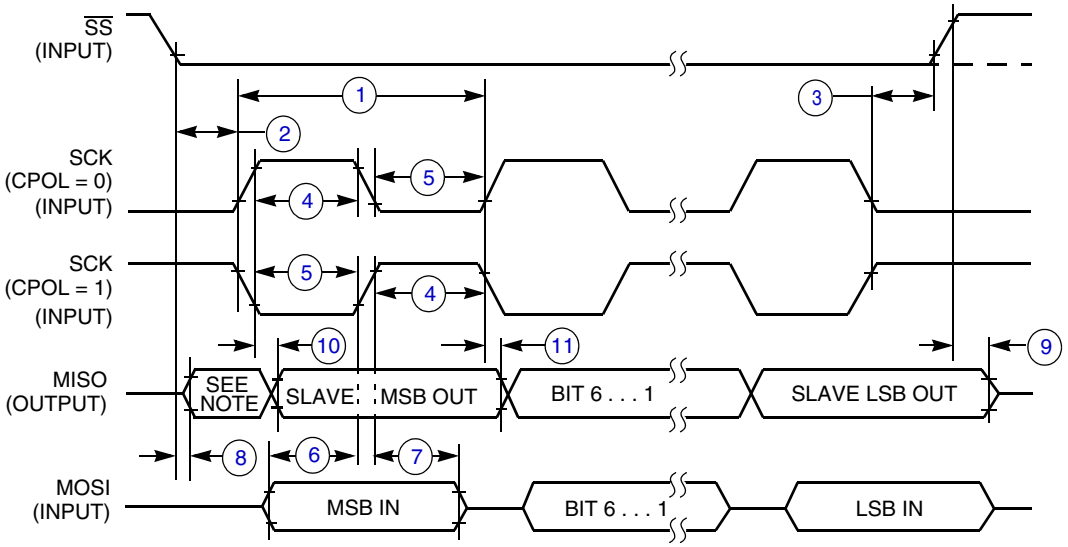
where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation A-1 and Equation A-2 iteratively for any value of T_A.

A.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.



NOTE:
1. Not defined but normally LSB of character just received

Figure A-17. SPI Slave Timing (CPHA = 1)

A.13 Flash and EEPROM Specifications

This section provides details about program/erase times and program-erase endurance for the Flash and EEPROM memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table A-16. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage for program/erase	$V_{prog/erase}$	2.7		5.5	V
2	—	Supply voltage for read operation	V_{Read}	2.7		5.5	V
3	—	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
4	—	Internal FCLK period ($1/f_{FCLK}$)	t_{Fcyc}	5		6.67	µs
5	—	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	—	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	—	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
8	—	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[3] T_L to T_H = –40°C to +125°C T = 25°C	n_{FLPE}	10,000	— 100,000	— —	cycles