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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	40KB (40K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-WFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub30f40g-a-qfn20

1. Feature List

The EFM8UB3 highlighted features are listed below.

- **High-speed CIP-51 MCU Core**
  - Pipelined instruction architecture; executes 70% of instruction set in 1 or 2 system clocks
  - Up to 48 MIPS throughput with 48 MHz clock
  - Uses standard 8051 instruction set
  - Expanded interrupt handler
- **Memory**
  - 40 KB Flash
  - Flash is in-system programmable in 512-byte sectors
  - 3328 bytes RAM, including:
    - 256 bytes standard 8051 RAM
    - 2048 bytes on-chip XRAM
    - 1024 bytes of USB buffer
- **On-chip Debug**
  - On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
  - Provides 4 hardware breakpoints, single stepping, inspect/modify memory and registers
- **12-bit Analog-to-Digital Converter**
  - Multiple selectable inputs
  - Up to 800 ksps 10-bit mode
  - Precise Internal VREF 1.65 V or external VREF supported
- **Clock Sources**
  - 48 MHz ± 1.5% precision internal oscillator and ±0.25% using USB clock recovery
  - 24.5 MHz low power internal oscillator with ±2% accuracy
  - 80 kHz low-frequency, low power internal oscillator (LFO)
  - External CMOS clock option
  - Flexible clock divider: Reduce frequency by up to 128x from any clock source
- **2 x Analog Comparators**
  - Multiplexed selectable inputs
  - Integrated 6-bit programmable reference voltage selectable as comparator input channel
  - Programmable hysteresis and response time
  - 400 nA current consumption in low power mode
- **Power Management**
  - 5 V-input LDO regulator for direct connection to USB supply
    - External LDO is needed for USB-C VBUS powered applications that require more than 5 V.
  - Internal low dropout (LDO) regulator for CPU core voltage
  - Power-on reset and brownout detect circuit
  - Multiple power modes supported to minimize power consumption while maintaining performance
- **General-Purpose I/O**
  - Up to 17 pins
  - V_{IO} + 2.5 V tolerant; push-pull or open-drain
  - Priority crossbar to support flexible digital peripheral pin assignments
- **Timers/Counters/PWM**
  - 6 general purpose 16-bit counters/timers
  - 16-bit Programmable Counter Array (PCA) with 3 channels of PWM, capture/compare, or frequency output capability, and hardware kill/safe state capability
  - Independent watchdog timer, clocked from the low frequency oscillator
- **Communication Interfaces and Digital Peripherals**
  - UART, up to 3 Mbaud
  - SMBus (1 Mbps)
  - USB 2.0-compliant full speed with integrated low-power transceiver, 4 bidirectional endpoints and dedicated 1024-byte buffer
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- **Single Voltage Supply**
  - (VREGIN shorted to VDD): 2.3 to 3.6 V
  - (VREGIN not shorted to VDD): 2.7 to 5.25 V
- **Pre-loaded USB Bootloader**
- **Package Options: QFN20, QFN24, QSOP24**
- **Temperature Range: -40 to +85 °C**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8UB3 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Devices are available in 20-pin QFN, 24-pin QFN, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

3.6 Communications and Other Digital Peripherals

Universal Serial Bus (USB0)

The USB0 peripheral provides a full-speed USB 2.0 compliant device controller and PHY with additional Low Energy USB features. The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation, and includes a dedicated USB oscillator with clock recovery mechanism for crystal-free operation. No external components are required. The USB function controller (USB0) consists of a Serial Interface Engine (SIE), USB transceiver (including matching resistors and configurable pull-up resistors), and 1 KB FIFO block. The Low Energy Mode ensures the current consumption is optimized and enables USB communication on a strict power budget.

The USB0 module includes the following features:

- Full and Low Speed functionality.
- Implements 4 bidirectional endpoints.
- Low Energy Mode to reduce active supply current based on bus bandwidth.
- USB 2.0 compliant USB peripheral support (no host capability).
- Direct module access to 1 KB of RAM for FIFO memory.
- Clock recovery to meet USB clocking requirements with no external components.
- Charger detection circuitry with automatic detection of SDP, CDP, and DCP interfaces.
- D+ and D- can be routed to ADC input to support ACM and proprietary charger architectures.

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions.
- Dedicated baud rate generator supports baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 5, 6, 7, 8, or 9 bit data.
- Automatic start and stop generation.
- Automatic parity generation and checking.
- Four byte FIFO on transmit and receive.
- Auto-baud detection.
- LIN break and sync field detection.
- CTS / RTS hardware flow control.

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes.
- Supports external clock frequencies up to 12 Mbps in master or slave mode.
- Support for all clock phase and polarity modes.
- 8-bit programmable clock rate (master).
- Programmable receive timeout (slave).
- Two byte FIFO on transmit and receive.
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte.
- Support for multiple masters on the same data lines.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in 4.1.1 Recommended Operating Conditions, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD [1]	V_{DD}		2.3 [1]	—	3.6	V
Operating Supply Voltage on VIO [3, 4]	V_{IO}		1.71	—	V_{DD}	V
Operating Supply Voltage on VREGIN [1]	V_{REGIN}		3.0 [1]	—	5.5	V
System Clock Frequency	f_{SYSCLK}		0	—	48	MHz
Operating Ambient Temperature	T_A		-40	—	85	°C

Note:

1. Standard USB compliance tests require 3.0 V on VDD for compliant operation. If using the internal regulator to supply this voltage on VDD, the minimum regulator input voltage is 3.7 V.
2. All voltages with respect to GND.
3. On devices without a VIO pin, $V_{IO} = V_{DD}$.
4. GPIO levels are undefined whenever VIO is less than 1 V.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Always-on [4]	I_{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V_{DD} = 3.0 V	—	850	1085	µA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V_{DD} = 3.0 V	—	420	545	µA
ADC0 Burst Mode, 10-bit single conversions, external reference	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	385	—	µA
		100 ksps, V_{DD} = 3.0 V	—	193	—	µA
		10 ksps, V_{DD} = 3.0 V	—	20	—	µA
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	495	—	µA
		100 ksps, V_{DD} = 3.0 V	—	250	—	µA
		10 ksps, V_{DD} = 3.0 V	—	25.5	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V	—	520	—	µA
		50 ksps, V_{DD} = 3.0 V	—	260	—	µA
		10 ksps, V_{DD} = 3.0 V	—	53	—	µA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V, Normal bias	—	970	—	µA
		50 ksps, V_{DD} = 3.0 V, Low power bias	—	425	—	µA
		10 ksps, V_{DD} = 3.0 V, Low power bias	—	86	—	µA
Internal ADC0 Reference, Always-on [5]	I_{VREFFS}	Normal Power Mode	—	690	765	µA
		Low Power Mode	—	166	195	µA
Temperature Sensor	I_{TSENSE}		—	68	110	µA
Comparator 0 (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	µA
		CPMD = 10	—	3	—	µA
		CPMD = 01	—	9.1	—	µA
		CPMD = 00	—	24.2	—	µA
Comparator Reference[6]	I_{CPREF}		—	25.3	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	14	20	µA

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1, 2]	t_{WRITE}	One Byte, F_{SYSCLK} = 24.5 MHz	19	20	21	µs
Erase Time[1, 2]	t_{ERASE}	One Page, F_{SYSCLK} = 24.5 MHz	5.2	5.35	5.5	ms
V_{DD} Voltage During Programming [3]	V_{PROG}	5 V Voltage Regulator used	2.7	—	5.5	V
		5 V Voltage Regulator bypassed	2.3	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
CRC Calculation Time	t_{CRC}	One 256-Byte Block SYSCLK = 48 MHz	—	5.5	—	µs

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{SUSPENDWK}$	SYSCLK = HFOSC0 CLKDIV = 0x00	—	170	—	ns
Snooze Mode Wake-up Time	$t_{SLEEPWK}$	SYSCLK = HFOSC0 CLKDIV = 0x00	—	12	—	µs

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	PSS_{HFOSC0}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{HFOSC0}	V_{DD} = 3.0 V	—	40	—	ppm/°C
High Frequency Oscillator 1 (48 MHz)						
Oscillator Frequency	f_{HFOSC1}	Full Temperature and Supply Range	47.3	48	48.7	MHz
Power Supply Sensitivity	PSS_{HFOSC1}	T_A = 25 °C	—	0.02	—	%/V
Temperature Sensitivity	TS_{HFOSC1}	V_{DD} = 3.0 V	—	45	—	ppm/°C
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{DD} = 3.0 V	—	65	—	ppm/°C

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	48	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

4.1.14 Configurable Logic

Table 4.14. Configurable Logic

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay through LUT	t_{DLY_LUT}	Through single CLU Using an external pin	—	—	38.7	ns
		Through single CLU Using an internal connection	—	1.6	5.0	ns
Propagation Delay through D flip-flop clock	t_{DLY_DFF}	Through single CLU Using an external pin	—	—	38.7	ns
		Through single CLU Using an internal connection	—	1.4	5.6	ns
Clocking Frequency	F_{CLK}	1 or 2 CLUs Cascaded	—	—	48	MHz
		3 or 4 CLUs Cascaded	—	—	48	MHz

4.1.17 SMBus

Table 4.17. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	70[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	µs
Data Hold Time	$t_{HD:DAT}$		275[3]	—	—	ns
Data Setup Time	$t_{SU:DAT}$		300[3]	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	µs
Clock High Period	t_{HIGH}		9.4	—	50[4]	µs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	255[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	255[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	µs
Data Hold Time	$t_{HD:DAT}$		275[3]	—	—	ns
Data Setup Time	$t_{SU:DAT}$		300[3]	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	µs
Clock High Period	t_{HIGH}		2.6	—	50[4]	µs
Fast Mode Plus (1 MHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	666[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	666[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.67	—	—	µs

4.3 Absolute Maximum Ratings

Stresses above those listed in 4.3 Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.20. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		-55	125	°C
Storage Temperature	T_{STG}		-65	150	°C
Voltage on VDD	V_{DD}		GND-0.3	4.2	V
Voltage on VIO[2]	V_{IO}		GND-0.3	4.2	V
Voltage on VREGIN	V_{REGIN}		GND-0.3	5.8	V
Voltage on D+ or D-[2]	V_{USBD}		GND-0.3	V_{DD}+0.3	V
Voltage on I/O pins (including VBUS / P2.1) or RSTb[2]	V_{IN}	V_{IO} > 3.3 V	GND-0.3	5.8	V
		V_{IO} < 3.3 V	GND-0.3	V_{IO}+2.5	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I_{IO}		-100	100	mA
Operating Junction Temperature	T_J		-40	105	°C

Note:
1. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. On devices without a VIO pin, $V_{IO} = V_{DD}$.

5. Typical Connection Diagrams

5.1 Power

The figure below shows a typical connection diagram for the power pins of the EFM8UB3 devices when the internal regulator used and USB is connected (bus-powered).

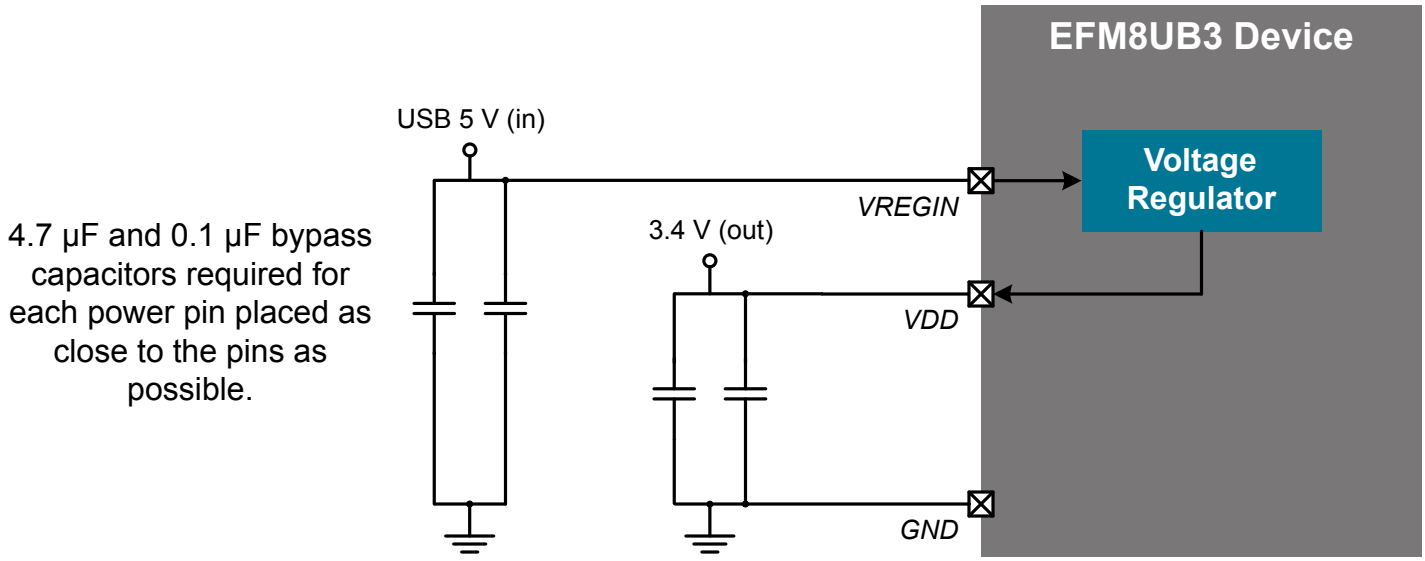

Figure 5.1. Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered)

Table 6.1. Pin Definitions for EFM8UB3x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU2B.7 CLU3B.6 CLU0OUT	ADC0.2 CMP0P.2 CMP0N.2
2	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1 CLU0A.6 CLU3A.7	ADC0.1 CMP0P.1 CMP0N.1 AGND
3	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
4	GND	Ground			ADC0.19
5	D+	USB Data Positive			ADC0.28
6	D-	USB Data Negative			ADC0.29
7	VIO	I/O Power Input			
8	VDD	Supply Power Input / 5V Regulator Output			ADC0.18
9	VREGIN	5V Regulator Input			
10	P2.1	Multifunction I/O		VBUS	ADC0.24 CMP1P.13 CMP1N.13
11	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
12	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
13	P1.6	Multifunction I/O	Yes	CLU0A.7	ADC0.14 CMP1P.6 CMP1N.6

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
12	P1.5	Multifunction I/O	Yes		ADC0.13 CMP1P.5 CMP1N.5
15	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
16	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
17	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2
18	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1
19	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0B.6 CLU2A.7 CLU3OUT	ADC0.8 CMP1P.0 CMP1N.0
20	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1A.7 CLU3A.6	ADC0.7 CMP0P.7 CMP0N.7
21	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU1B.6 CLU2OUT	ADC0.6 CMP0P.6 CMP0N.6
22	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART1_RX CLU1B.7 CLU2A.6	ADC0.5 CMP0P.5 CMP0N.5

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
23	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 CLU0B.7 CLU2B.6 CLU1OUT UART1_TX	ADC0.4 CMP0P.4 CMP0N.4
24	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU1A.6 CLU3B.7	ADC0.3 CMP0P.3 CMP0N.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
3	GND	Ground			ADC0.19
4	D+	USB Data Positive			ADC0.28
5	D-	USB Data Negative			ADC0.29
6	VDD	Supply Power Input / 5V Regulator Output			ADC0.18
7	VREGIN	5V Regulator Input			
8	P2.1	Multifunction I/O		VBUS	ADC0.24 CMP1P.13 CMP1N.13
9	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
10	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
11	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2
12	GND	Ground			
13	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1
14	P1.0	Multifunction I/O	Yes	P1MAT.0 CLU0B.6 CLU2A.7 CLU3OUT	ADC0.8 CMP1P.0 CMP1N.0
15	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7 CLU1A.7 CLU3A.6	ADC0.7 CMP0P.7 CMP0N.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
16	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU1B.6 CLU2OUT	ADC0.6 CMP0P.6 CMP0N.6
17	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART1_RX CLU1B.7 CLU2A.6	ADC0.5 CMP0P.5 CMP0N.5
18	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 CLU0B.7 CLU2B.6 CLU1OUT UART1_TX	ADC0.4 CMP0P.4 CMP0N.4
19	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU1A.6 CLU3B.7	ADC0.3 CMP0P.3 CMP0N.3
20	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU2B.7 CLU3B.6 CLU0OUT	ADC0.2 CMP0P.2 CMP0N.2
Center	GND	Ground			

7. QFN24 Package Specifications

7.1 QFN24 Package Dimensions

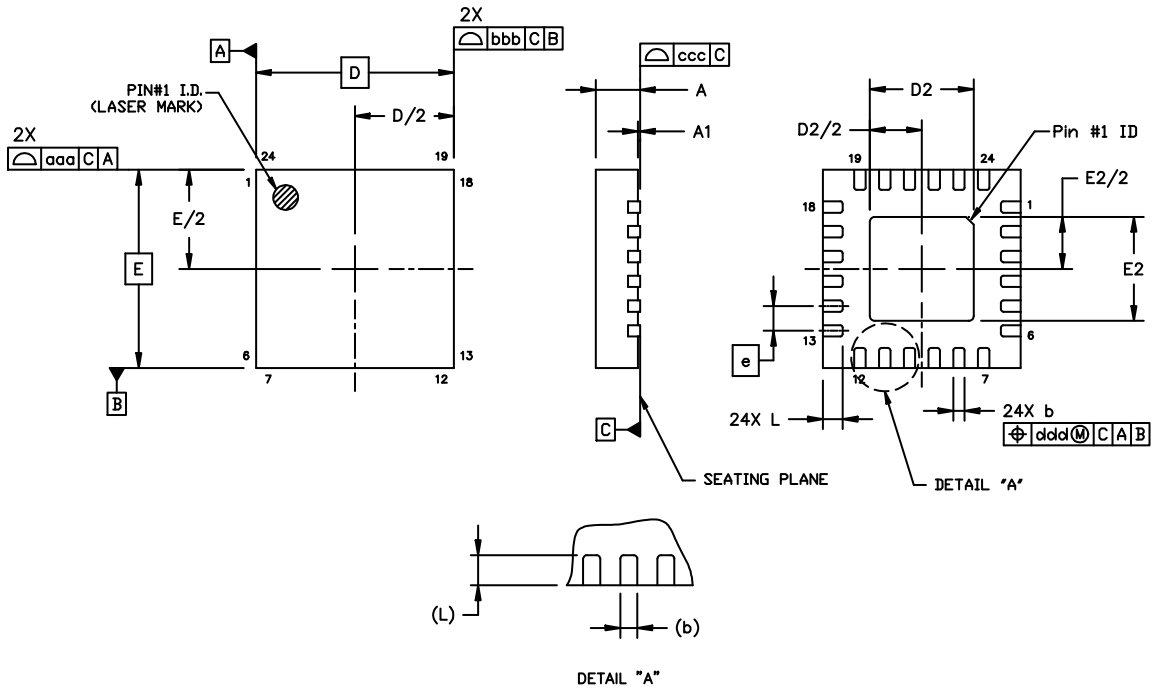

Figure 7.1. QFN24 Package Drawing

Table 7.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.35	2.45	2.55
e		0.50 BSC	
E		4.00 BSC	
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

7.2 PCB Land Pattern

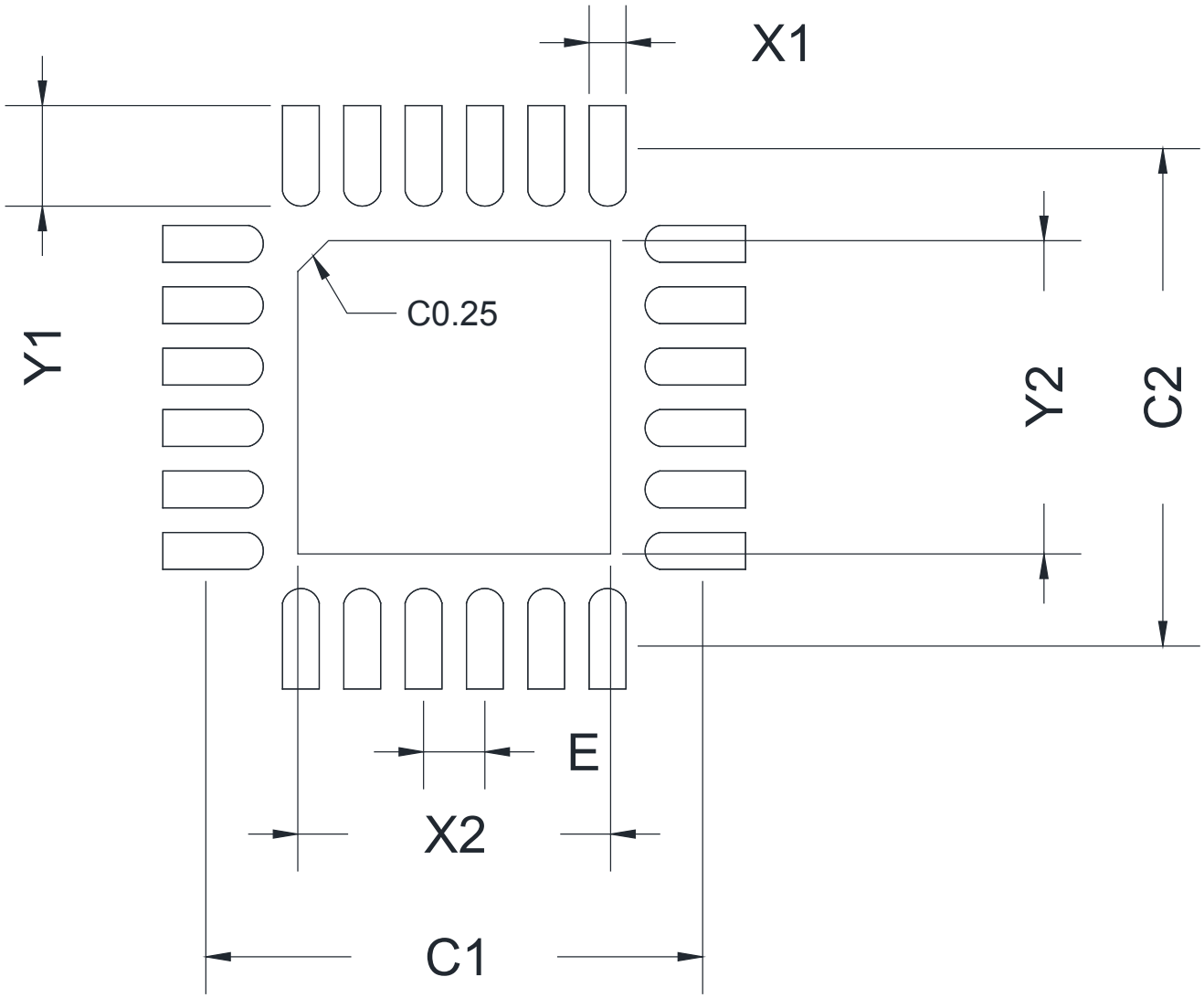

Figure 7.2. PCB Land Pattern Drawing

Table 7.2. PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.90	
C2	3.90	
E	0.50	
X1	0.30	
X2	2.55	
Y1	0.85	
Y2	2.55	

9. QFN20 Package Specifications

9.1 QFN20 Package Dimensions

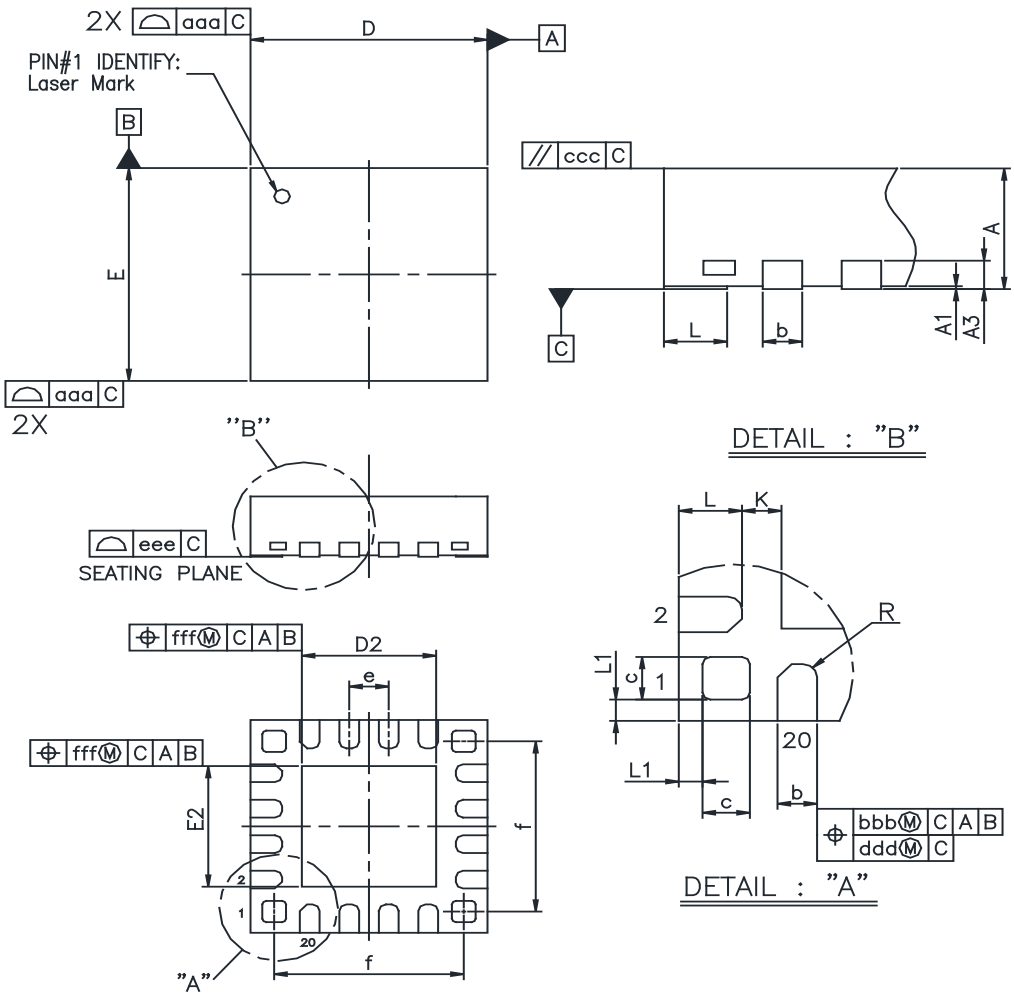

Figure 9.1. QFN20 Package Drawing

Table 9.1. QFN20 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
c	0.25	0.30	0.35
D		3.00 BSC	
D2	1.6	1.70	1.80
e		0.50 BSC	
E		3.00 BSC	

Dimension	Min	Typ	Max
E2	1.60	1.70	1.80
f		2.50 BSC	
L	0.30	0.40	0.50
K		0.25 REF	
R	0.09	0.125	0.15
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. The drawing complies with JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2 QFN20 PCB Land Pattern

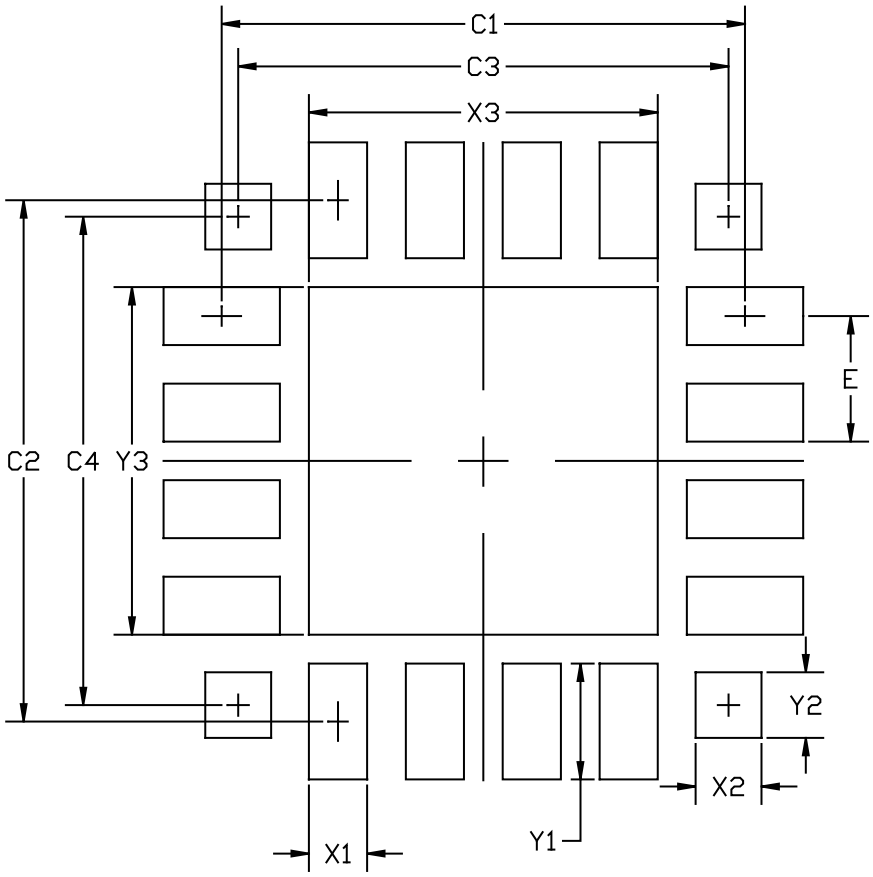

Figure 9.2. QFN20 PCB Land Pattern Drawing

Table 9.2. QFN20 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.10	
C2	3.10	
C3	2.50	
C4	2.50	
E	0.50	
X1	0.30	
X2	0.25	0.35
X3	1.80	
Y1	0.90	
Y2	0.25	0.35
Y3	1.80	