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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	13
Program Memory Size	40KB (40K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-WFQFN Exposed Pad
Supplier Device Package	20-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub30f40g-a-qfn20r

3.2 Power

Control over the device power consumption can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	• Core and peripheral clocks halted • HFOSC0 and HFOSC1 oscillators stopped • Regulators in normal bias mode for fast wake • Timer 3 and 4 may clock from LFOSC0 • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SUSPEND bit in PCON1	• USB0 Bus Activity • Timer 4 Event • SPI0 Activity • Port Match Event • Comparator 0 Falling Edge • CLUn Interrupt-Enabled Event
Stop	• All internal power nets shut down • 5V regulator remains active (if enabled) • Internal 1.8 V LDO on • Pins retain state • Exit on any reset source	1. Clear STOPCF bit in REG0CN 2. Set STOP bit in PCON0	Any reset source
Snooze	• Core and peripheral clocks halted • HFOSC0 and HFOSC1 oscillators stopped • Regulators in low bias current mode for energy savings • Timer 3 and 4 may clock from LFOSC0 • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SNOOZE bit in PCON1	• USB0 Bus Activity • Timer 4 Event • SPI0 Activity • Port Match Event • Comparator 0 Falling Edge • CLUn Interrupt-Enabled Event
Shutdown	• All internal power nets shut down • 5V regulator remains active (if enabled) • Internal 1.8 V LDO off to save energy • Pins retain state • Exit on pin or power-on reset	1. Set STOPCF bit in REG0CN 2. Set STOP bit in PCON0	• RSTb pin reset • Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P1.6 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.0 and P2.1 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.0.

The port control block offers the following features:

- Up to 17 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 17 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.6 Communications and Other Digital Peripherals

Universal Serial Bus (USB0)

The USB0 peripheral provides a full-speed USB 2.0 compliant device controller and PHY with additional Low Energy USB features. The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation, and includes a dedicated USB oscillator with clock recovery mechanism for crystal-free operation. No external components are required. The USB function controller (USB0) consists of a Serial Interface Engine (SIE), USB transceiver (including matching resistors and configurable pull-up resistors), and 1 KB FIFO block. The Low Energy Mode ensures the current consumption is optimized and enables USB communication on a strict power budget.

The USB0 module includes the following features:

- Full and Low Speed functionality.
- Implements 4 bidirectional endpoints.
- Low Energy Mode to reduce active supply current based on bus bandwidth.
- USB 2.0 compliant USB peripheral support (no host capability).
- Direct module access to 1 KB of RAM for FIFO memory.
- Clock recovery to meet USB clocking requirements with no external components.
- Charger detection circuitry with automatic detection of SDP, CDP, and DCP interfaces.
- D+ and D- can be routed to ADC input to support ACM and proprietary charger architectures.

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions.
- Dedicated baud rate generator supports baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 5, 6, 7, 8, or 9 bit data.
- Automatic start and stop generation.
- Automatic parity generation and checking.
- Four byte FIFO on transmit and receive.
- Auto-baud detection.
- LIN break and sync field detection.
- CTS / RTS hardware flow control.

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes.
- Supports external clock frequencies up to 12 Mbps in master or slave mode.
- Support for all clock phase and polarity modes.
- 8-bit programmable clock rate (master).
- Programmable receive timeout (slave).
- Two byte FIFO on transmit and receive.
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte.
- Support for multiple masters on the same data lines.

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset
- USB reset

3.9 Debugging

The EFM8UB3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3.10 Bootloader

All devices come pre-programmed with a USB bootloader. This bootloader resides in the code security page and last pages of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio in the [**Documentation**] area.

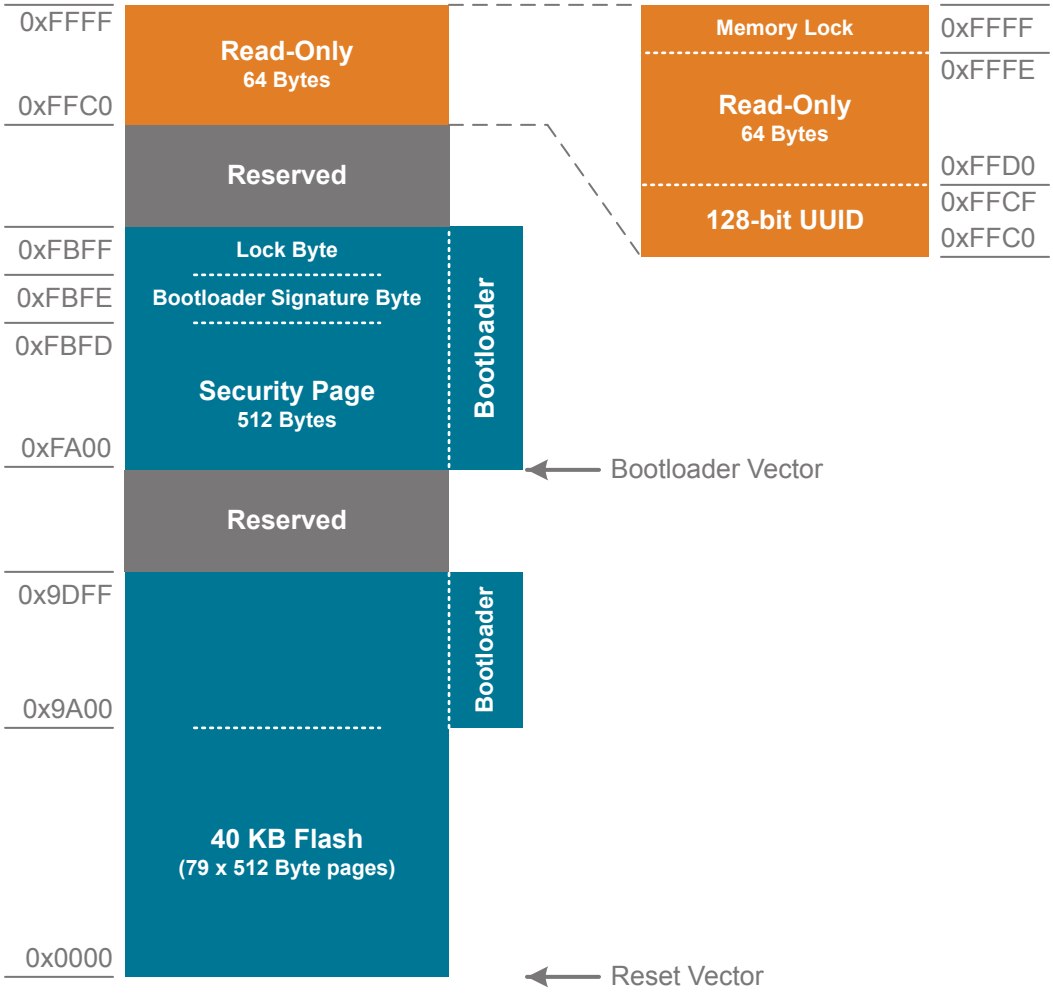

Figure 3.2. Flash Memory Map with Bootloader—40 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
USB	VBUS
	D+
	D-

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in 4.1.1 Recommended Operating Conditions, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD [1]	V_{DD}		2.3 [1]	—	3.6	V
Operating Supply Voltage on VIO [3, 4]	V_{IO}		1.71	—	V_{DD}	V
Operating Supply Voltage on VREGIN [1]	V_{REGIN}		3.0 [1]	—	5.5	V
System Clock Frequency	f_{SYSCLK}		0	—	48	MHz
Operating Ambient Temperature	T_A		-40	—	85	°C

Note:

1. Standard USB compliance tests require 3.0 V on VDD for compliant operation. If using the internal regulator to supply this voltage on VDD, the minimum regulator input voltage is 3.7 V.
2. All voltages with respect to GND.
3. On devices without a VIO pin, $V_{IO} = V_{DD}$.
4. GPIO levels are undefined whenever VIO is less than 1 V.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode-Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 48 MHz (HFOSC1) [2]	—	9.6	10.5	mA
		F_{SYSCLK} = 24.5 MHz (HFOSC0) [2]	—	4.6	5.3	mA
		F_{SYSCLK} = 1.53 MHz (HFOSC0) [2]	—	616	—	µA
		F_{SYSCLK} = 80 kHz [3]	—	131	—	µA
Idle Mode-Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 48 MHz (HFOSC1) [2]	—	7.1	7.8	mA
		F_{SYSCLK} = 24.5 MHz (HFOSC0) [2]	—	3.4	3.9	mA
		F_{SYSCLK} = 1.53 MHz (HFOSC0) [2]	—	550	—	µA
		F_{SYSCLK} = 80 kHz [3]	—	139	—	µA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I_{DD}	LFO Running	—	125	—	µA
		LFO Stopped	—	120	—	µA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I_{DD}	LFO Running	—	25	—	µA
		LFO Stopped	—	20	—	µA
Stop Mode—Core halted and all clocks stopped,Internal LDO On, Supply monitor off.	I_{DD}		—	120	—	µA
Shutdown Mode—Core halted and all clocks stopped,Internal LDO Off, Supply monitor off.	I_{DD}		—	0.35	—	µA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I_{HFOSC0}	Operating at 24.5 MHz, T_A = 25 °C	—	122	—	µA
High-Frequency Oscillator 1	I_{HFOSC1}	Operating at 48 MHz, T_A = 25 °C	—	910	—	µA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, T_A = 25 °C	—	4.2	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Always-on [4]	I_{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V_{DD} = 3.0 V	—	850	1085	µA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V_{DD} = 3.0 V	—	420	545	µA
ADC0 Burst Mode, 10-bit single conversions, external reference	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	385	—	µA
		100 ksps, V_{DD} = 3.0 V	—	193	—	µA
		10 ksps, V_{DD} = 3.0 V	—	20	—	µA
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, V_{DD} = 3.0 V	—	495	—	µA
		100 ksps, V_{DD} = 3.0 V	—	250	—	µA
		10 ksps, V_{DD} = 3.0 V	—	25.5	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V	—	520	—	µA
		50 ksps, V_{DD} = 3.0 V	—	260	—	µA
		10 ksps, V_{DD} = 3.0 V	—	53	—	µA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, V_{DD} = 3.0 V, Normal bias	—	970	—	µA
		50 ksps, V_{DD} = 3.0 V, Low power bias	—	425	—	µA
		10 ksps, V_{DD} = 3.0 V, Low power bias	—	86	—	µA
Internal ADC0 Reference, Always-on [5]	I_{VREFFS}	Normal Power Mode	—	690	765	µA
		Low Power Mode	—	166	195	µA
Temperature Sensor	I_{TSENSE}		—	68	110	µA
Comparator 0 (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	µA
		CPMD = 10	—	3	—	µA
		CPMD = 01	—	9.1	—	µA
		CPMD = 00	—	24.2	—	µA
Comparator Reference[6]	I_{CPREF}		—	25.3	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	14	20	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5V Regulator	I_{VREG}	Normal Mode (SUSEN = 0, BIASENB = 0)	—	260	375	µA
		Suspend Mode (SUSEN = 1, BIASENB = 0)	—	67	123	µA
		Bias Disabled (BIASENB = 1)	—	1.8	16	µA
		Disabled (BIASENB = 1, REG1ENB = 1)	—	2.5	—	nA
USB (USB0) Full-Speed	I_{USB}	Low Energy Mode, 64 byte 1ms IN Interrupt transfers	—	850	—	µA
		Low Energy Mode, 64 byte 1ms OUT Interrupt transfers	—	250	—	µA
		Low Energy Mode, Idle (SOF only)	—	50	—	µA

Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.
6. This value is the current sourced from the pin or supply selected as the full-scale reference to the comparator DAC.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		2.16	2.23	2.29	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.2	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to V_{DD} > 2.3 V	10	—	—	µs
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	50	—	µs
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{SYSCLK} >1 MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	PSS_{HFOSC0}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{HFOSC0}	V_{DD} = 3.0 V	—	40	—	ppm/°C
High Frequency Oscillator 1 (48 MHz)						
Oscillator Frequency	f_{HFOSC1}	Full Temperature and Supply Range	47.3	48	48.7	MHz
Power Supply Sensitivity	PSS_{HFOSC1}	T_A = 25 °C	—	0.02	—	%/V
Temperature Sensitivity	TS_{HFOSC1}	V_{DD} = 3.0 V	—	45	—	ppm/°C
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{DD} = 3.0 V	—	65	—	ppm/°C

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	48	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns

4.1.8 ADC

Table 4.8. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	200	ksps
		10 Bit Mode	—	—	800	ksps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t_{PWR}		1.2	—	—	µs
SAR Clock Frequency	f_{SAR}	High Speed Mode, Reference is 2.4 V internal	—	—	6.25	MHz
		High Speed Mode, Reference is not 2.4 V internal	—	—	12.5	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 12.25 MHz, System Clock = 24.5 MHz.		1.1		µs
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}		—	20	—	pF
Input Mux Impedance	R_{MUX}		—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range [1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±2.3	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	-1	±0.7	1.9	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Offset Error	E_{OFF}	12 Bit Mode, VREF = 1.65 V	-3	0	3	LSB
		10 Bit Mode, VREF = 1.65 V	-2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C

4.1.15 Port I/O

Table 4.15. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	V_{OH}	I_{OH} = -7 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -3.3 mA, 2.3 V ≤ V_{IO} < 3.0 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (High Drive)	V_{OL}	I_{OL} = 13.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 7 mA, 2.3 V ≤ V_{IO} < 3.0 V	—	—	V_{IO} x 0.2	V
Output High Voltage (Low Drive)	V_{OH}	I_{OH} = -4.75 mA, V_{IO} ≥ 3.0 V	V_{IO} - 0.7	—	—	V
		I_{OH} = -2.25 mA, 2.3 V ≤ V_{IO} < 3.0 V	V_{IO} x 0.8	—	—	V
Output Low Voltage (Low Drive)	V_{OL}	I_{OL} = 6.5 mA, V_{IO} ≥ 3.0 V	—	—	0.6	V
		I_{OL} = 3.5 mA, 2.3 V ≤ V_{IO} < 3.0 V	—	—	V_{IO} x 0.2	V
Input High Voltage (all port pins including VBUS)	V_{IH}		0.7 x V_{IO}	—	—	V
Input Low Voltage (all port pins including VBUS)	V_{IL}		—	—	0.3 x V_{IO}	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{IO} = 3.6	-30	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND < V_{IN} < V_{IO}	-1.1	—	1.1	µA
Input Leakage Current with V_{IN} above V_{IO}	I_{LK}	V_{IO} < V_{IN} < V_{IO}+2.0 V	0	5	60	µA

Note:
1. On devices without a VIO pin, V_{IO} = V_{DD}.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		0.33	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		0.67	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		0.67	—	—	µs
Data Hold Time	$t_{HD:DAT}$		275[3]	—	—	ns
Data Setup Time	$t_{SU:DAT}$		300[3]	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		0.33	—	—	µs
Clock High Period	t_{HIGH}		0.67	—	50[4]	µs

Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications. The maximum frequency cannot be achieved with all combinations of oscillators and dividers available, but the effective frequency must not exceed 256 kHz.
3. Data setup and hold timing at 40 MHz or lower with EXTHOLD set to 1.
4. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.

Table 4.18. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	f_{CSO} / 3
Bus Free Time Between STOP and START Conditions	t_{BUF}	2 / f_{CSO}
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	1 / f_{CSO}
Repeated START Condition Setup Time	$t_{SU:STA}$	2 / f_{CSO}
STOP Condition Setup Time	$t_{SU:STO}$	2 / f_{CSO}
Clock Low Period	t_{LOW}	1 / f_{CSO}
Clock High Period	t_{HIGH}	2 / f_{CSO}

Note:
1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

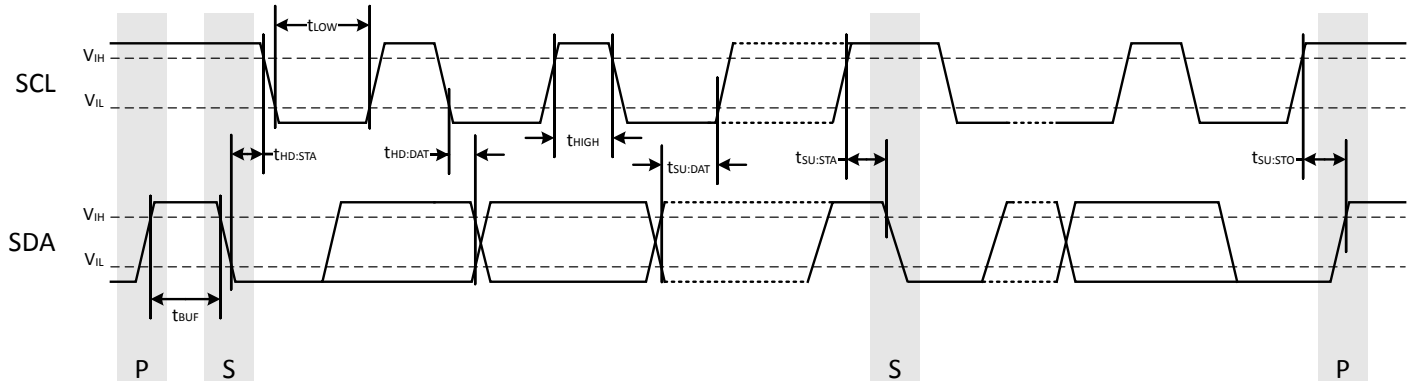

Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.19. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFN20 Packages	—	60	—	°C/W
		QFN24 Packages	—	30	—	°C/W
		QSOP24 Packages	—	65	—	°C/W
		QFN32 Packages	—	26	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

5.2 USB

Figure 5.4 Bus-Powered Connection Diagram for USB Pins on page 35 shows a typical connection bus-powered diagram for the USB pins of the EFM8UB3 devices including ESD protection diodes on the USB pins. Bypass capacitors on VREGIN and VDD are required as discussed in 5.1 Power, but are not shown in the figure.

Note: The VBUS pin is not required as a sensing pin for proper operation in bus-powered configurations. Rather than using VBUS as a sensing pin, it is recommended to use the VBUS pin only as a GPIO by clearing VBUSEN and VBUSIE to 0 in the USB0CF register. To do this using the USB stack, set the device to use bus-powered mode.

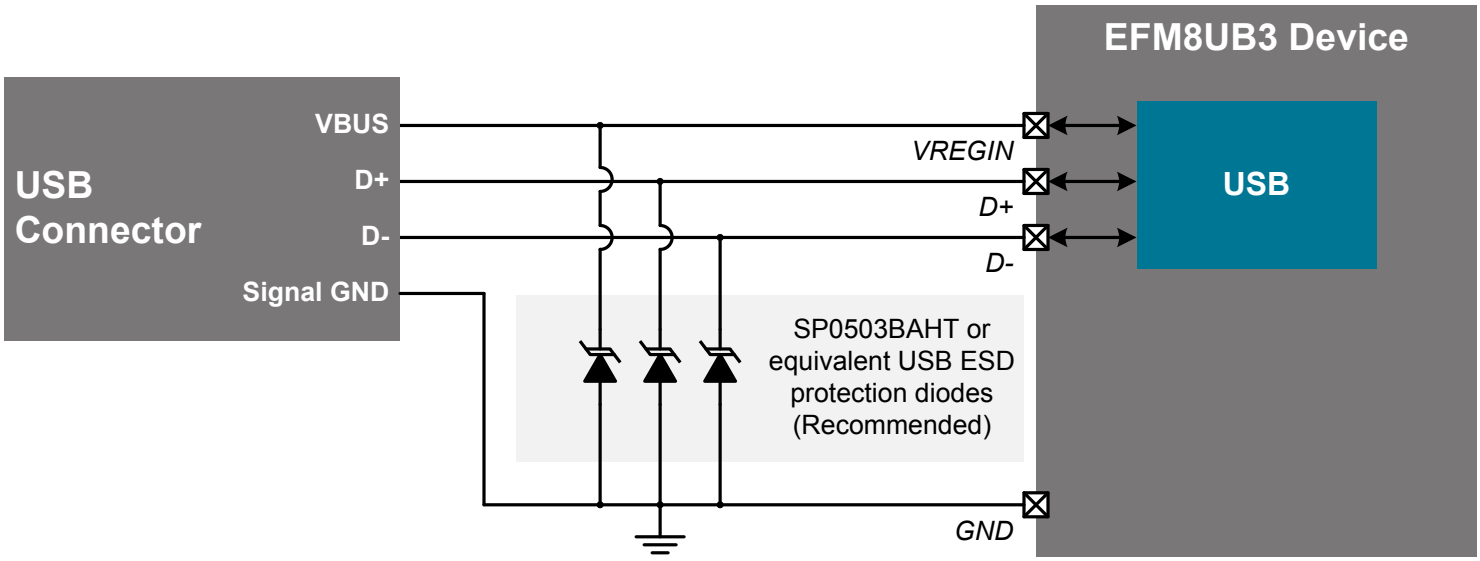

Figure 5.4. Bus-Powered Connection Diagram for USB Pins

5.3 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in *AN124: Pin Sharing Techniques for the C2 Interface*. Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.

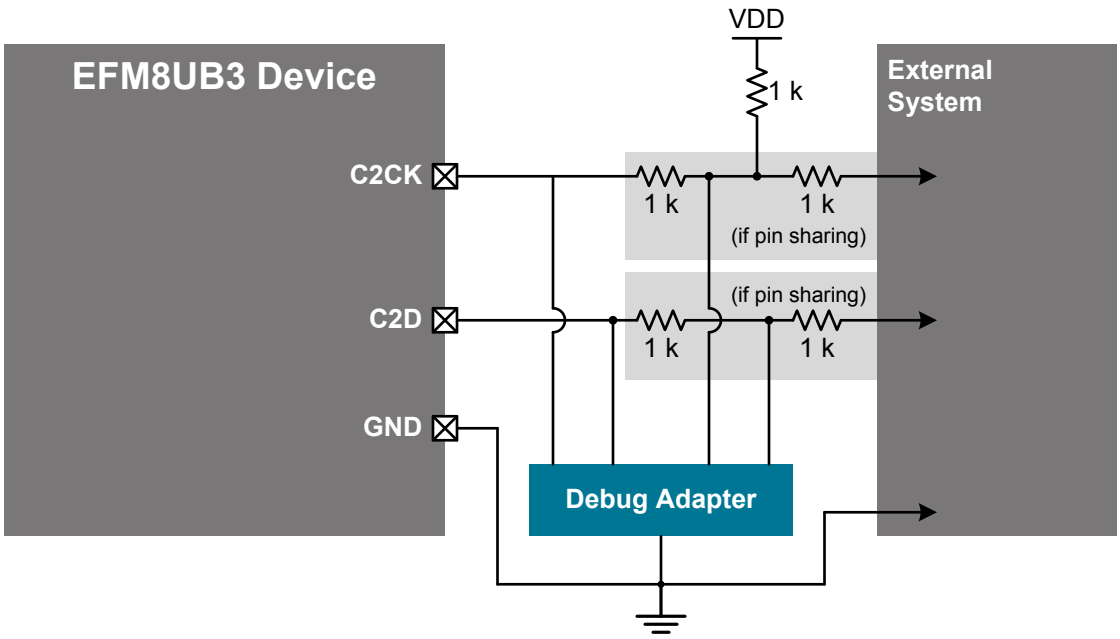

Figure 5.6. Debug Connection Diagram

5.4 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note *AN203: 8-bit MCU Printed Circuit Board Design Notes* contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
16	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6 CLU1B.6 CLU2OUT	ADC0.6 CMP0P.6 CMP0N.6
17	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5 UART1_RX CLU1B.7 CLU2A.6	ADC0.5 CMP0P.5 CMP0N.5
18	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4 CLU0B.7 CLU2B.6 CLU1OUT UART1_TX	ADC0.4 CMP0P.4 CMP0N.4
19	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3 CLU1A.6 CLU3B.7	ADC0.3 CMP0P.3 CMP0N.3
20	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2 CLU2B.7 CLU3B.6 CLU0OUT	ADC0.2 CMP0P.2 CMP0N.2
Center	GND	Ground			

7. QFN24 Package Specifications

7.1 QFN24 Package Dimensions

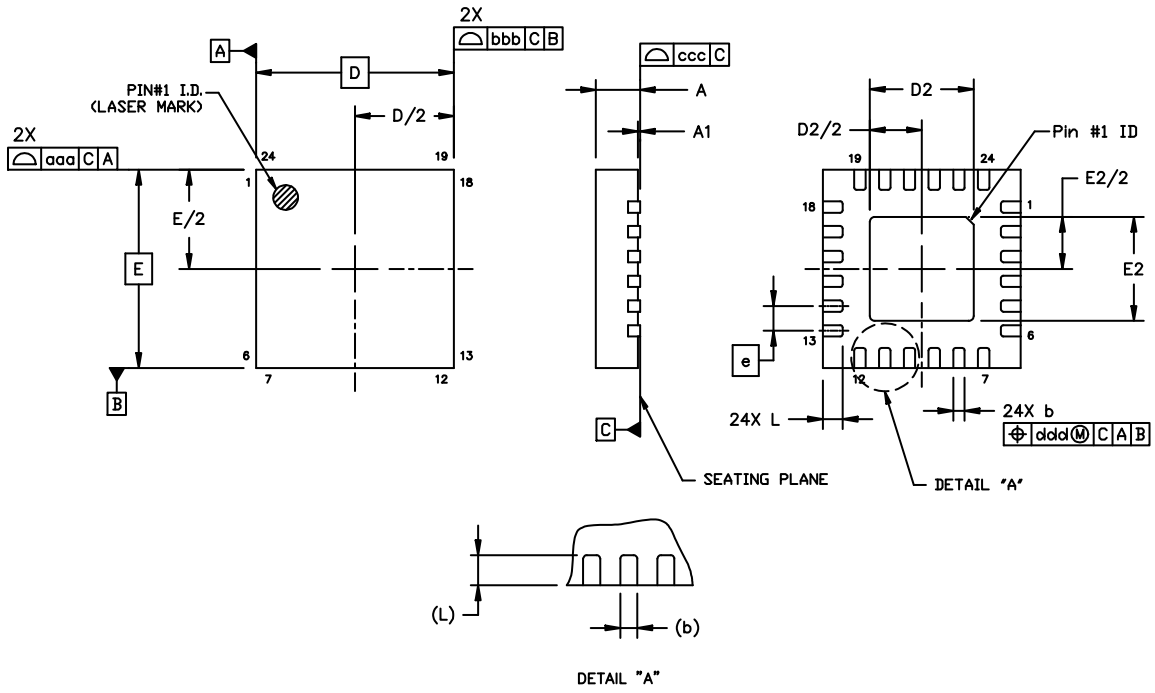

Figure 7.1. QFN24 Package Drawing

Table 7.1. QFN24 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.35	2.45	2.55
e		0.50 BSC	
E		4.00 BSC	
E2	2.35	2.45	2.55
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

8. QSOP24 Package Specifications

8.1 Package Dimensions

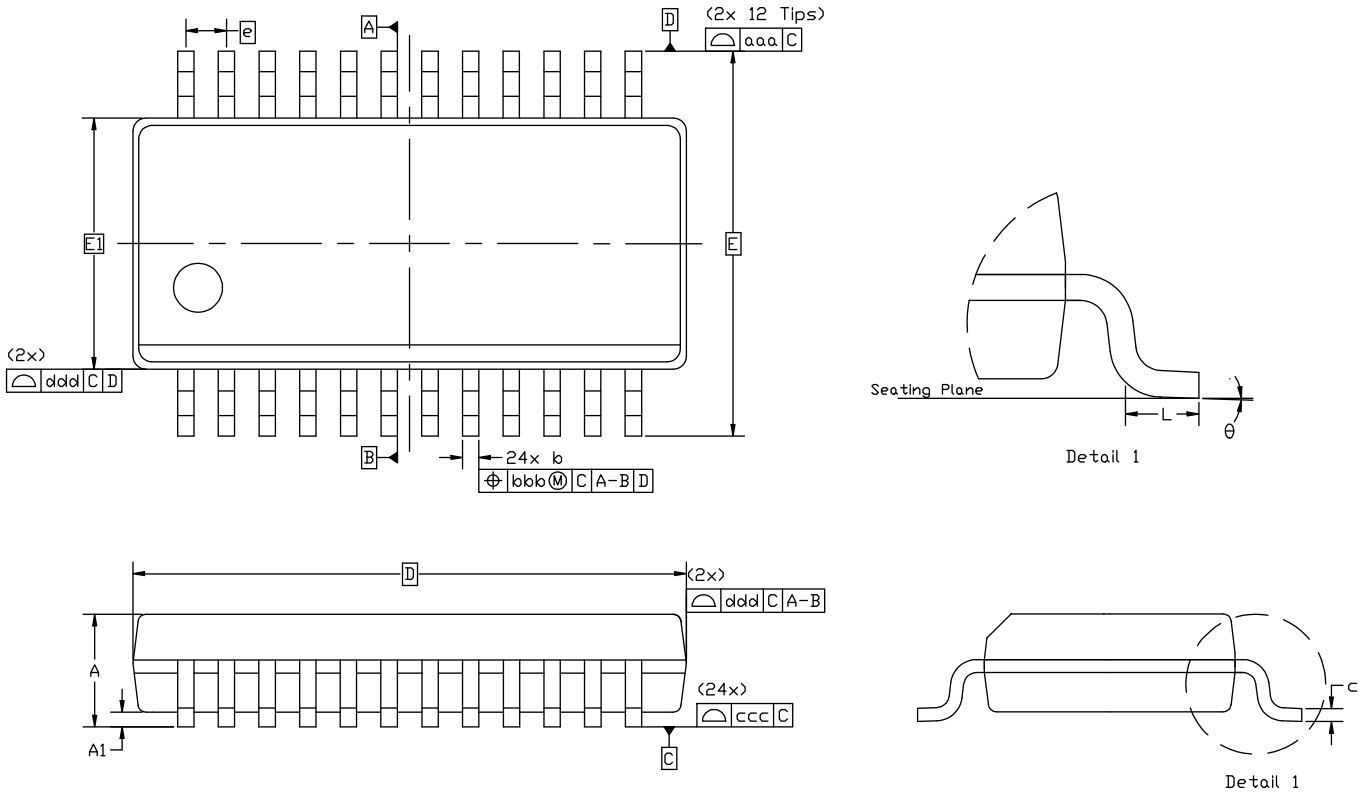

Figure 8.1. Package Drawing

Table 8.1. Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27

9. QFN20 Package Specifications

9.1 QFN20 Package Dimensions

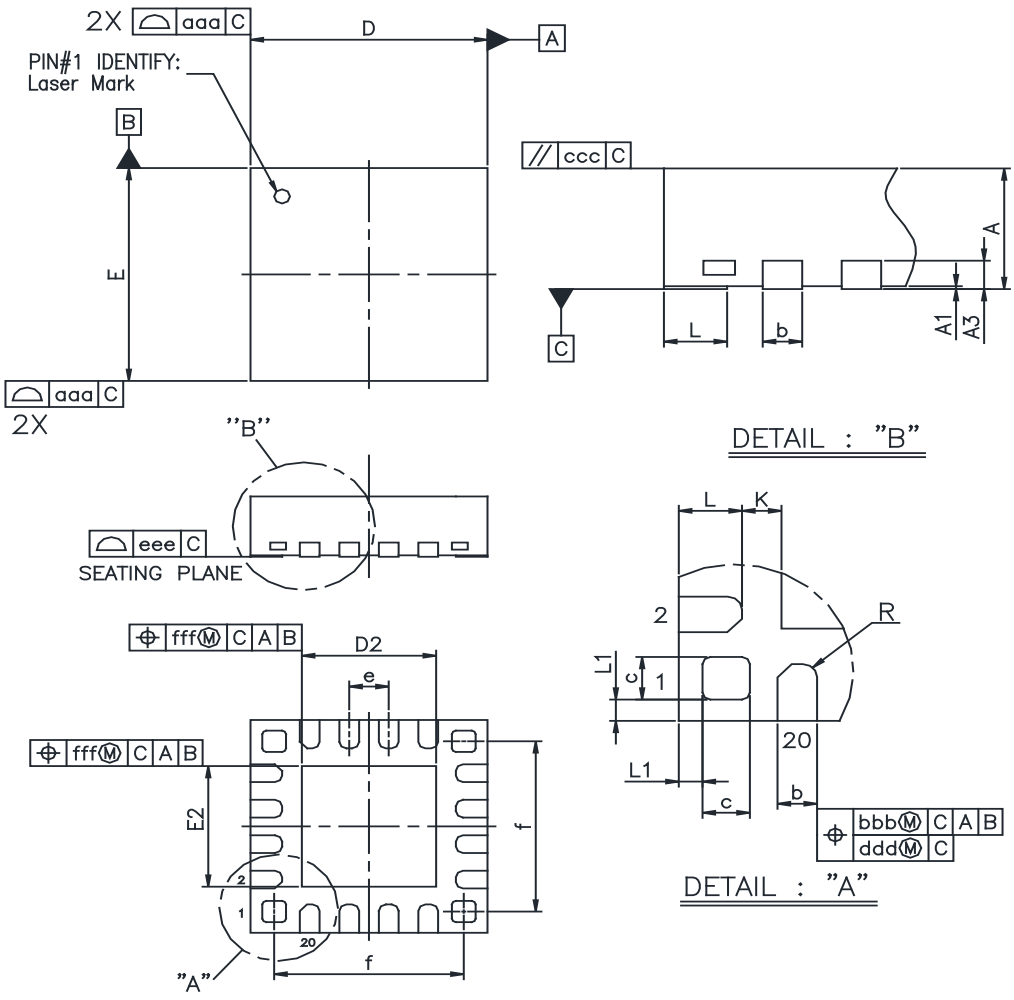

Figure 9.1. QFN20 Package Drawing

Table 9.1. QFN20 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
c	0.25	0.30	0.35
D		3.00 BSC	
D2	1.6	1.70	1.80
e		0.50 BSC	
E		3.00 BSC	

10. Revision History

Revision 1.1

October 20th, 2017

- Updated the front page diagram to indicate USB and SPI are available in Snooze mode.
- Updated the front page and 1. Feature List to refer to two analog comparators.
- Corrected the number of I/O mentioned on the front page.
- Added "Pre-programmed USB Bootloader" to 1. Feature List.
- Updated I/O tolerance range to V_{IO} + 2.5 V in 1. Feature List.
- Updated 3.1 Introduction to mention all device documentation.
- Updated 3.2 Power to remove mention of the I2C Slave peripheral.
- Added bootloader pinout information to 3.10 Bootloader.
- Corrected the application note number for *AN124: Pin Sharing Techniques for the C2 Interface* in 5.3 Debug.
- Added a note to Table 4.2 Power Consumption on page 17 providing more information about the Comparator Reference specification.
- Added maximum specifications to 4.1.14 Configurable Logic Propagation Delay through LUT (internal connection) and Propagation Delay through D flip-flop clock (internal connection).
- Updated 4.1.15 Port I/O to refer to V_{IO} instead of V_{DD} for I/O specifications. Also added a note that V_{IO} = V_{DD} on devices without a VIO pin.
- Added specifications for 4.1.17 SMBus.
- Updated 4.3 Absolute Maximum Ratings to correct the GPIO pin associated with VBUS and update the maximum specfications to be relative to VIO, not VDD.
- Added a VIO specification to 4.3 Absolute Maximum Ratings.
- Updated text and figures in 5.1 Power to remove mention of the VBUS pin.
- Updated the title of Figure 5.3 Connection Diagram with Voltage Regulator Not Used (Self-Powered) on page 34 to include "Self-Powered".
- Updated to show a resistor divider on VBUS in Figure 5.5 Self-Powered Connection Diagram for USB Pins on page 36. Also added two notes regarding VBUS.
- Updated the revision history format.

Revision 1.0

July 20th, 2017

- Initial release.