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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Break at Chatra	A strain
Product Status	ACTIVE
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D - 16bit; D/A - 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-MAPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl46z128vmc4

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Ratings 1

Thermal handling ratings 1.1

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	_	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

Moisture handling ratings 1.2

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level		3		1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).

2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

Determined according to JEDEC Standard JESD78, IC Latch-Up Test.



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	_
	Low-voltage warning thresholds — high range					1
V _{LVW1H}	 Level 1 falling (LVWV = 00) 	2.62	2.70	2.78	v	
V _{LVW2H}	 Level 2 falling (LVWV = 01) 	2.72	2.80	2.88	v	
V _{LVW3H}	 Level 3 falling (LVWV = 10) 	2.82	2.90	2.98	v	
V _{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	v	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range		±60	_	mV	_
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V _{LVW1L}	 Level 1 falling (LVWV = 00) 	1.74	1.80	1.86	v	
V _{LVW2L}	 Level 2 falling (LVWV = 01) 	1.84	1.90	1.96	v	
V _{LVW3L}	 Level 3 falling (LVWV = 10) 	1.94	2.00	2.06	v	
V _{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	v	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range		±40	_	mV	_
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

Table 6.	Vpp supply LVD and POR	operating requirements	(continued)
	*DD Supply LVD and I On v	speraling requirements	(continucu)

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — Normal drive pad (except RESET_b) • 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = -5 mA • 1.71 V \leq V _{DD} \leq 2.7 V, I _{OH} = -2.5 mA	V _{DD} – 0.5 V _{DD} – 0.5	_	V V	1, 2
V _{OH}	Output high voltage — High drive pad (except RESET_b) • 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = -20 mA • 1.71 V \leq V _{DD} \leq 2.7 V, I _{OH} = -10 mA	V _{DD} – 0.5 V _{DD} – 0.5	_	V V	1, 2
I _{OHT}	Output high current total for all ports	_	100	mA	



Symbol	Description	Min.	Max.	Unit	Notes
V _{OL}	Output low voltage — Normal drive pad				1
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 5 mA	_	0.5	V	
	• 1.71 V \leq V _{DD} \leq 2.7 V, I _{OL} = 2.5 mA	_	0.5	v	
V _{OL}	Output low voltage — High drive pad				1
	• 2.7 V \leq V_{DD} \leq 3.6 V, I_{OL} = 20 mA	_	0.5	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 10 \text{ mA}$	_	0.5	V	
I _{OLT}	Output low current total for all ports	—	100	mA	
I _{IN}	Input leakage current (per pin) for full temperature range	_	1	μA	3
I _{IN}	Input leakage current (per pin) at 25 °C	—	0.025	μA	3
I _{IN}	Input leakage current (total all pins) for full temperature range	_		μA	3
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μΑ	
R _{PU}	Internal pullup resistors	20	50	kΩ	4

Table 7. Voltage and current operating behaviors (continued)

1. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.

- 2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
- 3. Measured at $V_{DD} = 3.6 V$

4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx \rightarrow RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.			300	μs	1

 Table 8. Power mode transition operating behaviors



Symbol	Description		Тур.	Max	Unit	Note
	Run mode current - 48 MHz core / 24	at 25 °C	6.9	7.1	mA	
	MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 3.0 V	at 125 °C	7.3	7.6	mA	
I _{DD_WAIT}	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled, at 3.0 V	_	2.9	3.5	mA	3
I _{DD_WAIT}	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	_	2.2	2.8	mA	3
I _{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus, at 3.0 V		1.6	2.1	mA	3
I _{DD_VLPRCO} _CM	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, LPTMR running with 4 MHz internal reference clock, CoreMark benchmark code executing from flash, at 3.0 V		798		μΑ	5
IDD_VLPRCO	Very low power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code executing from flash, at 3.0 V		167	336	μA	6
I _{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code executing from flash, at 3.0 V	_	192	354	μA	6
I _{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 3.0 V	_	257	431	μA	4, 6
I _{DD_VLPW}	Very low power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled, at 3.0 V	_	112	286	μA	6
I _{DD_STOP}	Stop mode current at 3.0 V	at 25 °C	306	328	μA	
		at 50 °C	322	349	μA	
		at 70 °C	348	382	μA	
		at 85 °C	384	433	μA	
		at 105 °C	481	578	μA	
I _{DD_VLPS}	Very-low-power stop mode current at	at 25 °C	2.71	5.03	μA	
	5.0 V	at 50 °C	7.05	11.94	μA	
		at 70 °C	15.80	26.87	μA	

Table 9. Power consumption operating behaviors (continued)



Symbol	Description			٦	empera	ature (°	C)		Unit
			-40	25	50	70	85	105	
I _{IREFSTEN4MHz}	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.		56	56	56	56	56	56	μA
I _{IREFSTEN32KHz}	32 kHz internal reference clock Measured by entering STOP n 32 kHz IRC enabled.	(IRC) adder. node with the	52	52	52	52	52	52	μA
I _{EREFSTEN4MHz}	External 4 MHz crystal clock a Measured by entering STOP o with the crystal enabled.	dder. r VLPS mode	206	228	237	245	251	258	μA
I _{EREFSTEN32KHz}	External 32 kHz crystal clock	VLLS1	440	490	540	560	570	580	nA
	adder by means of the	VLLS3	440	490	540	560	570	580]
	EREFSTEN] bits. Measured	LLS	490	490	540	560	570	680	
	by entering all modes with the	VLPS	510	560	560	560	610	680	
	crystal enabled.	STOP	510	560	560	560	610	680]
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.		22	22	22	22	22	22	μA
I _{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz		432	357	388	475	532	810	nA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
	115200 baud rate. Includes selected clock source power consumption.	OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I _{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	86	μA
	compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	OSCERCLK (4 MHz external crystal)	235	256	265	274	280	287	

Table 10. Low power mode peripheral adders — typical value





Figure 4. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors Table 11. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Тур.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	12	dBµV	1,2
V _{RE2}	Radiated emissions voltage, band 2	50–150	8	dBµV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	7	dBµV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	4	dBµV	
V _{RE_IEC}	IEC level	0.15–1000	М	—	2,3

- Determined according to IEC Standard 61967-1, Integrated Circuits Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions and IEC Standard 61967-2, Integrated Circuits -Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions – TEM Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
- 2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 8 MHz (crystal), f_{SYS} = 48 MHz, f_{BUS} = 24 MHz
- 3. Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions-TEM Cell and Wideband TEM Cell Method





Figure 6. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 18. MCG specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C	_	32.768	—	kHz	
f _{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	_	39.0625	kHz	
$\Delta_{fdco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTRIM] and C4[SCFTRIM]	—	± 0.3	± 0.6	%f _{dco}	1



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
J _{acc_pll}	PLL accumulated jitter over 1µs (RMS)					10
	• f _{vco} = 48 MHz	_	1350	—	ps	
	• f _{vco} = 100 MHz	_	600	_	ps	
D _{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D _{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t _{pll_lock}	Lock detector detection time	_		150 × 10 ⁻⁶ + 1075(1/ f _{pll_ref})	S	11

Table 18. MCG specifications (continued)

- 1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
- 2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, $f_{ints_{ft}}$.
- 3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
- The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation
 (Δf_{dco_t}) over voltage and temperature must be considered.
- 5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
- 6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
- 7. This specification is based on standard deviation (RMS) of period or frequency.
- 8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- 9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
- 10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
- 11. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	—	3.6	V	
IDDOSC	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	_	500	—	nA	
	• 4 MHz	_	200	—	μA	
	• 8 MHz (RANGE=01)	_	300	—	μA	
	• 16 MHz	_	950	—	μA	
		_	1.2	_	mA	

Table 19. Oscillator DC electrical specifications



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	• 24 MHz		1.5	—	mA	
	• 32 MHz					
I _{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	_	25	_	μA	
	• 4 MHz	_	400	_	μA	
	• 8 MHz (RANGE=01)	_	500	_	μA	
	• 16 MHz	_	2.5	_	mA	
	• 24 MHz	_	3	_	mA	
	• 32 MHz	_	4		mA	
C _x	EXTAL load capacitance	_	_	_		2, 3
Cy	XTAL load capacitance	—	—	_		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	_	10	_	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)				MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	_	1		MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)				kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	_	200		kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	_			kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
		_	0	_	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	

Table 19.	Oscillator DC electrical s	pecifications ((continued))
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V_{DD}=3.3 V, Temperature =25 °C
 See crystal or resonator manufacturer's recommendation





Figure 7. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
	ADC	• ADLPC = 1, ADHSC =	1.2	2.4	3.9	MHz	t _{ADACK} =
asynchronous	0	2.4	4.0	6.1	MHz	1/f _{ADACK}	
		• ADLPC = 1, ADHSC = 1	3.0	5.2	7.3	MHz	
f _{adack}		• ADLPC = 0, ADHSC = 0	4.4	6.2	9.5	MHz	
		• ADLPC = 0, ADHSC = 1					
	Sample Time	See Reference Manual chapte	r for sample	times			
TUE	Total unadjusted	12-bit modes	—	±4	±6.8	LSB ⁴	5
	error	12-bit modes	—	±1.4	±2.1		
DNL	Differential non- linearity	12-bit modes	_	±0.7	-1.1 to +1.9	LSB ⁴	5
		 <12-bit modes 	—	±0.2	–0.3 to 0.5		

Table 26.	16-bit ADC	characteristics	(V _{REFH} =	V_{DDA} ,	V _{REFL} =	V _{SSA})
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- 1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
- 2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- 3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{\text{REFH}} V_{\text{REFL}})/2^{N}$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- 8. ADC conversion clock < 3 MHz







Typical ADC 16-bit Single-Ended ENOB vs ADC Clock





Symbol	Description	Min.	Тур.	Max.	Unit
V _{DD}	Supply voltage	1.71		3.6	V
I _{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	_	—	200	μA
I _{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	_	20	μA
V _{AIN}	Analog input voltage	$V_{SS} - 0.3$	_	V _{DD}	V
V _{AIO}	Analog input offset voltage	—	_	20	mV
V _H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	—	5	_	mV
	 CR0[HYSTCTR] = 01 	—	10	_	mV
	• CR0[HYSTCTR] = 10	—	20	_	mV
	 CR0[HYSTCTR] = 11 	—	30		mV
V _{CMPOh}	Output high	V _{DD} – 0.5	_	—	V
V _{CMPOI}	Output low	—	_	0.5	V
t _{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t _{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	_	_	40	μs
I _{DAC6b}	6-bit DAC current adder (enabled)	_	7	—	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3		0.3	LSB

3.6.2 CMP and 6-bit DAC electrical specifications Table 27. Comparator and 6-bit DAC electrical specifications

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD} -0.6 V.

 Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.

3. 1 LSB = $V_{reference}/64$



Figure 11. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements Table 28. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
V _{DACR}	Reference voltage	1.13	3.6	V	1
CL	Output load capacitance	—	100	pF	2
١L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or $V_{\text{REFH}}.$

2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.



3.6.3.2 12-bit DAC operating behaviors Table 29. 12-bit DAC operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA_DACL}	Supply current — low-power mode	_	—	250	μΑ	
I _{DDA_DACH}	Supply current — high-speed mode	_	—	900	μΑ	
t _{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t _{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	_	15	30	μs	1
t _{CCDACLP}	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	_	0.7	1	μs	1
V _{dacoutl}	DAC output voltage range low — high- speed mode, no load, DAC set to 0x000		—	100	mV	
V _{dacouth}	DAC output voltage range high — high- speed mode, no load, DAC set to 0xFFF	V _{DACR} -100	_	V _{DACR}	mV	
INL	Integral non-linearity error — high speed mode	_	_	±8	LSB	2
DNL	Differential non-linearity error — V _{DACR} > 2 V	_	_	±1	LSB	3
DNL	Differential non-linearity error — V _{DACR} = VREF_OUT	_	_	±1	LSB	4
VOFFSET	Offset error	—	±0.4	±0.8	%FSR	5
E _G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \ge 2.4 V$	60	—	90	dB	
T _{CO}	Temperature coefficient offset voltage	—	3.7	_	μV/C	6
T _{GE}	Temperature coefficient gain error	_	0.000421	_	%FSR/C	
Rop	Output resistance (load = $3 \text{ k}\Omega$)	_	—	250	Ω	
SR	Slew rate -80h \rightarrow F7Fh \rightarrow 80h				V/µs	
	 High power (SP_{HP}) 	1.2	1.7	—		
	• Low power (SP _{LP})	0.05	0.12	—		
BW	3dB bandwidth				kHz	
	• High power (SP _{HP})	550	_	—		
	 Low power (SP_{LP}) 	40	_	—		

1. Settling within ± 1 LSB

2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV

3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV

4. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V 5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} – 100 mV

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

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NOTE

The MCGPLLCLK meets the USB jitter specifications for certification with the use of an external clock/crystal for both Device and Host modes.

The MCGFLLCLK does not meet the USB jitter specifications for certification.

3.8.2 USB VREG electrical specifications Table 30. USB VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	_	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	_	125	186	μΑ	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero		1.1	10	μA	
I _{DDoff}	 Quiescent current — Shutdown mode VREGIN = 5.0 V and temperature=25 °C Across operating voltage and temperature 	_	650 —	 4	nA μA	
I _{LOADrun}	Maximum load current — Run mode	—	—	120	mA	
I _{LOADstby}	Maximum load current — Standby mode	—	—	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) > 3.6 V					
	Run mode	3	3.3	3.6	v	
	Standby mode	2.1	2.8	3.6	v	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	_	3.6	V	2
C _{OUT}	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	_	100	mΩ	
I _{LIM}	Short circuit current		290	_	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 $^\circ\text{C}$ unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to ILoad.





Figure 17. SPI slave mode timing (CPHA = 1)

3.8.4 Inter-Integrated Circuit Interface (I2C) timing Table 35. I2C timing

Characteristic	Symbol	Standa	rd Mode	Fast	Mode	Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f _{SCL}	0	100	0	400 ¹	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	4	_	0.6		μs
LOW period of the SCL clock	t _{LOW}	4.7	—	1.3	—	μs
HIGH period of the SCL clock	t _{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	4.7	_	0.6	_	μs
Data hold time for I ² C bus devices	t _{HD} ; DAT	0 ²	3.45 ³	04	0.9 ²	μs
Data set-up time	t _{SU} ; DAT	250 ⁵	—	100 ³ , ⁶	—	ns
Rise time of SDA and SCL signals	t _r	_	1000	20 +0.1C _b ⁷	300	ns
Fall time of SDA and SCL signals	t _f	_	300	20 +0.1C _b ⁶	300	ns
Set-up time for STOP condition	t _{SU} ; STO	4	—	0.6	—	μs
Bus free time between STOP and START condition	t _{BUF}	4.7	—	1.3	_	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see Voltage and current operating behaviors) or when using the Normal drive pins and VDD ≥ 2.7 V



3.8.6.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15.5	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	_	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	19	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	26	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

Table 36. I2S/SAI master mode timing



Figure 19. I2S/SAI timing — master modes



	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	VCAP1	VLL2	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
в	PTE1	PTD6/ LLWU_P15	PTD3	VCAP2	VLL1	PTC7	PTC2	PTC4/ LLWU_P8	в
С	PTD5	PTD2	PTD0	VSS	VLL3	PTC1/ LLWU_P6/ RTC_CLKIN	PTB19	PTC3/ LLWU_P7	с
D	USB0_DM	VREGIN	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
Е	USB0_DP	VOUT33	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	PTE21	PTE23	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	PTA20	F
G	PTE20	PTE22	VREFL	VREFH	PTA4	PTA13	VDD	PTA19	G
н	PTE29	PTE30	PTE31	PTE24	PTE25	PTA12	VSS	PTA18	н
	1	2	3	4	5	6	7	8	

Figure 25. KL46 64-pin BGA pinout diagram



6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: PKL46 and MKL46

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	 M = Fully qualified, general market flow P = Prequalification
KL##	Kinetis family	• KL46
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	 128 = 128 KB 256 = 256 KB
R	Silicon revision	 (Blank) = Main A = Revision after main
Т	Temperature range (°C)	• V = -40 to 105
PP	Package identifier	 LH = 64 LQFP (10 mm x 10 mm) MP = 64 MAPBGA (5 mm x 5 mm)

Table 42. Part number fields descriptions



Rev. No.	Date	Substantial Changes	
		 Updated Capacitance attributes Updated footnote in the Device clock specifications Added thermal attributes of 64-pin MAPBGA in the Thermal attributes Added V_{REFH} and V_{REFL} in the 16-bit ADC electrical characteristics Updated footnote to the V_{DACR} in the 12-bit DAC operating requirements Updated I_{LOADrun} and I_{LIM} in the USB VREG electrical specifications Added Inter-Integrated Circuit Interface (I2C) timing 	
4	5/2014	 Updated Power consumption operating behaviors Updated USB electrical specifications Updated Definition: Operating behavior 	
5	08/2014	 Updated related source in the front page Updated Power consumption operating behaviors Updated the note in USB electrical specifications 	

Table 44.	Revision	history ((continued)
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