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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D - 16bit; D/A - 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl46z256vlh4

- Periodic interrupt timers
- 16-bit low-power timer (LPTMR)
- Real time clock

Security and integrity modules

- 80-bit unique identification number per chip

Ordering Information [1]

Part Number	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MKL46Z128VLH4	128	16	50
MKL46Z256VLH4	256	32	50
MKL46Z256VMP4	256	32	50
MKL46Z128VLL4	128	16	84
MKL46Z256VLL4	256	32	84
MKL46Z128VMC4	128	16	84
MKL46Z256VMC4	256	32	84

1. To confirm current availability of ordererable part numbers, go to http://www.freescale.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL46P121M48SF4RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL46P121M48SF4[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_*x*N40H[2]
Package drawing	Package dimensions are provided in package drawings.	LQFP 64-pin: 98ASS23234W[1] MAPBGA 64-pin: 98ASA00420D[1] LQFP 100-pin: 98ASS23308W[1] MAPBGA 121-pin: 98ASA00344D[1]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.
2. To find the associated resource, go to http://www.freescale.com and perform a search using this term with the “*x*” replaced by the revision of the device you are using.

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-3	—	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|.
2. Open drain outputs must be pulled to V_{DD}.

2.2.2 LVD and POR operating requirements

Table 6. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value

Symbol	Description		Temperature (°C)						Unit
			-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.		56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.		52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.		206	228	237	245	251	258	µA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	VLLS1	440	490	540	560	570	580	nA
		VLLS3	440	490	540	560	570	580	
		LLS	490	490	540	560	570	680	
		VLPS	510	560	560	560	610	680	
		STOP	510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.		22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.		432	357	388	475	532	810	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	µA
		OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	86	µA
		OSCERCLK (4 MHz external crystal)	235	256	265	274	280	287	

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	µA
I_{LCD}	LCD peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the OSC0_CR[EREFSTEN, EREFSTEN] bits. VIREG disabled, resistor bias network enabled, 1/8 duty cycle, 8 x 36 configuration for driving 288 Segments, 32 Hz frame rate, no LCD glass connected. Includes ERCLK32K (32 kHz external crystal) power consumption.	5	5	5	5	5	5	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

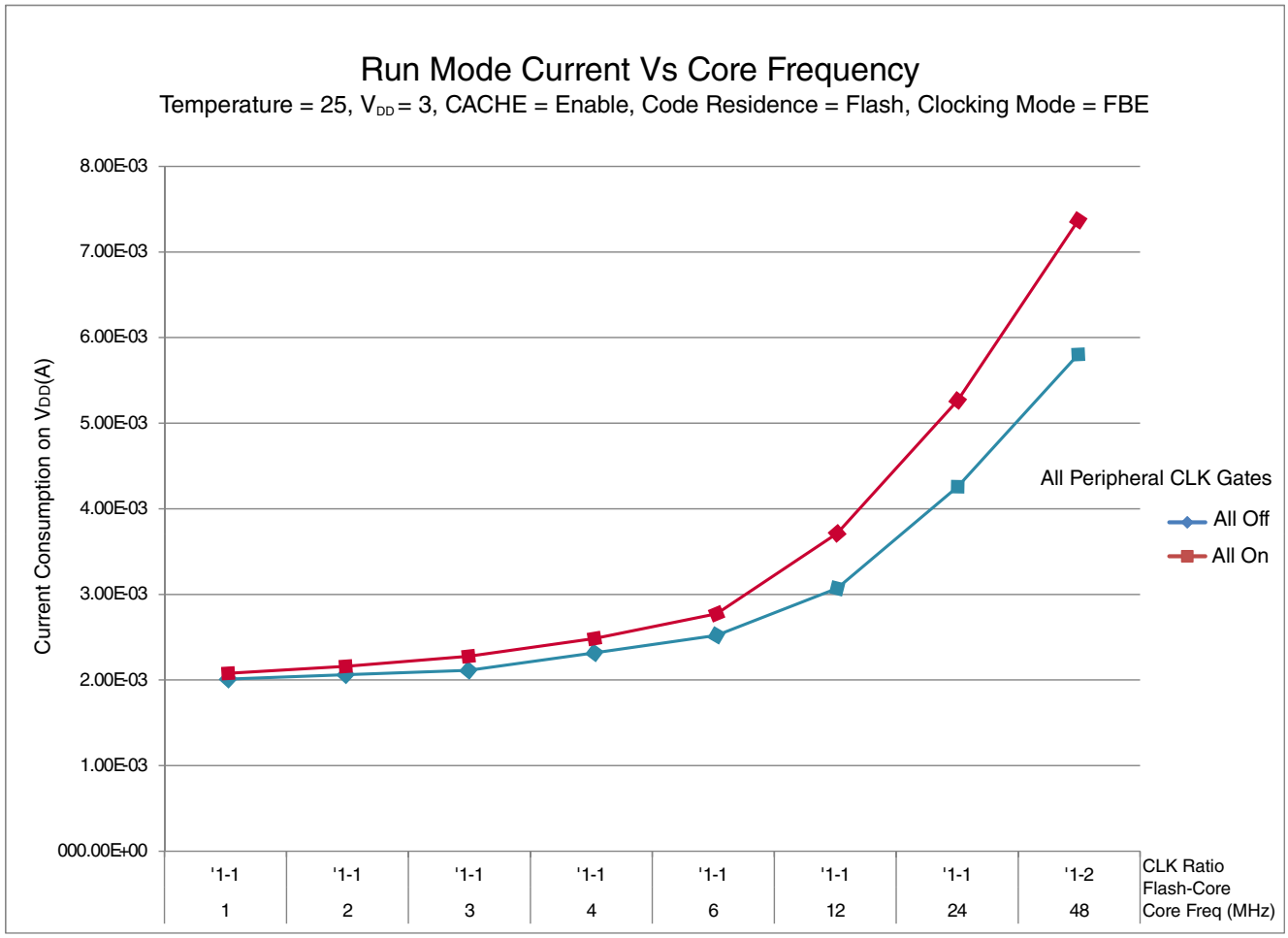


Figure 3. Run mode supply current vs. core frequency

2.4.2 Thermal attributes

Table 16. Thermal attributes

Board type	Symbol	Description	121 MAPBGA	100 LQFP	64 LQFP	64 MAPBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	94	64	69	49.8	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	57	51	51	42.3	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	81	54	58	40.9	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	53	45	44	37.7	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	40	37	33	39.2	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	30	19	19	50.3	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	8	4	4	2.2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 17. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	 0	 25	 MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	 20	 —	 ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

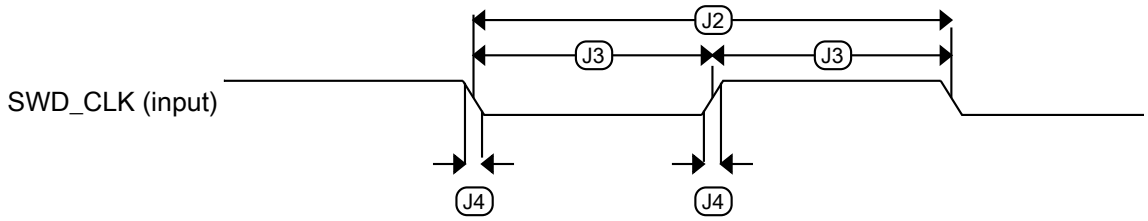


Figure 5. Serial wire clock input timing

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk128k}$	Erase Block high-voltage time for 128 KB	—	52	452	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk128k}$	Read 1s Block execution time • 128 KB program flash	—	—	1.7	ms	—
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
$t_{ersblk128k}$	Erase Flash Block execution time • 128 KB program flash	—	88	600	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	—
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	175	1300	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 23. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 25 and Table 26 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

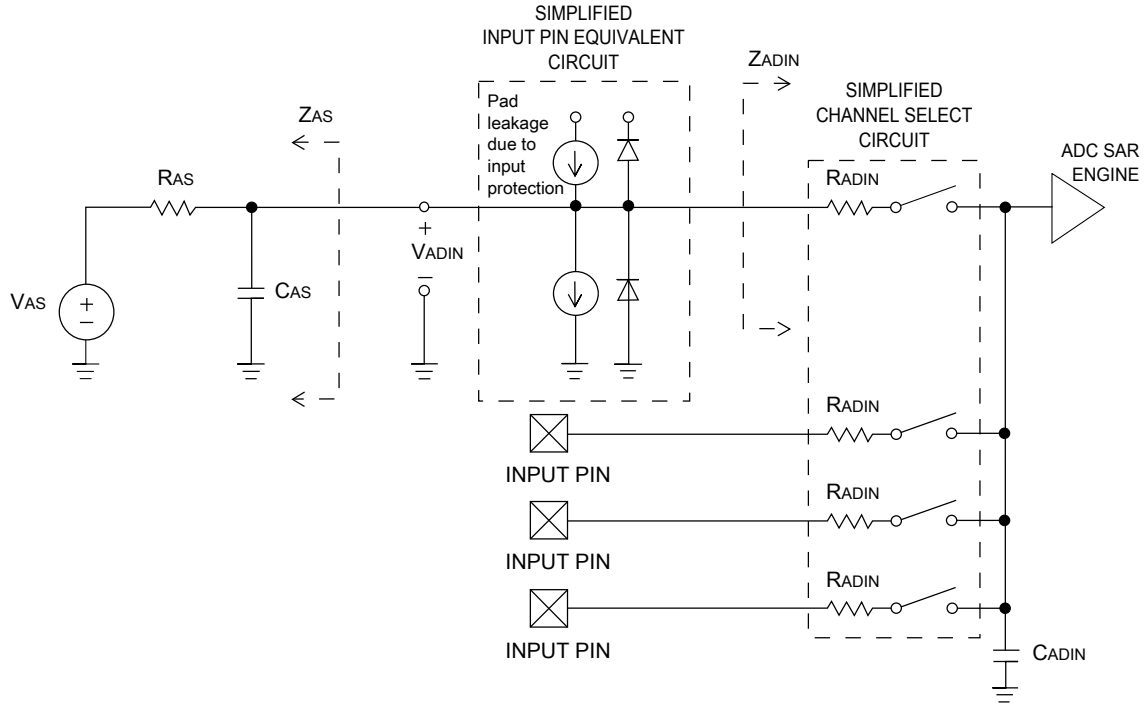


Figure 7. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 26. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	t_{ADACK} = $1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5

Table continues on the next page...

Table 26. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	— —	-94 -85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	82 78	95 90	— —	dB dB	7
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

3.6.3.2 12-bit DAC operating behaviors

Table 29. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	250	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	900	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	 1.2 0.05	 1.7 0.12	 — —	V/μs	
BW	3dB bandwidth • High power (SP_{HP}) • Low power (SP_{LP})	 550 40	 — —	 — —	kHz	

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

3.8.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 31. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$

Table 32. SPI master mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—

Table continues on the next page...

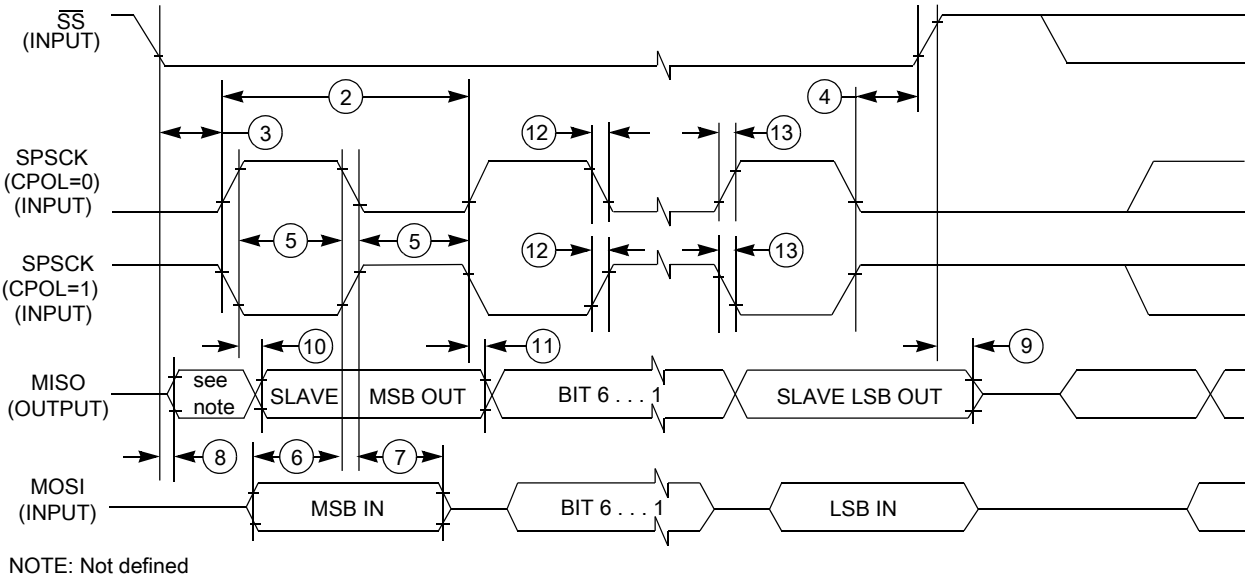


Figure 17. SPI slave mode timing (CPHA = 1)

3.8.4 Inter-Integrated Circuit Interface (I2C) timing

Table 35. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[1]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[2]	3.45[3]	0[4]	0.9[2]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3, 6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see Voltage and current operating behaviors) or when using the Normal drive pins and VDD ≥ 2.7 V

Table 38. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	75	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

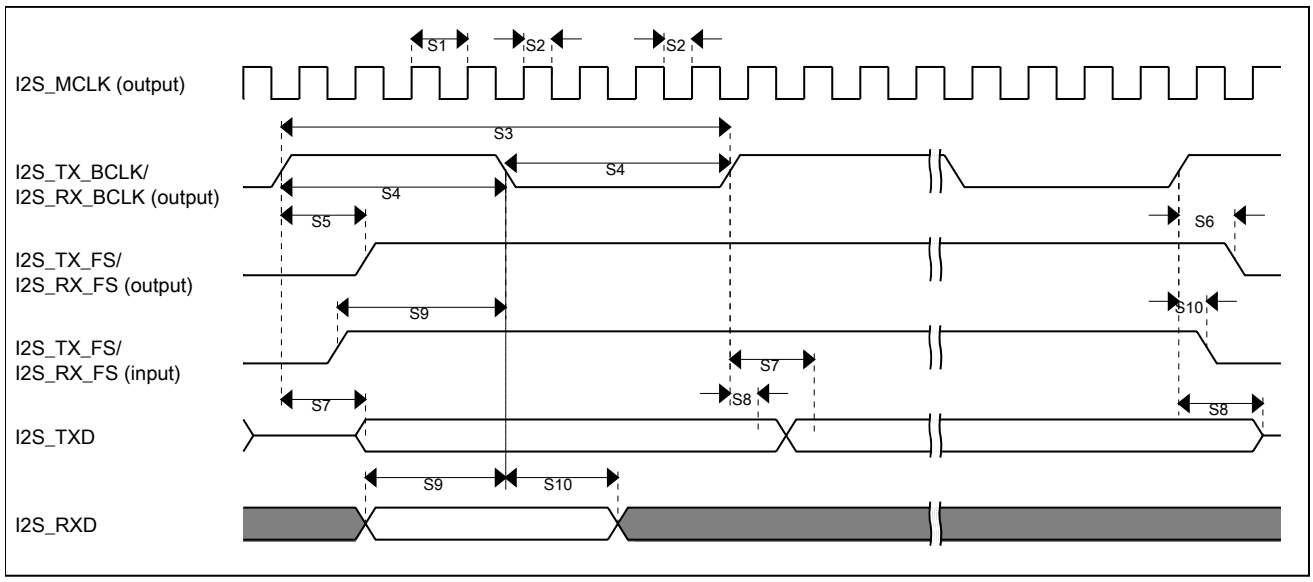


Figure 21. I2S/SAI timing — master modes

Table 39. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns

Table continues on the next page...

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
64-pin LQFP	98ASS23234W
64-pin MAPBGA	98ASA00420D
100-pin LQFP	98ASS23308W
121-pin MAPBGA	98ASA00344D

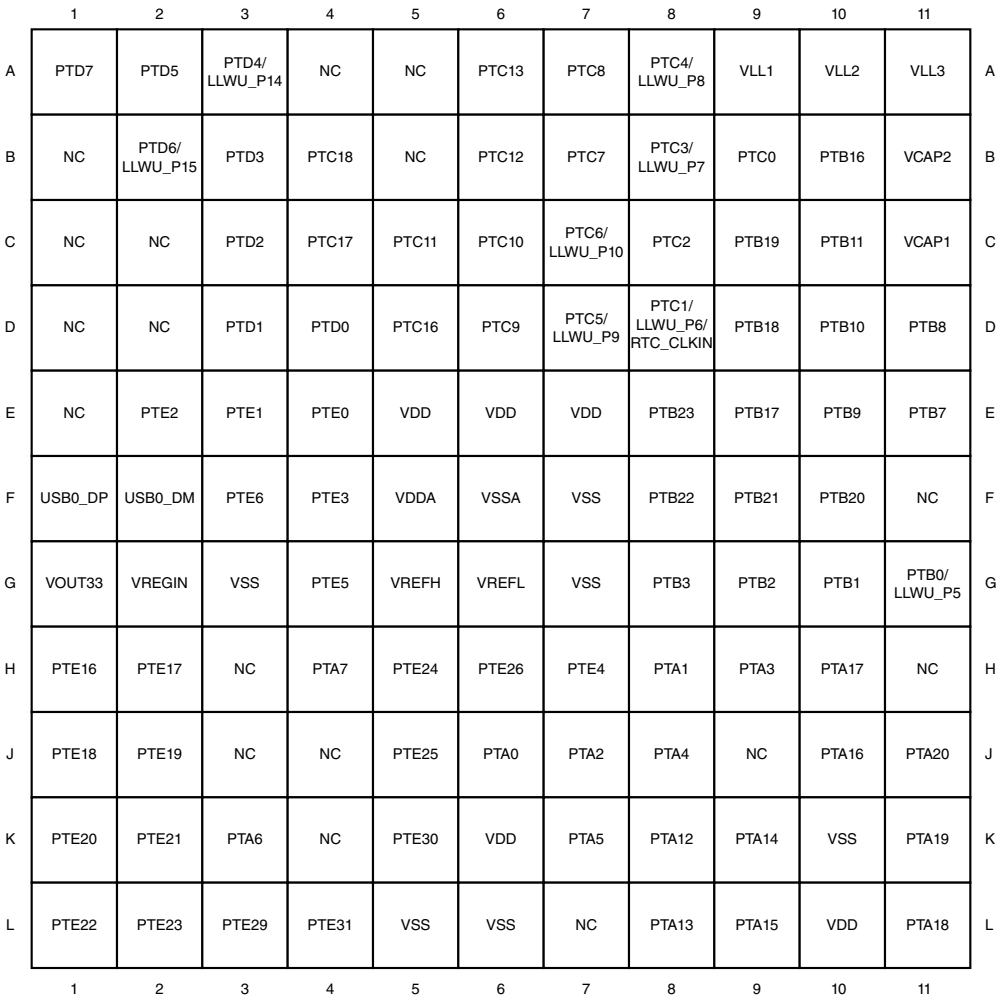
5 Pinout

5.1 KL46 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

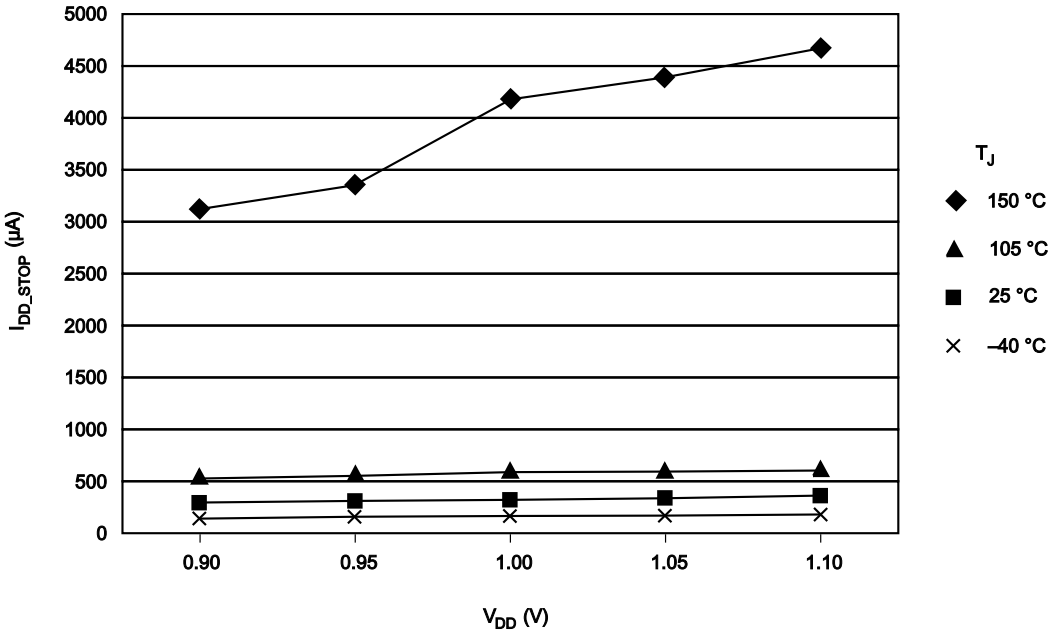
121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
E4	1	A1	1	PTE0	DISABLED	LCD_P48	PTE0	SPI1_MISO	UART1_TX	RTC_ CLKOUT	CMP0_OUT	I2C1_SDA	LCD_P48
E3	2	B1	2	PTE1	DISABLED	LCD_P49	PTE1	SPI1_MOSI	UART1_RX		SPI1_MISO	I2C1_SCL	LCD_P49
E2	3	—	—	PTE2	DISABLED	LCD_P50	PTE2	SPI1_SCK					LCD_P50
F4	4	—	—	PTE3	DISABLED	LCD_P51	PTE3	SPI1_MISO			SPI1_MOSI		LCD_P51
H7	5	—	—	PTE4	DISABLED	LCD_P52	PTE4	SPI1_PCS0					LCD_P52
G4	6	—	—	PTE5	DISABLED	LCD_P53	PTE5						LCD_P53
F3	7	—	—	PTE6	DISABLED	LCD_P54	PTE6			I2S0_MCLK	audioUSB_ SOF_OUT		LCD_P54
E6	8	—	3	VDD	VDD	VDD							
G7	9	C4	4	VSS	VSS	VSS							
L6	—	—	—	VSS	VSS	VSS							
F1	10	E1	5	USB0_DP	USB0_DP	USB0_DP							
F2	11	D1	6	USB0_DM	USB0_DM	USB0_DM							
G1	12	E2	7	VOUT33	VOUT33	VOUT33							
G2	13	D2	8	VREGIN	VREGIN	VREGIN							
H1	14	—	—	PTE16	ADC0_DP1/ ADC0_SE1	LCD_P55/ ADC0_DP1/ ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_ CLKIN0			LCD_P55

121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
H4	41	—	—	PTA7	DISABLED		PTA7		TPM0_CH4				
K8	42	H6	28	PTA12	DISABLED		PTA12		TPM1_CH0			I2S0_TXD0	
L8	43	G6	29	PTA13	DISABLED		PTA13		TPM1_CH1			I2S0_TX_FS	
K9	44	—	—	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_ BCLK	I2S0_TXD0
L9	45	—	—	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0	
J10	46	—	—	PTA16	DISABLED		PTA16	SPI0_MOSI			SPI0_MISO	I2S0_RX_FS	I2S0_RXD0
H10	47	—	—	PTA17	DISABLED		PTA17	SPI0_MISO			SPI0_MOSI	I2S0_MCLK	
L10	48	G7	30	VDD	VDD	VDD							
K10	49	H7	31	VSS	VSS	VSS							
L11	50	H8	32	PTA18	EXTAL0	EXTAL0	PTA18		UART1_RX	TPM_ CLKIN0			
K11	51	G8	33	PTA19	XTAL0	XTAL0	PTA19		UART1_TX	TPM_ CLKIN1		LPTMR0_ ALT1	
J11	52	F8	34	PTA20	RESET_b		PTA20						RESET_b
G11	53	F7	35	PTB0/ LLWU_P5	LCD_P0/ ADC0_SE8/ TSI0_CH0	LCD_P0/ ADC0_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				LCD_P0
G10	54	F6	36	PTB1	LCD_P1/ ADC0_SE9/ TSI0_CH6	LCD_P1/ ADC0_SE9/ TSI0_CH6	PTB1	I2C0_SDA	TPM1_CH1				LCD_P1
G9	55	E7	37	PTB2	LCD_P2/ ADC0_SE12/ TSI0_CH7	LCD_P2/ ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	TPM2_CH0				LCD_P2
G8	56	E8	38	PTB3	LCD_P3/ ADC0_SE13/ TSI0_CH8	LCD_P3/ ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	TPM2_CH1				LCD_P3
E11	57	—	—	PTB7	LCD_P7	LCD_P7	PTB7						LCD_P7
D11	58	—	—	PTB8	LCD_P8	LCD_P8	PTB8	SPI1_PCS0	EXTRG_IN				LCD_P8
E10	59	—	—	PTB9	LCD_P9	LCD_P9	PTB9	SPI1_SCK					LCD_P9
D10	60	—	—	PTB10	LCD_P10	LCD_P10	PTB10	SPI1_PCS0					LCD_P10
C10	61	—	—	PTB11	LCD_P11	LCD_P11	PTB11	SPI1_SCK					LCD_P11
B10	62	E6	39	PTB16	LCD_P12/ TSI0_CH9	LCD_P12/ TSI0_CH9	PTB16	SPI1_MOSI	UART0_RX	TPM_ CLKIN0	SPI1_MISO		LCD_P12
E9	63	D7	40	PTB17	LCD_P13/ TSI0_CH10	LCD_P13/ TSI0_CH10	PTB17	SPI1_MISO	UART0_TX	TPM_ CLKIN1	SPI1_MOSI		LCD_P13
D9	64	D6	41	PTB18	LCD_P14/ TSI0_CH11	LCD_P14/ TSI0_CH11	PTB18		TPM2_CH0	I2S0_TX_ BCLK			LCD_P14
C9	65	C7	42	PTB19	LCD_P15/ TSI0_CH12	LCD_P15/ TSI0_CH12	PTB19		TPM2_CH1	I2S0_TX_FS			LCD_P15
F10	66	—	—	PTB20	LCD_P16	LCD_P16	PTB20					CMP0_OUT	LCD_P16
F9	67	—	—	PTB21	LCD_P17	LCD_P17	PTB21						LCD_P17
F8	68	—	—	PTB22	LCD_P18	LCD_P18	PTB22						LCD_P18
E8	69	—	—	PTB23	LCD_P19	LCD_P19	PTB23						LCD_P19



	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	NC	NC	PTC13	PTC8	PTC4/ LLWU_P8	VLL1	VLL2	VLL3	A
B	NC	PTD6/ LLWU_P15	PTD3	PTC18	NC	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	VCAP2	B
C	NC	NC	PTD2	PTC17	PTC11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	VCAP1	C
D	NC	NC	PTD1	PTD0	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6/ RTC_CLKIN	PTB18	PTB10	PTB8	D
E	NC	PTE2	PTE1	PTE0	VDD	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	USB0_DP	USB0_DM	PTE6	PTE3	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	NC	F
G	VOUT33	VREGIN	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	PTE16	PTE17	NC	PTA7	PTE24	PTE26	PTE4	PTA1	PTA3	PTA17	NC	H
J	PTE18	PTE19	NC	NC	PTE25	PTA0	PTA2	PTA4	NC	PTA16	PTA20	J
K	PTE20	PTE21	PTA6	NC	PTE30	VDD	PTA5	PTA12	PTA14	VSS	PTA19	K
L	PTE22	PTE23	PTE29	PTE31	VSS	VSS	NC	PTA13	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 23. KL46 121-pin BGA pinout diagram



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 43. Typical value conditions

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 44. Revision history

Rev. No.	Date	Substantial Changes
3	3/2014	• Updated the front page and restructured the chapters • Updated Voltage and current operating behaviors • Updated EMC radiated emissions operating behaviors • Updated Power mode transition operating behaviors

Table continues on the next page...

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Document Number KL46P121M48SF4
Revision 5 08/2014