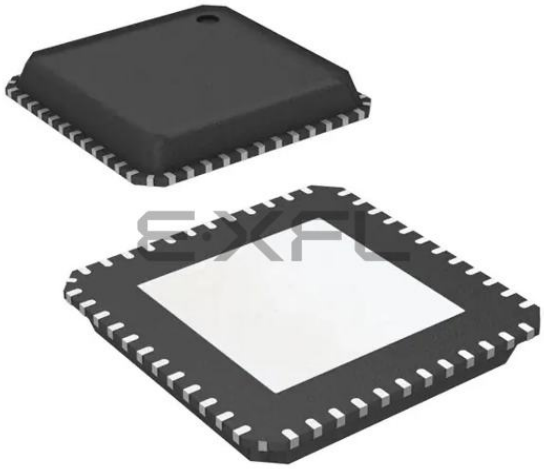
Infineon Technologies - XE161FU8F40VAAKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-54
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe161fu8f40vaakxuma1

1.2 Definition of Feature Variants

The XE161FU types are offered with several Flash memory sizes. **Table 3** and **Table 4** describe the location of the available Flash memory.

Table 3 Continuous Flash Memory Ranges

Total Flash Size	1st Range[1)]	2nd Range	3rd Range
64 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'0FFF_H$	n.a.
32 Kbytes	$C0'0000_H$ … $C0'7FFF_H$	n.a.	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1
64	64	n.a.
32	32	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XE161FU types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels / Message Objects
10 ADC0 channels	CH0, CH2, CH3, CH4, CH8, CH9, CH16, CH17, CH19, CH20
2 serial channels	U0C0, U0C1

Key to Pin Definitions

- **Ctrl.**: The output signal for a port pin is selected by bit field PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bit field PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.
  Output signal OH is controlled by hardware.
- **Type**: Indicates the pad type and its power supply domain (B, M).
  - St: Standard pad
  - Sp: Special pad e.g. XTALx
  - DA: Digital IO and analog input
  - In: Input only pad
  - PS: Power supply pad

Table 6 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
1	$\overline{\text{TESTM}}$	I	In/B	**Testmode Enable** Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
2	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE161FU's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
3	P6.3	O0 / I	St/B	**Bit 3 of Port 6, General Purpose Input/Output**
	T3OUT	O2	St/B	**GPT12E Timer T3 Toggle Latch Output**
	ADC0_REQTRyF	I	St/B	**External Request Trigger Input for ADC0/1**
4	P6.1	O0 / I	DA/B	**Bit 1 of Port 6, General Purpose Input/Output**
	ADC0_CH17	I	DA/B	**Analog Input Channel 17 for ADC0**
	EMUX1	O1	DA/B	**External Analog MUX Control Output 1 (ADC0)**
	T3OUT	O2	DA/B	**GPT12E Timer T3 Toggle Latch Output**
	ADC0_REQTRyE	I	DA/B	**External Request Trigger Input for ADC0**
	ESR1_6	I	DA/B	**ESR1 Trigger Input 6**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
5	P6.0	O0 / I	DA/B	**Bit 0 of Port 6, General Purpose Input/Output**
	ADC0_CH16	I	DA/B	**Analog Input Channel 16 for ADC0**
	EMUX0	O1	DA/B	**External Analog MUX Control Output 0 (ADC0)**
	$\overline{\text{BRKOUT}}$	O3	DA/B	**OCDS Break Signal Output**
	ADC0_REQGTyG	I	DA/B	**External Request Gate Input for ADC0**
10	P5.0	I	In/B	**Bit 0 of Port 5, General Purpose Input**
	ADC0_CH0	I	In/B	**Analog Input Channel 0 for ADC0**
11	P5.2	I	In/B	**Bit 2 of Port 5, General Purpose Input**
	ADC0_CH2	I	In/B	**Analog Input Channel 2 for ADC0**
	TDI_A	I	In/B	**JTAG Test Data Input**
12	P5.3	I	In/B	**Bit 3 of Port 5, General Purpose Input**
	ADC0_CH3	I	In/B	**Analog Input Channel 3 for ADC0**
	T3INA	I	In/B	**GPT12E Timer T3 Count/Gate Input**
13	P5.4	I	In/B	**Bit 4 of Port 5, General Purpose Input**
	ADC0_CH4	I	In/B	**Analog Input Channel 4 for ADC0**
	T3EUDA	I	In/B	**GPT12E Timer T3 External Up/Down Control Input**
	TMS_A	I	In/B	**JTAG Test Mode Selection Input**
14	P5.8	I	In/B	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/B	**Analog Input Channel 8 for ADC0**
	CCU60_T12HRC	I	In/B	**External Run Control Input for T12 of CCU60**
	CCU60_T13HRC	I	In/B	**External Run Control Input for T13 of CCU60**
15	P5.9	I	In/B	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/B	**Analog Input Channel 9 for ADC0**
	CC2_T7IN	I	In/B	**CAPCOM2 Timer T7 Count Input**
16	P2.0	O0 / I	DA/B	**Bit 0 of Port 2, General Purpose Input/Output**
	ADC0_CH19	I	DA/B	**Analog Input Channel 19 for ADC0**
	T5INB	I	DA/B	**GPT12E Timer T5 Count/Gate Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
33	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_CC62	O2	St/B	**CCU60 Channel 2 Output**
	CCU60_CC62INA	I	St/B	**CCU60 Channel 2 Input**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
34	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
35	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COUT61	O2	St/B	**CCU60 Channel 1 Output**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR1_9	I	St/B	**ESR1 Trigger Input 9**
36	P10.5	O0 / I	St/B	**Bit 5 of Port 10, General Purpose Input/Output**
	U0C1_SCLKOUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU60_COUT62	O2	St/B	**CCU60 Channel 2 Output**
	U0C1_DX1B	I	St/B	**USIC0 Channel 1 Shift Clock Input**
37	P10.6	O0 / I	St/B	**Bit 6 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	U0C0_DX0C	I	St/B	**USIC0 Channel 0 Shift Data Input**
	CCU60_CTRAPA	I	St/B	**CCU60 Emergency Trap Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
38	P10.7	O0 / I	St/B	**Bit 7 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_COUT63	O2	St/B	**CCU60 Channel 3 Output**
	U0C1_DX0B	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CCU60_CCPOS0A	I	St/B	**CCU60 Position Input 0**
	T4INB	I	St/B	**GPT12E Timer T4 Count/Gate Input**
39	P10.8	O0 / I	St/B	**Bit 8 of Port 10, General Purpose Input/Output**
	U0C0_MCLKOUT	O1	St/B	**USIC0 Channel 0 Master Clock Output**
	U0C1_SELO0	O2	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	CCU60_CCPOS1A	I	St/B	**CCU60 Position Input 1**
	U0C0_DX1C	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	$\overline{\text{BRKIN\_B}}$	I	St/B	**OCDS Break Signal Input**
	T3EUDB	I	St/B	**GPT12E Timer T3 External Up/Down Control Input**
	ESR2_11	I	St/B	**ESR2 Trigger Input 11**
40	P10.9	O0 / I	St/B	**Bit 9 of Port 10, General Purpose Input/Output**
	U0C0_SELO4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_MCLKOUT	O2	St/B	**USIC0 Channel 1 Master Clock Output**
	CCU60_CCPOS2A	I	St/B	**CCU60 Position Input 2**
	TCK_B	I	St/B	**DAP0/JTAG Clock Input**
	T3INB	I	St/B	**GPT12E Timer T3 Count/Gate Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
18, 43	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDIM} pins must be connected to each other.
7, 20, 41	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins.
6, 19, 42	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane.

3.1 Memory Subsystem and Organization

The memory space of the XE161FU is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 8 XE161FU **Memory Map** [1]

Address Area	Start Loc.	End Loc.	Area Size[2]	Notes
IMB register space	FF'FF00$_H$	FF'FFFF$_H$	256 bytes	
Reserved	F0'0000$_H$	FF'FEFF$_H$	< 1 Mbyte	Minus IMB registers.
Reserved for EPSRAM	E8'1000$_H$	EF'FFFF$_H$	508 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8'0000$_H$	E8'0FFF$_H$	up to 4 Kbytes	With Flash timing.
Reserved for PSRAM	E0'1000$_H$	E7'FFFF$_H$	508 Kbytes	Mirrors PSRAM
PSRAM	E0'0000$_H$	E0'0FFF$_H$	up to 4 Kbytes	Program SRAM.
Reserved for Flash	C1'1000$_H$	DF'FFFF$_H$	1980 Kbytes	
Flash 0	C0'0000$_H$	C1'0FFF$_H$	68 Kbytes[3]	
External memory area	40'0000$_H$	BF'FFFF$_H$	8 Mbytes	
External IO area[4]	21'0000$_H$	3F'FFFF$_H$	1984 Kbytes	
Reserved	20'B400$_H$	20'FFFF$_H$	19 Kbytes	
USIC0 alternate regs.	20'B000$_H$	20'B3FF$_H$	1 Kbytes	Accessed via LXBus controller
Reserved	20'4800$_H$	20'AFFF$_H$	26 Kbytes	
USIC0 registers	20'4000$_H$	20'47FF$_H$	2 Kbytes	Accessed via LXBus controller
Reserved	20'0000$_H$	20'3FFF$_H$	16 Kbytes	
External memory area	01'0000$_H$	1F'FFFF$_H$	1984 Kbytes	
SFR area	00'FE00$_H$	00'FFFF$_H$	0.5 Kbytes	
Dual-port RAM (DPRAM)	00'F600$_H$	00'FDFF$_H$	2 Kbytes	
Reserved for DPRAM	00'F200$_H$	00'F5FF$_H$	1 Kbytes	
ESFR area	00'F000$_H$	00'F1FF$_H$	0.5 Kbytes	
XSFR area	00'E000$_H$	00'EFFF$_H$	4 Kbytes	
Data SRAM (DSRAM)	00'D800$_H$	00'DFFF$_H$	2 Kbytes	

2 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

The on-chip Flash memory stores code, constant data, and control data. The on-chip Flash memory consist of 1 module of 64 Kbytes. Each module is organized in 4-Kbyte sectors.
The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.6**.

Memory Content Protection

The contents of on-chip memories can be protected against soft errors (induced e.g. by radiation) by activating the parity mechanism or the Error Correction Code (ECC).
The parity mechanism can detect a single-bit error and prevent the software from using incorrect data or executing incorrect instructions.
The ECC mechanism can detect and automatically correct single-bit errors. This supports the stable operation of the system.

It is strongly recommended to activate the ECC mechanism wherever possible because this dramatically increases the robustness of an application against such soft errors.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

3.17 Power Management

The XE161FU provides the means to control the power it consumes either at a given time or averaged over a certain duration.
Two mechanisms can be used (and partly in parallel):

- **Clock Generation Management** controls the frequency of internal and external clock signals. Clock signals for currently inactive parts of logic are disabled automatically. The user can drastically reduce the consumed power by reducing the XE161FU system clock frequency.
  External circuits can be controlled using the programmable frequency output EXTCLK.
- **Peripheral Management** permits temporary disabling of peripheral modules. Each peripheral can be disabled and enabled separately. The CPU can be switched off while the peripherals can continue to operate.

Wake-up from power reduction modes can be triggered either externally with signals generated by the external system, or internally by the on-chip wake-up timer. This supports intermittent operation of the XE161FU by generating cyclic wake-up signals. Full performance is available to quickly react to action requests while the intermittent sleep phases greatly reduce the average system power consumption.

Note: When selecting the supply voltage and the clock source and generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states. Recommended sequences are provided which ensure the intended operation of power supply system and clock system. Please refer to the Programmer's Guide.

4.3.1 DC Parameters for Upper Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Note: Operating Conditions apply.

Table 16 is valid under the following conditions: $V_{DDP} \leq$ 5.5 V; V_{DDP}typ. 5 V; $V_{DDP} \geq$ 4.5 V

Table 16 DC Characteristics for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs).	C_{IO} CC	–	–	10	pF	not subject to production test
Input Hysteresis[1)]	HYS CC	0.11 x V_{DDP}	–	–	V	R_S= 0 Ohm
Absolute input leakage current on pins of analog ports[2)]	$\|I_{OZ1}\|$ CC	–	10	200	nA	$V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Absolute input leakage current for all other pins. [2)3)]	$\|I_{OZ2}\|$ CC	–	0.2	5	µA	$T_J \leq$ 110 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
		–	0.2	10	µA	$T_J \leq$ 150 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Pull Level Force Current[4)]	$\|I_{PLF}\|$ SR	220	–	–	µA	$V_{IN} \geq V_{IHmin}$ *(pulldown_enabled)*; $V_{IN} \leq V_{ILmax}$ *(pullup_enabled)*
Pull Level Keep Current[5)]	$\|I_{PLK}\|$ SR	–	–	30	µA	$V_{IN} \geq V_{IHmin}$ *(pullup_enabled);* $V_{IN} \leq V_{ILmax}$ *(pulldown_enabled)*
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	

Table 16 DC Characteristics for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 x V_{DDP}	V	
Output High voltage[6]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \geq I_{OHmax}$
		V_{DDP} - 0.4	–	–	V	$I_{OH} \geq I_{OHnom}$ [7]
Output Low Voltage[6]	V_{OL} CC	–	–	0.4	V	$I_{OL} \leq I_{OLnom}$ [8]
		–	–	1.0	V	$I_{OL} \leq I_{OLmax}$

1) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

2) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

3) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (T_J = junction temperature [°C]): I_{OZ} = 0.05 x $e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]): I_{OZ} = $I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

4) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device.

5) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level.

6) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

7) As a rule, with decreasing output current the output levels approach the respective supply level (VOL->VSS, VOH->VDDP). However, only the levels for nominal output currents are verified.

8) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}->V_{SS}, V_{OH}->V_{DDP}). However, only the levels for nominal output currents are verified.

4.3.3 Power Consumption

The power consumed by the XE161FU depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current I_S depends on the device activity
- The leakage current I_{LK} depends on the device temperature

To determine the actual power consumption, always both components, switching current I_S and leakage current I_{LK} must be added:

$I_{DDP} = I_S + I_{LK}$.

Note: The power consumption values are not subject to production test. They are verified by design/characterization.
To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in most parts of domain DMP_M stopped.

Note: The maximum values cover the complete specified operating range of all manufactured devices.
The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.
After a power reset, the decoupling capacitors for V_{DDIM} are charged with the maximum possible current.

For additional information, please refer to **Section 5.2**, **Thermal Considerations**.

Note: Operating Conditions apply.

4.4 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 20 ADC Parameters for All Voltage Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at an analog input	C_{AINSW} CC	–	9	20	pF	not subject to production test [1]
Total capacitance at an analog input	C_{AINT} CC	–	20	30	pF	not subject to production test [1]
Switched capacitance at the reference input	C_{AREFSW} CC	–	15	30	pF	not subject to production test [1]
Total capacitance at the reference input	C_{AREFT} CC	–	20	40	pF	not subject to production test [1]
Broken wire detection delay against VAGND[2]	t_{BWG} CC	–	–	50[3]		
Broken wire detection delay against VAREF[2]	t_{BWR} CC	–	–	50[4]		
Conversion time for 8-bit result[2]	t_{c8} CC	(10 + STC x t_{ADCI} + 2 x t_{SYS}				
Conversion time for 10-bit result[2]	t_{c10} CC	(12 + STC x t_{ADCI} + 2 x t_{SYS}				
Conversion time for 12-bit result[2]	t_{c12} CC	(16 + STC x t_{ADCI} + 2 x t_{SYS}				
Analog reference ground	V_{AGND} SR	V_{SS} - 0.05	–	1.5	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	–	V_{AREF}	V	[5]
Analog reference voltage	V_{AREF} SR	V_{AGND} + 1.0	–	V_{DDPB} + 0.05	V	

1) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation.

4.5 System Parameters

The following parameters specify several aspects which are important when integrating the XE161FU into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 24 Various System Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Short-term deviation of internal clock source frequency[1]	Δf_{INT} CC	-1	–	1	%	ΔT_J = ≤ 10°C
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Wakeup clock source frequency[2]	f_{WU} CC	400	–	700	kHz	FREQSEL= 00
		210	–	390	kHz	FREQSEL= 01
		140	–	260	kHz	FREQSEL= 10
		110	–	200	kHz	FREQSEL= 11
Startup time from power-on with code execution from Flash	t_{SPO} CC	1.4	1.9	2.4	ms	f_{WU} = 500 kHz
Startup time from stopover mode with code execution from PSRAM	t_{SSO} CC	11 / f_{WU}[3]	–	12 / f_{WU}[3]	µs	
Core voltage (PVC) supervision level	V_{PVC} CC	V_{LV} - 0.03	V_{LV}	V_{LV} + 0.07[4]	V	[5]
Supply watchdog (SWD) supervision level	V_{SWD} CC	V_{LV} - 0.10[6]	V_{LV}	V_{LV} + 0.15	V	voltage_range= lower [5]
		V_{LV} - 0.15	V_{LV}	V_{LV} + 0.15	V	voltage_range= upper [5]

1) The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.

2) This parameter is tested for the fastest and the slowest selection. The medium selections are not subject to production test - verified by design/characterization.

3) f_{WU} in MHz.

4.6 Flash Memory Parameters

The XE161FU is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XE161FU's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 27 Flash Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Parallel Flash module program/erase limit depending on Flash read activity	N_{PP} SR	–	–	1[1)]		$N_{FL\_RD} \leq 1$
Flash erase endurance for security pages	N_{SEC} SR	10	–	–	cycles	$t_{RET} \geq$ 20 years
Flash wait states[2)]	$N_{WSFLASH}$ SR	1	–	–		$f_{SYS} \leq$ 8 MHz
		2	–	–		$f_{SYS} \leq$ 13 MHz
		3	–	–		$f_{SYS} \leq$ 17 MHz
		4	–	–		$f_{SYS} >$ 17 MHz
Erase time per sector/page	t_{ER} CC	–	7[3)]	8.0	ms	
Programming time per page	t_{PR} CC	–	3[3)]	3.5	ms	
Data retention time	t_{RET} CC	20	–	–	years	$N_{ER} \leq$ 1,000 cycles
Drain disturb limit	N_{DD} SR	32	–	–	cycles	

4.7.2 Definition of Internal Timing

The internal operation of the XE161FU is controlled by the internal system clock f_{SYS}.

Because the system clock signal f_{SYS} can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate f_{SYS}. This must be considered when calculating the timing for the XE161FU.

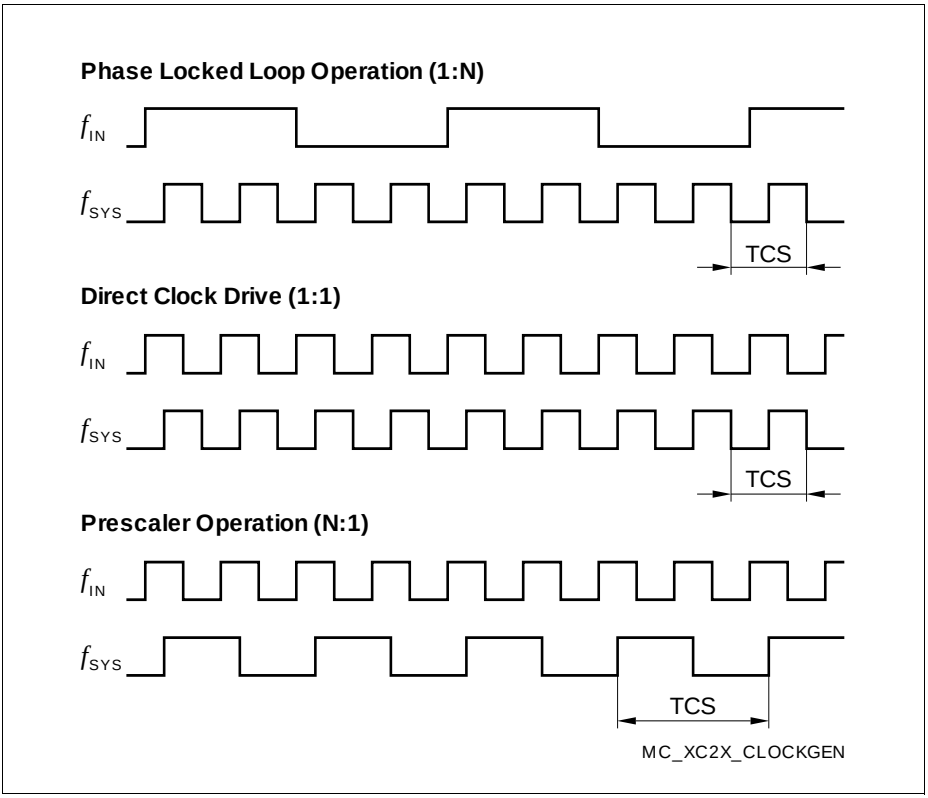

Figure 17 Generation Mechanisms for the System Clock

*Note: The example of PLL operation shown in **Figure 17** uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

Table 31 Standard Pad Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	0.8	mA	Driver_Strength = Medium
		–	–	1.0	mA	Driver_Strength = Strong
		–	–	0.15	mA	Driver_Strength = Weak
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	73 + 0.85 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	6 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Soft
		–	–	33 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	385 + 3.25 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and ΣI_{OH}) must remain below 25 mA.

4.7.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 32 is valid under the following conditions: C_L= 20 pF; SSC= master ; voltage_range= upper

Table 32 USIC SSC Master Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{SYS} - 8[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{SYS} - 6[1)]	–	–	ns	
Data output DOUT valid time	t_3 CC	-6	–	9	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-4	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 39 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

Table 39 JTAG Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	100[1]	–	–	ns	
TCK high time	t_2 SR	16	–	–	ns	
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[2]	t_8 CC	–	39	43	ns	
TDO high impedance to valid output from TCK falling edge[3][2]	t_9 CC	–	39	43	ns	
TDO valid output to high impedance from TCK falling edge[2]	t_{10} CC	–	39	43	ns	
TDO hold after TCK falling edge[2]	t_{18} CC	5	–	–	ns	

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \geq t_{SYS}$.

2) The falling edge on TCK is used to generate the TDO timing.

3) The setup time for TDO is given implicitly by the TCK cycle time.