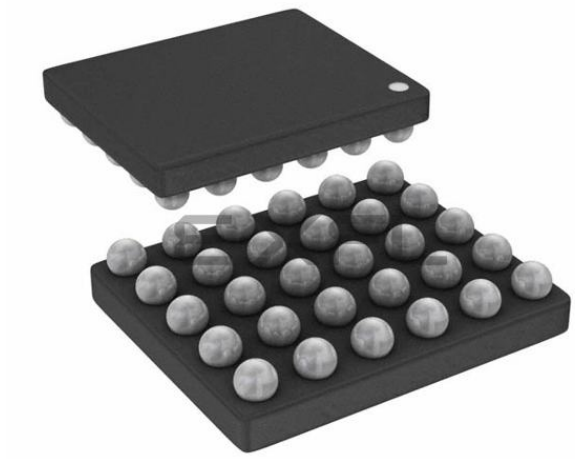
Lattice Semiconductor Corporation - ICE40UP3K-UWG30ITR Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	350
Number of Logic Elements/Cells	2800
Total RAM Bits	1130496
Number of I/O	21
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	30-UFBGA, WLCSP
Supplier Device Package	30-WLCSP (2.54x2.12)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40up3k-uwg30itr

Contents

Tables

Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, contact your local Lattice representative.

3. Architecture

3.1. Architecture Overview

The iCE40 UltraPlus family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I^2C controllers, two user configurable SPI controllers, blocks of sysMEM™ Embedded Block RAM (EBR) and Single Port RAM (SPRAM) surrounded by Programmable I/O (PIO). Figure 3.1 shows the block diagram of the iCE40UP5K device.

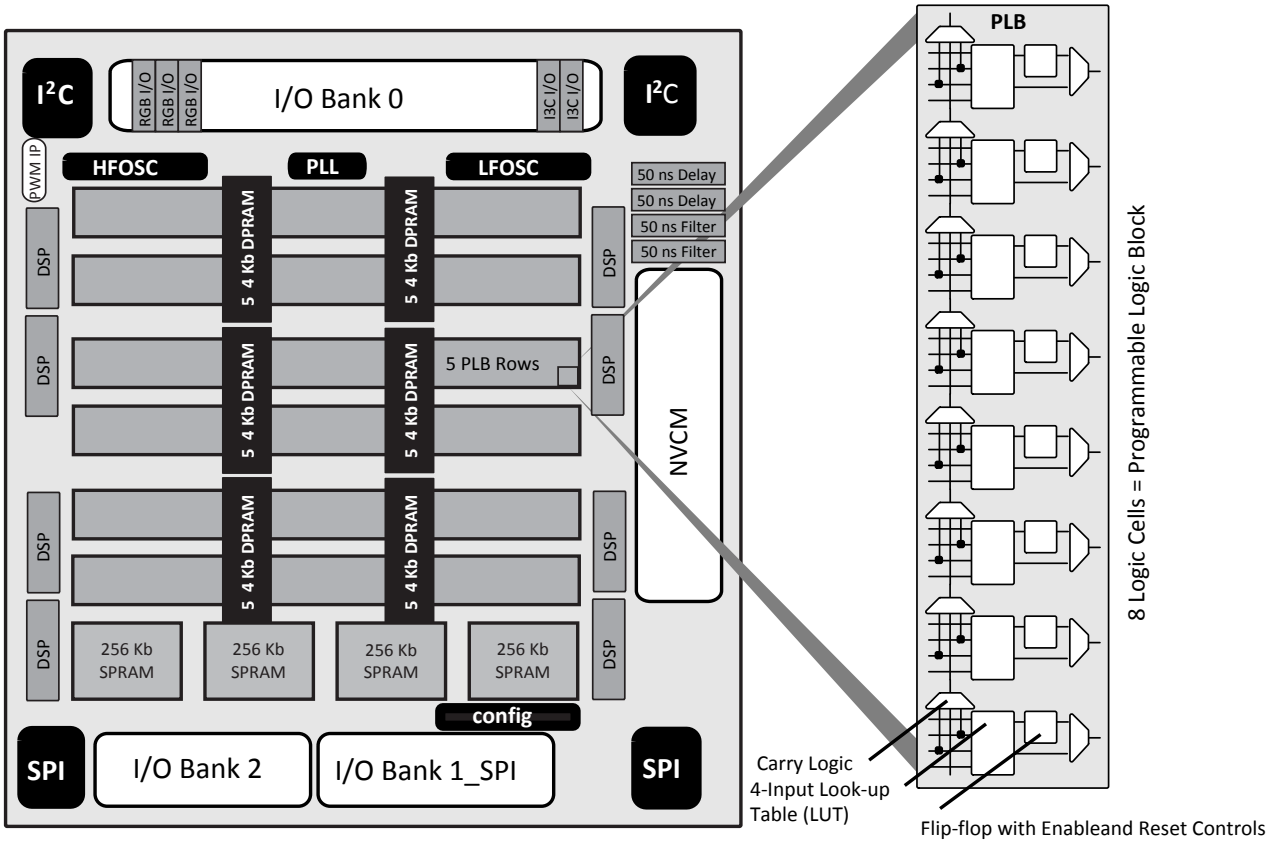


Figure 3.1. iCE40UP5K Device, Top View

The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 UltraPlus family, there are three sysIO banks, one on top and two at the bottom. User can connect some V_{CCIO}s together, if all the I/Os are using the same voltage standard. See the Power-up Supply Sequence section. The sysMEM EBRs are large 4 kb, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

In addition to the EBR, the iCE40 UltraPlus devices also feature four 256 kb SPRAM blocks that can be cascaded to create up to 1 Mb block. It is useful for temporary storage of large quantities of information.

Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

***Note**: If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

3.1.2. Routing

There are many resources provided in the iCE40 UltraPlus devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

3.1.3. Clock/Control Distribution Network

Each iCE40 UltraPlus device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 3.2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 3.2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	✓	✓	—
GBUF1		✓	—	✓
GBUF2		✓	✓	—
GBUF3		✓	—	✓
GBUF4		✓	✓	—
GBUF5		✓	—	✓
GBUF6		✓	✓	—
GBUF7		✓	—	✓

The maximum frequency for the global buffers are listed in Table 4.21.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 UltraPlus device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 UltraPlus device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

3.1.4. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 UltraPlus devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 UltraPlus global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 3.3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 UltraPlus PLL. There are two FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

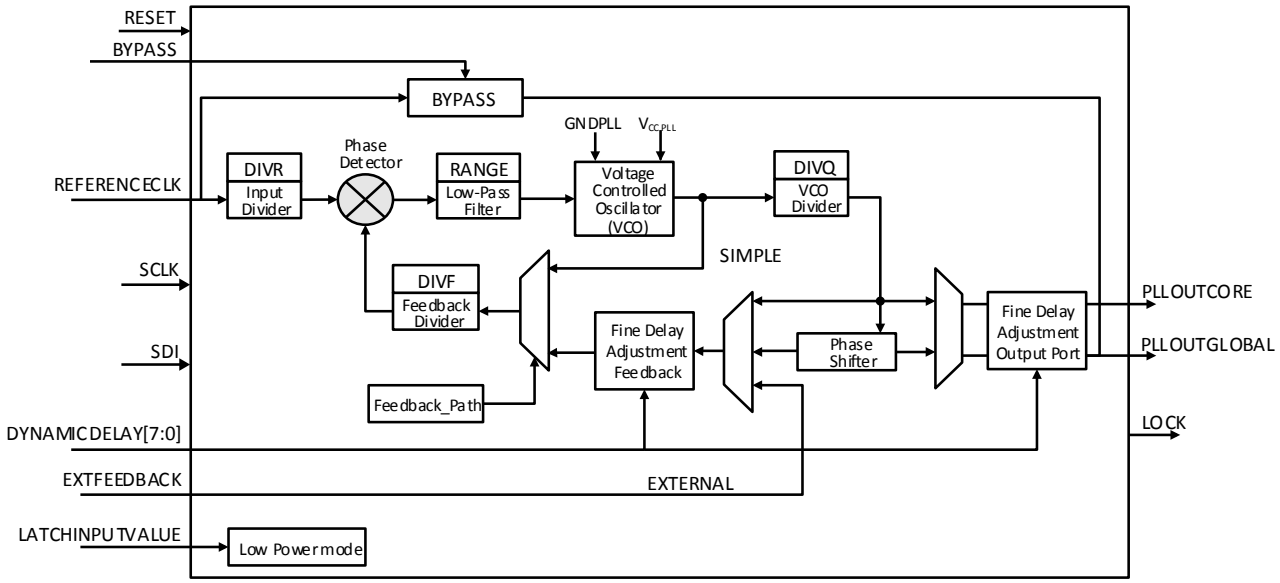


Figure 3.3. PLL Diagram

Table 3.3 provides signal descriptions of the PLL block.

Table 3.6. SPRAM Signal Descriptions

Signal Name	Direction	Description
ADDRESS[13:0]	Input	Address input
DATAIN[15:0]	Input	Write Data input
MASKWREN[3:0]	Input	Nibble WE control
WREN	Input	Write Enable
CHIPSELECT	Input	Enable SPRAM
CLOCK	Input	Clock input
STANDY	Input	Standby Mode
SLEEP	Input	Sleep Mode
POWEROFF	Input	Switch off power source to SPRAM
DATAOUT[15:0]	Output	Output Data

For further information on sysMEM SPRAM block, refer to TN1314, iCE40 SPRAM Usage Guide.

3.1.7. sysDSP

The iCE40 UltraPlus family provides an efficient sysDSP architecture that is very suitable for low-cost Digital Signal Processing (DSP) functions for mobile applications. Typical functions used in these applications are Multiply, Accumulate, and Multiply-Accumulate. The block can also be used for simple Add and Subtract functions.

iCE40 UltraPlus sysDSP Architecture Features

The iCE40 UltraPlus sysDSP supports many functions that include the following:

- Single 16-bit x 16-bit Multiplier, or two independent 8-bit x 8-bit Multipliers
- Optional independent pipeline control on Input Register, Output Register, and Intermediate Reg faster clock performance
- Single 32-bit Accumulator, or two independent 16-bit Accumulators
- Single 32-bit, or two independent 16-bit Adder/Subtracter functions, registered or asynchronous
- Cascadable to create wider Accumulator blocks

Figure 3.6 shows the block diagram of the sysDSP block. The block consists of the Multiplier section with a bypassable Output register, Input Register, and Intermediate register between Multiplier and AC timing to achieve the highest performance.

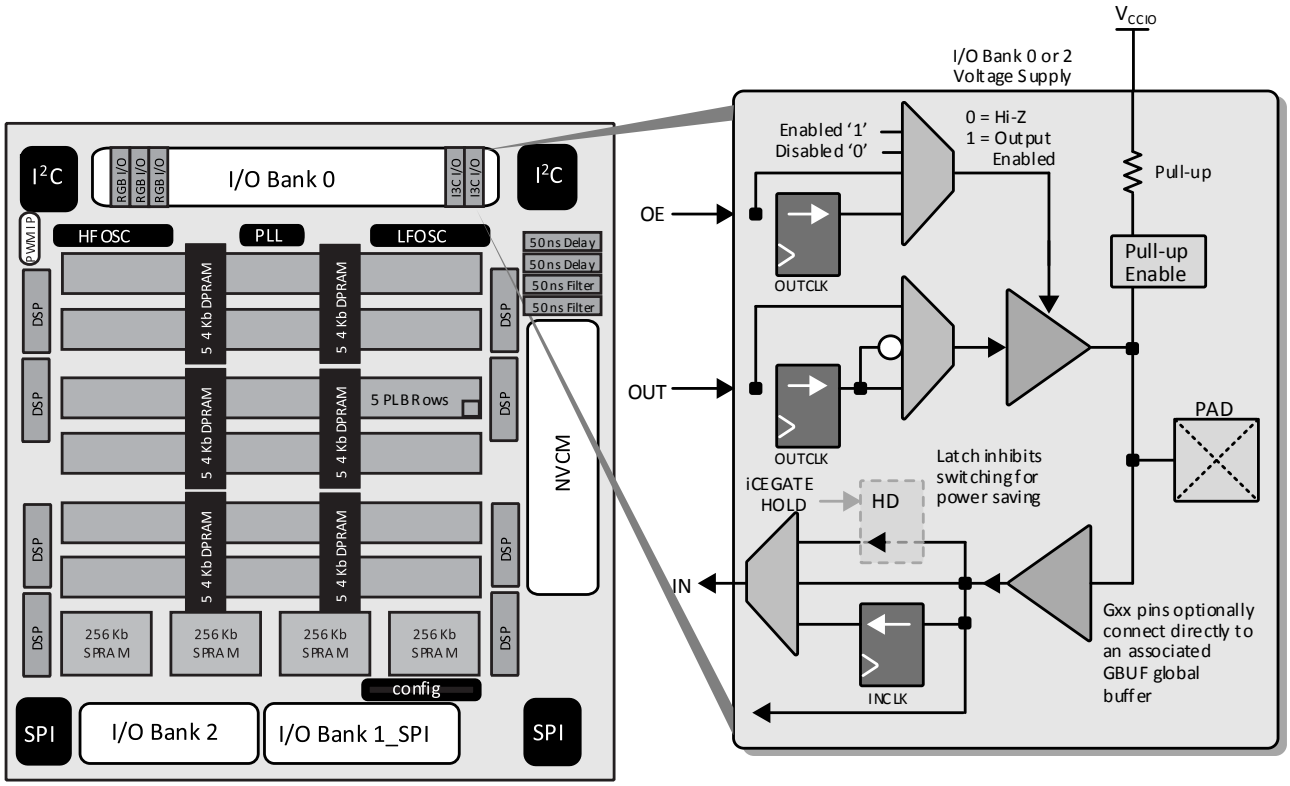


Figure 3.9. I/O Bank and Programmable I/O Cell

The PIO contains three blocks: an input register block, output register block iCEGate™ and tri-state register block. To save power, the optional iCEGate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers.

Figure 3.10 shows the input/output register block for the PIOs.

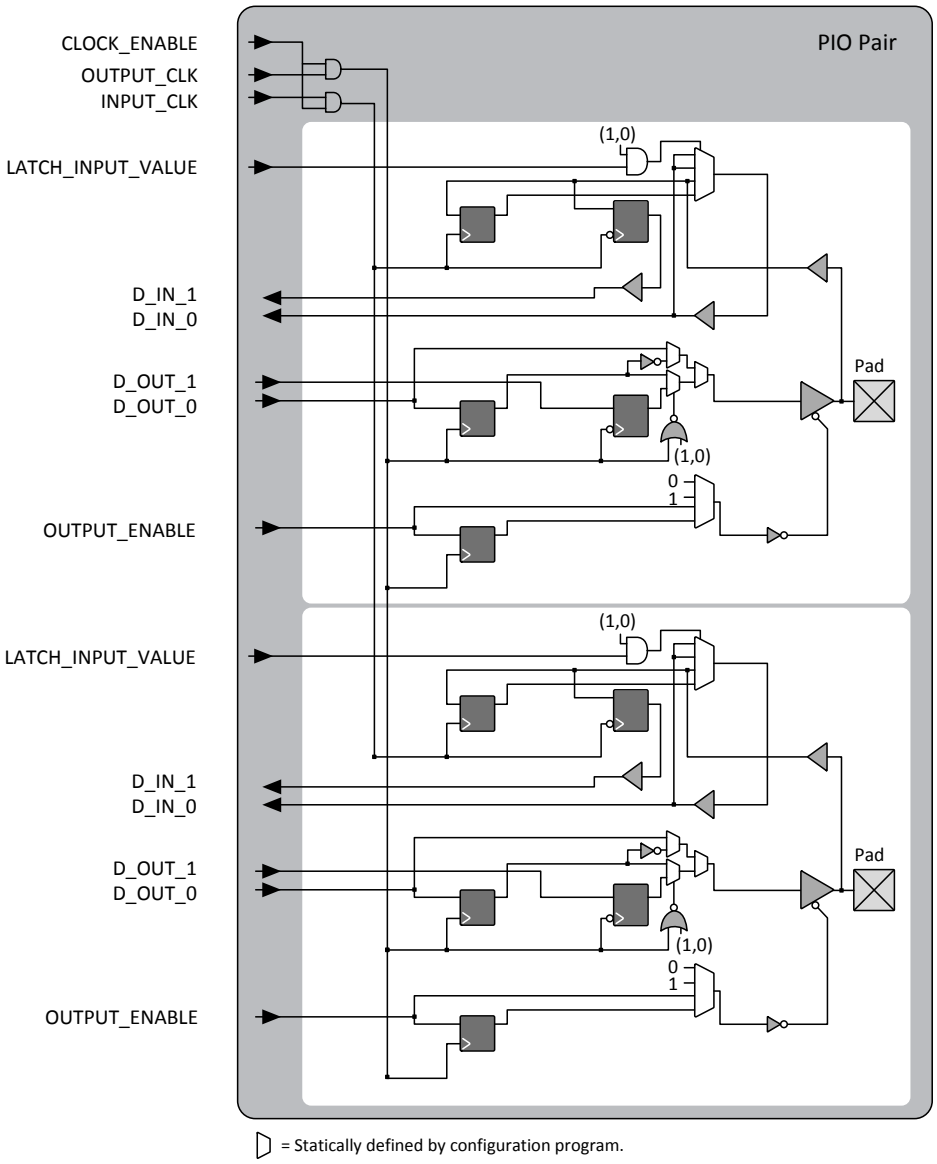


Figure 3.10. iCE I/O Register Block Diagram

Table 3.8. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

3.1.11. User I²C IP

The iCE40 UltraPlus devices have two I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The pins for the I²C interface are not pre-assigned. User can use any General Purpose I/O pins.

In each of the two cores, there are options to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I²C components.

When the IP core is configured as master, it will be able to control other devices on the I²C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 400 kHz data transfer speed
- General Call support
- Optionally delaying input or output data, or both
- Optional filter on SCL input

For further information on the User I²C, refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

3.1.12. User SPI IP

The iCE40 UltraPlus devices have two SPI IP cores. The pins for the SPI interface are not pre-assigned. User can use any General Purpose I/O pins. Both SPI IP cores can be configured as a SPI master or as a slave. When the SPI IP core is configured as a master, it controls the other SPI enabled devices connected to the SPI Bus. When SPI IP core is configured as a slave, the device will be able to interface to an external SPI master.

The SPI IP core supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer

For further information on the User SPI, refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

3.1.13. RGB High Current Drive I/O Pins

The iCE40 UltraPlus family devices offer multiple high current LED drive outputs in each device in the family to allow the iCE40 UltraPlus product to drive LED signals directly on mobile applications.

There are three outputs on each device that can sink up to 24 mA current. These outputs are open-drain outputs, and provides sinking current to an LED connecting to the positive supply. These three outputs are designed to drive the RBG LEDs, such as the service LED found in a lot of mobile devices. This RGB drive current is user programmable from 4 mA to 24 mA, in increments of 4 mA. This output functions as General Purpose I/O with open-drain when the high current drive is not needed.

3.1.14. RGB PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be used in the user design. This PWM IP provides the flexibility for user to dynamically change the modulation width of each of the RGB LED driver, which changes the color. Also, the user can dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the PWM IP, refer to TN1288, iCE40 LED Driver Usage Guide.

4. DC and Switching Characteristics

4.1. Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage V_{CC}	–0.5	1.42	V
Output Supply Voltage V_{CCIO}	–0.5	3.60	V
NVCM Supply Voltage V_{PP_2V5}	–0.5	3.60	V
PLL Supply Voltage V_{CCPLL}	–0.5	1.42	V
I/O Tri-state Voltage Applied	–0.5	3.60	V
Dedicated Input Voltage Applied	–0.5	3.60	V
Storage Temperature (Ambient)	–65	150	°C
Junction Temperature (T_J)	–65	125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	V_{PP_2V5} NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71[4]	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t_{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10.00	30.00	°C

Notes:

1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. See the Power-up Supply Sequence section. V_{CC} and V_{CCPLL} are recommended to be tied together to the same supply with an RC-based noise filter between them. Refer to TN1252, iCE40 Hardware Checklist.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration modes subject to the condition that none of the HFOSC/LFOSC and RGB LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

4.3. Power Supply Ramp Rates

Table 4.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies	0.6	10	V/ms

Notes:

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. See the Power-up Supply Sequence section below.

4.4. Power-On Reset

All iCE40 UltraPlus devices have on-chip Power-On-Reset (POR) circuitry to ensure proper initialization of the device. Only three supply rails are monitored by the POR circuitry as follows: (1) VCC, (2) SPI_VCCIO1 and (3) VPP_2V5. All other supply pins have no effect on the power-on reset feature of the device. Note that all supply voltage pins must be connected to power supplies for normal operation (including device configuration).

4.5. Power-up Supply Sequence

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5 V, or higher, before any subsequent power supplies in the sequence are applied.

1. **VCC** and **VCCPLL** should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the VCCPLL. Refer to TN1252, iCE40 Hardware Checklist.
2. **SPI_VCCIO1** should be the next supply, and can be applied any time after the previous supplies (VCC and VCCPLL) have reached as level of 0.5 V or higher.
3. **VPP_2V5** should be the next supply, and can be applied any time after previous supplies (VCC, VCCPLL and SPI_VCCIO1) have reached a level of 0.5 V or higher.
4. **Other Supplies** (VCCIO0 and VCCIO2) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (VCC and VCCPLL) have reached a level of 0.5 V or greater. There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are re-powered up again.

4.6. External Reset

When all power supplies have reached their minimum operating voltage defined in the Minimum Operation Condition Table, it is required to either keep CRESET_B LOW, or toggle CRESET_B from HIGH to LOW, for a duration of tCRESET_B, and release it to go HIGH, to start configuration download from either the internal NVCM or the external Flash memory. Figure 4.1 shows Power-Up sequence when SPI_VCCIO1 and VPP_2V5 are not connected together, and the CRESET_B signal triggers configuration download. shows when SPI_VCCIO1 and VPP_2V5 connected together. All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

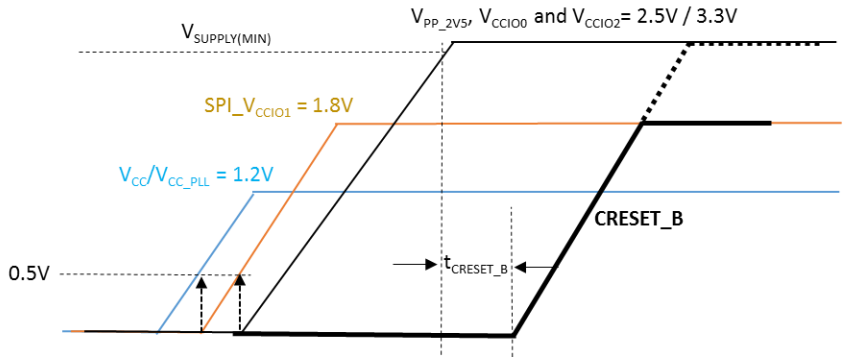


Figure 4.1. Power Up Sequence with SPE_VCCIO1 and VPP_2V5 Not Connected Together

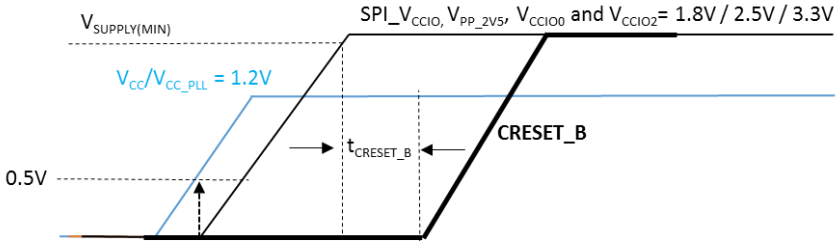


Figure 4.2. Power Up Sequence with All Supplies Connected Together to 1.8 V

4.7. Power-On-Reset Voltage Levels

Table 4.4. Power-On-Reset Voltage Levels

Symbol	Parameter		Min	Max	Unit
V_{PORUP}	Power-On-Reset ramp up trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5})	V_{CC}	0.62	0.92	V
		SPI_V_{CCIO1}	0.87	1.50	V
		V_{PP_2V5}	0.90	1.53	V
V_{PORDN}	Power-On-Reset ramp down trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5})	V_{CC}	—	0.79	V
		SPI_V_{CCIO1}	—	1.50	V
		V_{PP_2V5}	—	1.53	V

Note: These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

4.8. ESD Performance

Please contact Lattice Semiconductor for additional information.

4.15. Internal Oscillators (HFOSC, LFOSC)

Table 4.11. Internal Oscillators (HFOSC, LFOSC)

Parameter		Parameter Description	Spec/Recommended			Unit
Symbol	Conditions		Min	Typ	Max	
f_{CLKHF}	Commercial Temp	HFOSC clock frequency (t_J = 0 °C–85 °C)	-10%	48	10%	MHz
	Industrial Temp	HFOSC clock frequency (t_J = –40 °C–100 °C)	-20%	48	20%	MHz
f_{CLKLF}	—	LFOSC CLKK clock frequency	-10%	10	10%	kHz
DCH_{CLKHF}	Commercial Temp	HFOSC Duty Cycle (t_J = 0 °C–85 °C)	45	50	55	%
	Industrial Temp	HFOSC Duty Cycle (t_J = –40 °C–100 °C)	40	50	60	%
DCH_{CLKLF}	—	LFOSC Duty Cycle (Clock High Period)	45	50	55	%
Tsync_on	—	Oscillator output synchronizer delay	—	—	5	Cycles
Tsync_off	—	Oscillator output disable delay	—	—	5	Cycles

Note: Glitchless enabling and disabling OSC clock outputs.

4.16. sysI/O Recommended Operating Conditions

Table 4.12. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min	Typ	Max
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89

4.17. sysI/O Single-Ended DC Electrical Characteristics

Table 4.13. sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}* (mA)	I_{OH} Max (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO}+0.2 V	0.4	V_{CCIO} – 0.4	8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO}+0.2 V	0.4	V_{CCIO} – 0.4	6	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	V_{CCIO}+0.2 V	0.4	V_{CCIO} – 0.4	4	–4
					0.2	V_{CCIO} – 0.2	0.1	–0.1

4.20. sysDSP Timing

Over recommended operating conditions.

Table 4.17. sysDSP Timing

Parameter	Description	Min	Max	Unit
$f_{MAX8x8SMULT}$	Max frequency signed MULT8x8 bypassing pipeline register	50	—	MHz
$f_{MAX16x16SMULT}$	Max frequency signed MULT16x16 bypassing pipeline register	50	—	MHz

4.21. SPRAM Timing

Over recommended operating conditions.

Table 4.18. Single Port RAM Timing

Parameter	Description	Min	Max	Unit
$f_{MAXSRAM}$	Max frequency SPRAM (4/8/16-bit Read and Write)	70	—	MHz

4.22. Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

4.23. Maximum sysIO Buffer Performance

Table 4.19. Maximum sysIO Buffer Performance

I/O Standard	Max Speed	Unit
Inputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz
LVCMOS12	70	MHz

Note: Measured with a toggling pattern.

4.24. iCE40 UltraPlus Family Timing Adders

Over recommended commercial operating conditions.

Table 4.20. iCE40 UltraPlus Family Timing Adders

Buffer Type	Description	Timing (Typ)	Units
Input Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	ns
Output Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	-0.12	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	ns
LVCMOS12	LVCMOS, V_{CCIO} = 1.2 V	5.38	ns

Notes:

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. Commercial timing numbers are shown.

4.26. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 4.22. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Unit
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)	—	10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)	—	16	275	MHz
f_{VCO}	PLL VCO Frequency	—	533	1066	MHz
f_{PFD}[3]	Phase Detector Input Frequency	—	10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	40	60	%
t_{PH}	Output Phase Accuracy	—	—	±12	deg
t_{OPJIT}[1, 5, 6]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	450	ps p-p
		f_{OUT} < 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-Cycle Jitter	f_{OUT} >= 100 MHz	—	750	ps p-p
		f_{OUT} < 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} >= 25 MHz	—	275	ps p-p
		f_{PFD} < 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time	—	—	50	µs
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	f_{PFD} ≥ 20 MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable	—	—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width	—	100	—	ns
t_{RST}	RESET Pulse Width	—	10	—	ns
t_{RSTREC}	RESET Recovery Time	—	10	—	µs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width	—	100	—	VCO Cycles

Notes:

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

4.27. SPI Master or NVCM Configuration Time

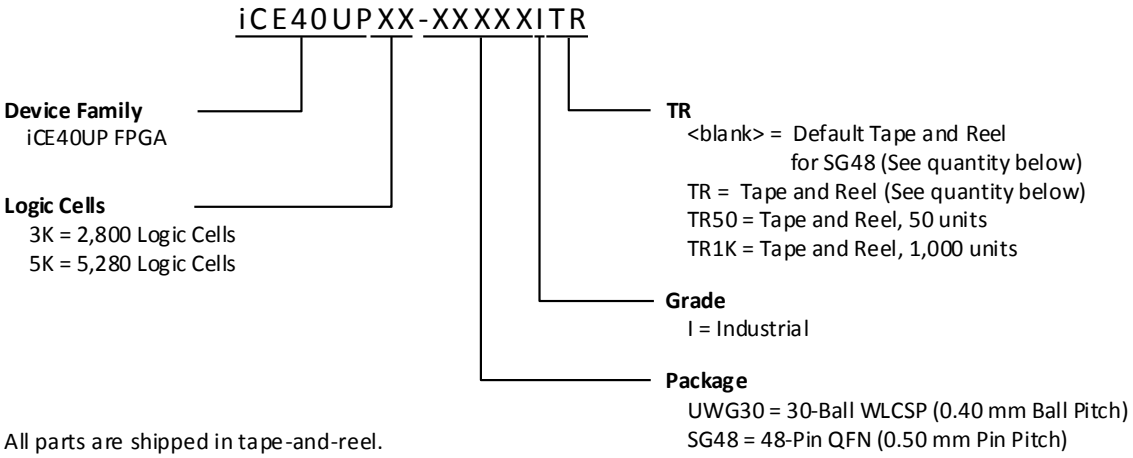
Table 4.23. SPI Master or NVCM Configuration Time

Symbol	Parameter	Conditions	Max	Unit
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	140	ms
		All devices – Medium frequency	50	ms
		All devices – High frequency	26	ms

Notes:

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

5.3. iCE40UP Part Number Description



All parts are shipped in tape-and-reel.

5.3.1. Tape and Reel Quantity

Package	TR Quantity
UWG30	5,000
SG48	2,000

5.4. Ordering Part Numbers

5.4.1. Industrial

Part Number	LUTs	Supply Voltage	Package	Pins	Temperature
iCE40UP3K-UWG30ITR	2800	1.2 V	Halogen-Free WLCSP	30	IND
iCE40UP3K-UWG30ITR1K	2800	1.2 V	Halogen-Free WLCSP	30	IND
iCE40UP3K-UWG30ITR50	2800	1.2 V	Halogen-Free WLCSP	30	IND
iCE40UP5K-SG48I	5280	1.2 V	Halogen-Free QFN	48	IND
iCE40UP5K-SG48ITR50	5280	1.2 V	Halogen-Free QFN	48	IND
iCE40UP5K-UWG30ITR	5280	1.2 V	Halogen-Free WLCSP	30	IND
iCE40UP5K-UWG30ITR1K	5280	1.2 V	Halogen-Free WLCSP	30	IND
iCE40UP5K-UWG30ITR50	5280	1.2 V	Halogen-Free WLCSP	30	IND

Supplemental Information

For Further Information

A variety of technical documents for the iCE40 UltraPlus family are available on the Lattice web site.

- TN1248, iCE40 Programming and Configuration
- TN1274, iCE40 SPI/I2C Hardened IP Usage Guide
- TN1276, Advanced iCE40 SPI/I2C Hardened IP Usage Guide
- TN1250, Memory Usage Guide for iCE40 Devices
- TN1251, iCE40 sysCLOCK PLL Design and Usage Guide
- TN1252, iCE40 Hardware Checklist
- TN1288, iCE40 LED Driver Usage Guide
- TN1295, DSP Function Usage Guide for iCE40 Devices
- TN1296, iCE40 Oscillator Usage Guide
- TN1314, iCE40 SPRAM Usage Guide
- iCE40 UltraPlus Pinout Files
- iCE40 UltraPlus Pin Migration Files
- Thermal Management document
- Package Diagrams
- Lattice design tools

Revision History

Date	Version	Section	Change Summary
February 2017	1.3	All	— Changed document status from Advance to Preliminary. — Updated footer.
		Architecture	— Corrected link to TN1288, iCE40 LED Driver Usage Guide. — Added link to TN1314, iCE40 SPRAM Usage Guide.
		DC and Switching Characteristics	— Updated Typ V_{CC}=1.2 V values for $I_{PP\_2VSPEAK}$ and $I_{COOPEAK}$ in Table 4.6. Supply Current. — Added Min value for $f_{MAXSRAM}$ to Table 4.18. Single Port RAM Timing. — Added LVCMOS12 information to Table 4.19. Maximum sysIO Buffer Performance and Table 4.20. iCE40 UltraPlus Family Timing Adders. — Updated Table 4.21. iCE40 UltraPlus External Switching Characteristics. Revised Max values for t_{ISKEW_GBUF}, t_{SKEW_IO}, t_{CO}, t_{COPLL}, and Min values for t_{SUPLL}, t_{HPLL}. — Added Max values to Table 4.23. SPI Master or NVCM Configuration Time.
		Pinout Information	— Updated TR description in the iCE40UP Part Number Description section. — Updated part number information in the Ordering Part Numbers section.
		Supplemental Information	— Corrected link to TN1288, iCE40 LED Driver Usage Guide. — Added link to TN1314, iCE40 SPRAM Usage Guide. — Added link to Package Diagrams.
June 2016	1.2	All	Updated template.
		Introduction	Added QFN package in features list.
		Product Family	Added packages to Table 2.1 iCE40 UltraPlus Family Selection Guide. Added information on RGB PWM IP in Overview.
		Architecture	— Performed minor editorial changes. — Added information on 256 kb SPRAM blocks. — Changed headings in Table 3.2. Global Buffer (GBUF) Connections to Programmable Logic Blocks. — Corrected VCCPLL format in Figure 3.3. PLL Diagram. — Updated note in Table 3.4. sysMEM Block Configurations. — Added reference to TN1314, iCE40 SPRAM Usage Guide. — Revised sysIO Buffer Banks information. — Corrected VCCIO format in Figure 3.9. I/O Bank and Programmable I/O Cell. — Revised Typical I/O Behavior During Power-up information. — Revised Supported Standards information. — Revised heading in Table 3.9. Supported Input Standards. — Revised heading and removed LVCMOS12 in Table 3.10. Supported Output Standards. — Revised HFOSC information in On-Chip Oscillator section. — Removed "An RGB PWM IP is also offered in the family." in RGB High Current Drive I/O Pins section.