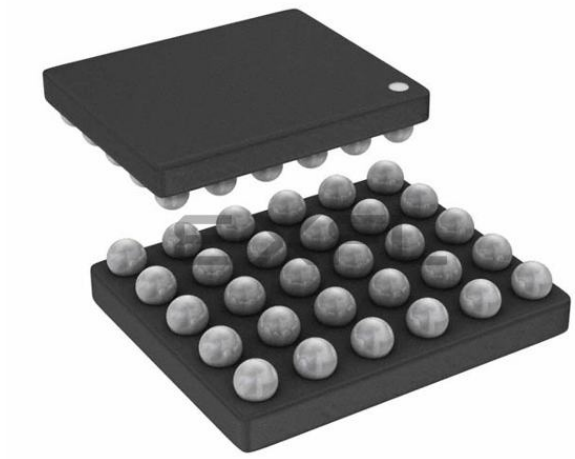
Lattice Semiconductor Corporation - ICE40UP3K-UWG30ITR1K Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	350
Number of Logic Elements/Cells	2800
Total RAM Bits	1130496
Number of I/O	21
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	30-UFBGA, WLCSP
Supplier Device Package	30-WLCSP (2.54x2.12)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40up3k-uwg30itr1k

Contents

Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, contact your local Lattice representative.

3. Architecture

3.1. Architecture Overview

The iCE40 UltraPlus family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I^2C controllers, two user configurable SPI controllers, blocks of sysMEM™ Embedded Block RAM (EBR) and Single Port RAM (SPRAM) surrounded by Programmable I/O (PIO). Figure 3.1 shows the block diagram of the iCE40UP5K device.

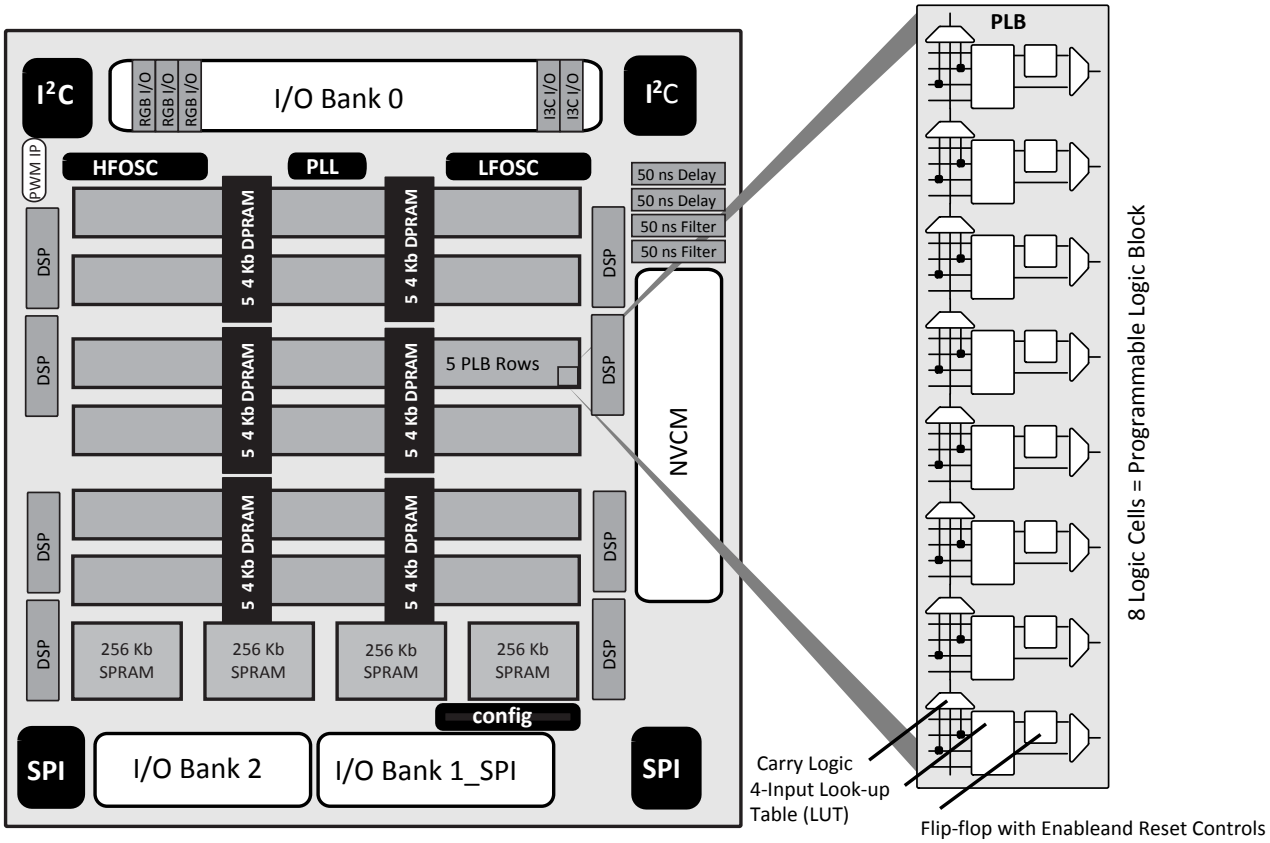

Figure 3.1. iCE40UP5K Device, Top View

The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 UltraPlus family, there are three sysIO banks, one on top and two at the bottom. User can connect some V_{CCIO}s together, if all the I/Os are using the same voltage standard. See the Power-up Supply Sequence section. The sysMEM EBRs are large 4 kb, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

In addition to the EBR, the iCE40 UltraPlus devices also feature four 256 kb SPRAM blocks that can be cascaded to create up to 1 Mb block. It is useful for temporary storage of large quantities of information.

Table 3.3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLLOUT output. 0 – PLL generated signal 1 – REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

3.1.5. sysMEM Embedded Block RAM Memory

Larger iCE40 UltraPlus device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as listed in Table 3.4.

Table 3.4. sysMEM Block Configurations

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4 k)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4 k)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4 k)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4 k)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

Note: For iCE40 UltraPlus, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock and falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses failing-edge clocks on both Read and Write.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 3.4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

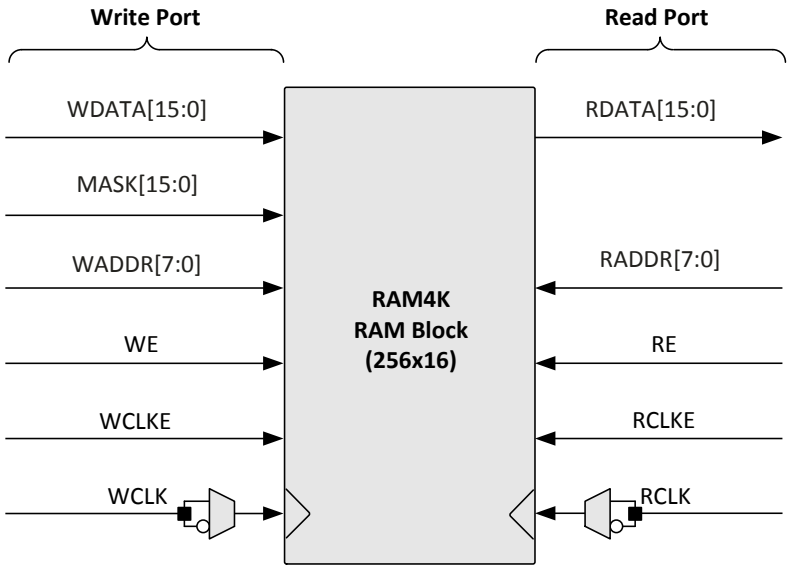

Figure 3.4. sysMEM Memory Primitives

Table 3.5 lists the EBR signals.

Table 3.5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 – Write bit 1 – Do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.

RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, refer to TN1250, Memory Usage Guide for iCE40 Devices.

3.1.6. sysMEM Single Port RAM Memory (SPRAM)

The SPRAM block is implemented to be accessed only as single port. Each block of SPRAM is designed to be 16K x 16 (256 kbits) in size. See Figure 3.5.

SPRAM Data Width

The SPRAM is designed with fixed 16-bit data width. However, the block contains nibble mask control on the write input that allows the user logic to operate the SPRAM as x4 or x8 with this control on the write side, and user logic to select which nible/byte in the read side.

SPRAM Initialization and ROM Operation

There is no pre-load into the SPRAM during device configuration, therefore, the SPRAM is not initialized after configuration.

SPRAM Cascading

Deeper SPRAM can be created using multiple SPRAM blocks, up to four blocks (64K x 16)

SPRAM Power Modes

There are three power modes in the SPRAM that the users can select during normal operation. This reduces the SPRAM block power when it Is not needed, allow lower power consumption in an always-on application. These modes are:

- **Standby Mode**: SPRAM stops all activity, and SPRAM freezes in its current state. Memory contents are retained, memory outputs are retained, and all register contents are retained.
- **Sleep Mode**: SPRAM block is shut down on all peripheral circuit, except the memory core. Memory contents are retained, memory outputs and register contents are clear and become unknown.
- **Power Off Mode**: Power source to the SPRAM is disconnected. This is the lowest power state. Memory contents are lost. Memory outputs are unknown.

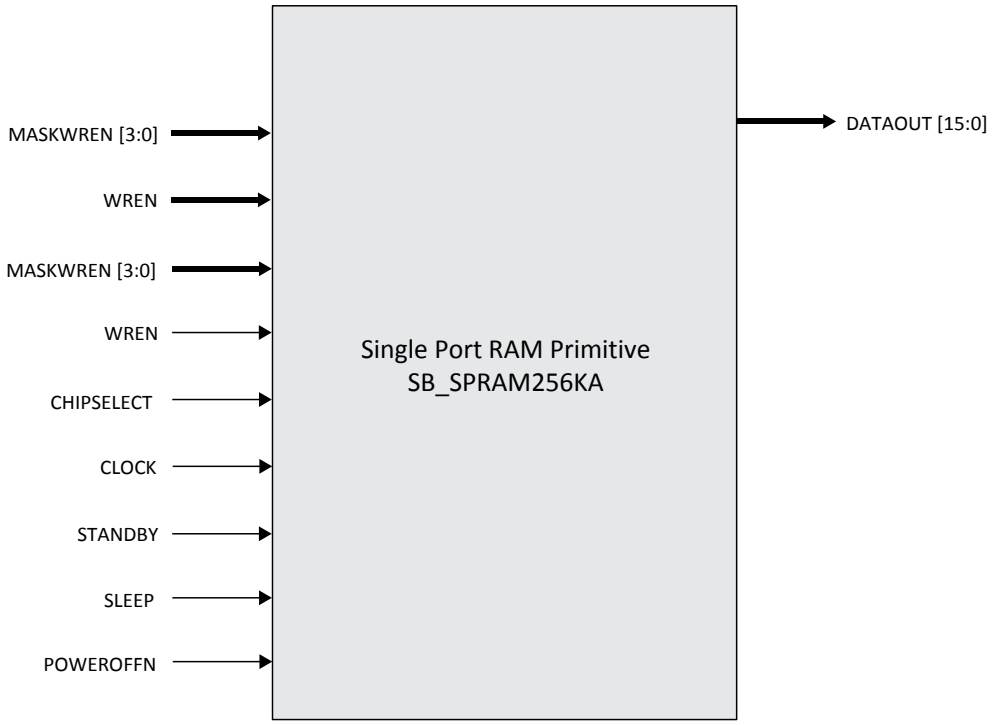

Figure 3.5. SPRAM Primitive

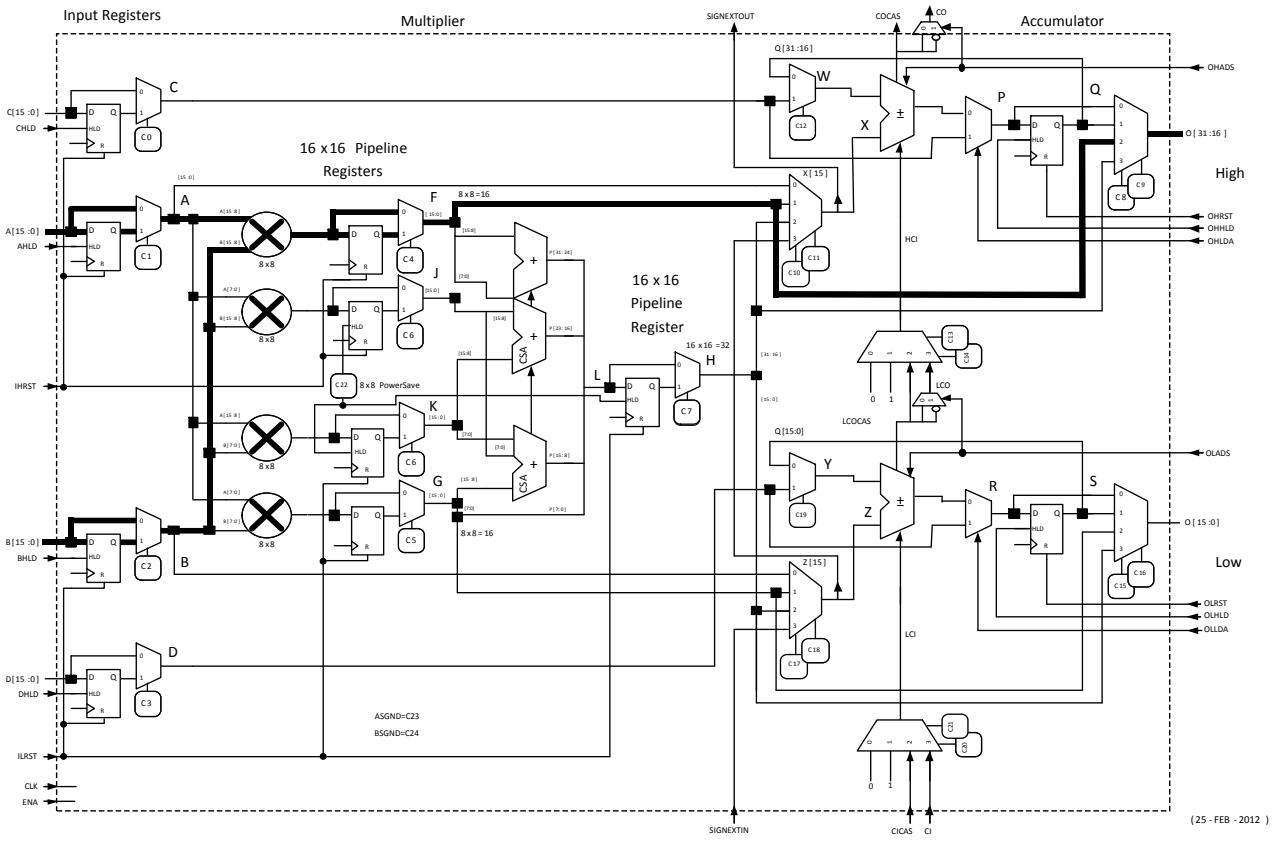

Figure 3.7. sysDSP 8-bit x 8-bit Multiplier

Figure 3.8 shows the path for an 16-bit x 16-bit Multiplier using the upper half of sysDSP block.

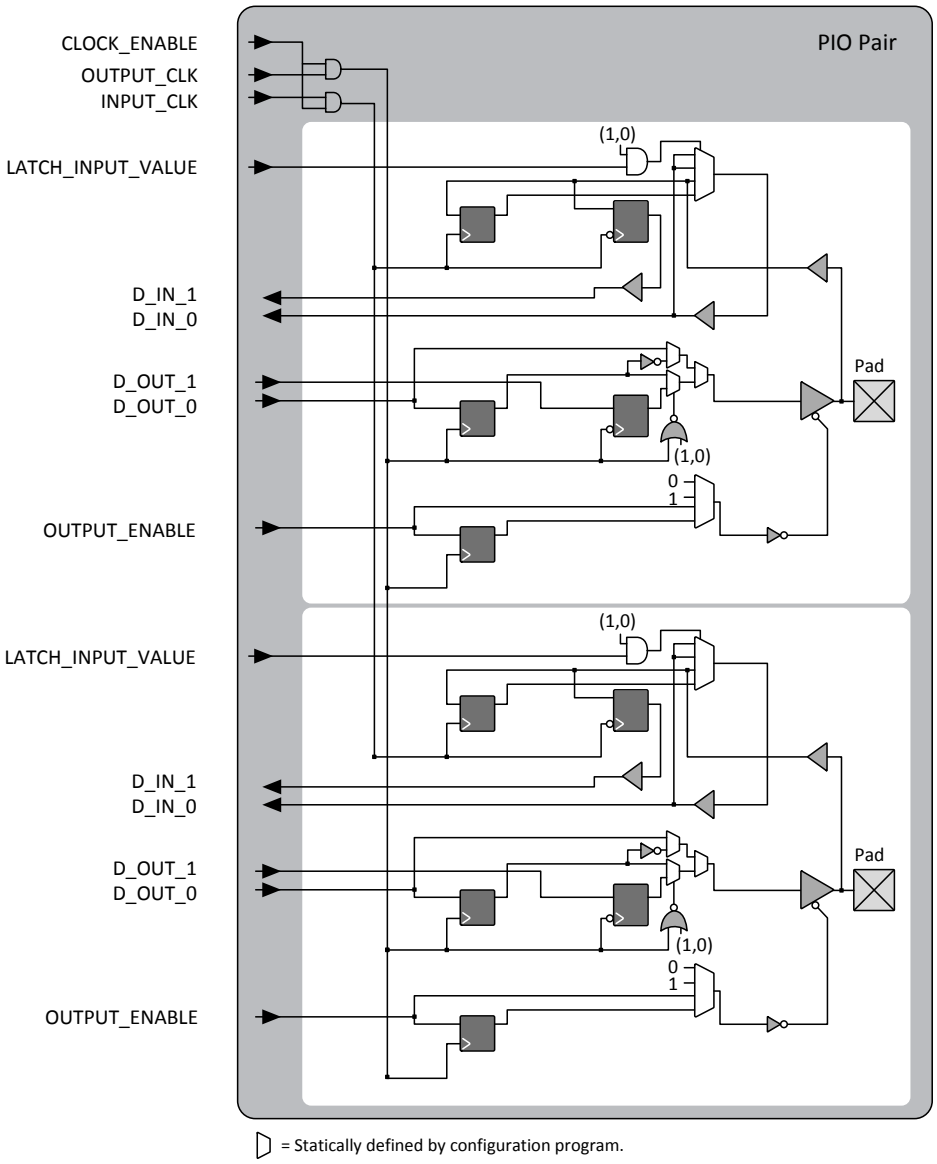

Figure 3.10. iCE I/O Register Block Diagram

Table 3.8. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

3.1.9. sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems with LVCMOS interfaces.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, SPI_V_{CCIO1} and V_{PP_2V5} reach the level defined in Table 4.4. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins maintain the pre-configuration state until V_{CC}, SPI_V_{CCIO1} and V_{PP_2V5} reach the defined levels. The I/Os take on the software user-configured settings only after POR signal is deactivated and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40 UltraPlus sysIO buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8 V, 2.5 V, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 3.9 and Table 3.10 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 UltraPlus devices.

Differential Comparators

The iCE40 UltraPlus devices provide differential comparator on pairs of I/O pins. These comparators are useful in some mobile applications. See the Pin Information Summary section on page 44 to locate the corresponding paired I/Os with differential comparators.

Table 3.9. Supported Input Standards

I/O Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	Yes	—	—
LVCMOS25	—	Yes	—
LVCMOS18	—	—	Yes

Table 3.10. Supported Output Standards

I/O Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18	1.8 V

3.1.10. On-Chip Oscillator

The iCE40 UltraPlus devices feature two different frequency Oscillator. One is tailored for low-power operation that runs at low frequency (LFOSC). Both Oscillators are controlled with internally generated current.

The LFOSC runs at nominal frequency of 10 kHz. The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option. The LFOSC can be used to perform all always-on functions, with the lowest power possible. The HFOSC can be enabled when the always-on functions detect a condition that would need to wake up the system to perform higher frequency functions.

3.1.15. Non-Volatile Configuration Memory

All iCE40 UltraPlus devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, refer to TN1248, iCE40 Programming and Configuration.

3.2. iCE40 UltraPlus Programming and Configuration

This section describes the programming and configuration of the iCE40 UltraPlus family.

3.2.1. Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_V_{CCIO1} power supply.

3.2.2. Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 UltraPlus, refer to TN1248, iCE40 Programming and Configuration.

3.2.3. Power Saving Options

The iCE40 UltraPlus devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 3.11 describes the function of these features.

Table 3.11. iCE40 UltraPlus Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

4.3. Power Supply Ramp Rates

Table 4.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies	0.6	10	V/ms

Notes:

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. See the Power-up Supply Sequence section below.

4.4. Power-On Reset

All iCE40 UltraPlus devices have on-chip Power-On-Reset (POR) circuitry to ensure proper initialization of the device. Only three supply rails are monitored by the POR circuitry as follows: (1) VCC, (2) SPI_VCCIO1 and (3) VPP_2V5. All other supply pins have no effect on the power-on reset feature of the device. Note that all supply voltage pins must be connected to power supplies for normal operation (including device configuration).

4.5. Power-up Supply Sequence

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5 V, or higher, before any subsequent power supplies in the sequence are applied.

1. **VCC** and **VCCPLL** should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the VCCPLL. Refer to TN1252, iCE40 Hardware Checklist.
2. **SPI_VCCIO1** should be the next supply, and can be applied any time after the previous supplies (VCC and VCCPLL) have reached as level of 0.5 V or higher.
3. **VPP_2V5** should be the next supply, and can be applied any time after previous supplies (VCC, VCCPLL and SPI_VCCIO1) have reached a level of 0.5 V or higher.
4. **Other Supplies** (VCCIO0 and VCCIO2) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (VCC and VCCPLL) have reached a level of 0.5 V or greater. There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are re-powered up again.

4.6. External Reset

When all power supplies have reached their minimum operating voltage defined in the Minimum Operation Condition Table, it is required to either keep CRESET_B LOW, or toggle CRESET_B from HIGH to LOW, for a duration of tCRESET_B, and release it to go HIGH, to start configuration download from either the internal NVCM or the external Flash memory. Figure 4.1 shows Power-Up sequence when SPI_VCCIO1 and VPP_2V5 are not connected together, and the CRESET_B signal triggers configuration download. shows when SPI_VCCIO1 and VPP_2V5 connected together. All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

4.20. sysDSP Timing

Over recommended operating conditions.

Table 4.17. sysDSP Timing

Parameter	Description	Min	Max	Unit
$f_{MAX8x8SMULT}$	Max frequency signed MULT8x8 bypassing pipeline register	50	—	MHz
$f_{MAX16x16SMULT}$	Max frequency signed MULT16x16 bypassing pipeline register	50	—	MHz

4.21. SPRAM Timing

Over recommended operating conditions.

Table 4.18. Single Port RAM Timing

Parameter	Description	Min	Max	Unit
$f_{MAXSRAM}$	Max frequency SPRAM (4/8/16-bit Read and Write)	70	—	MHz

4.22. Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

4.23. Maximum sysIO Buffer Performance

Table 4.19. Maximum sysIO Buffer Performance

I/O Standard	Max Speed	Unit
Inputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz
LVCMOS12	70	MHz

Note: Measured with a toggling pattern.

4.24. iCE40 UltraPlus Family Timing Adders

Over recommended commercial operating conditions.

Table 4.20. iCE40 UltraPlus Family Timing Adders

Buffer Type	Description	Timing (Typ)	Units
Input Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	ns
Output Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	-0.12	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	ns
LVCMOS12	LVCMOS, V_{CCIO} = 1.2 V	5.38	ns

Notes:

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. Commercial timing numbers are shown.

4.25. iCE40 UltraPlus External Switching Characteristics

Over recommended commercial operating conditions.

Table 4.21. iCE40 UltraPlus External Switching Characteristics

Parameter	Description	Device	Min	Max	Unit
Clocks					
Global Clock					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All Devices	—	185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All Devices	2	—	ns
t_{ISKEW_GBUF}	Global Buffer Clock Skew Within a Device	All Devices	—	530	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All Devices	—	9.0	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)*					
t_{SKEW_IO}	Data bus skew across a bank of IOs	All Devices	—	510	ps
t_{CO}	Clock to Output – PIO Output Register	All Devices	—	10.0	ns
t_{SU}	Clock to Data Setup – PIO Input Register	All Devices	–0.5	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	All Devices	5.55	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)					
t_{COPLL}	Clock to Output – PIO Output Register	All Devices	—	2.4	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	All Devices	7.3	—	ns
t_{HPLL}	Clock to Data Hold – PIO Input Register	All Devices	–1.1	—	ns

***Note**: All the data is from the worst case.

4.28. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 4.24. sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
All Configuration Mode						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 UltraPlus device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{SU}	CCLK setup time		6.16	—	—	ns
t_{HD}	CCLK hold time		1	—	—	ns

Notes:

1. Supported with 1.2 V V_{CC} and at 25 °C.
2. Extended range f_{MAX} Write operations support up to 53 MHz with 1.2 V V_{CC} and at 25 °C.
3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.

5. Pinout Information

5.1. Signal Descriptions

5.1.1. Power Supply Pins

Signal Name	Function	I/O	Description
V_{CC}	Power	—	Core Power Supply
V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	Power	—	Power for I/Os in Bank 0, 1, and 2.
V_{PP_2V5}	Power	—	Power for NVCM programming and operations.
V_{CCPLL}	Power	—	Power for PLL.
GND	GROUND	—	Ground
GND_LED	GROUND	—	Ground for LED drivers. Should connect to GND on board.

5.1.2. Configuration Pins

Signal Name		Function	I/O	Description
General I/O	Shared Function			
CRESET_B	—	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kΩ pull-up to SPI_V_{CCIO1}.
IOB_xxx	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO1}.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function. In 30-pin WLCSP, this pin connects to IOB_12a, which also is shared as global signal G4 in user mode.

5.1.3. Configuration SPI Pins

Signal Name		Function	I/O	Description
General I/O	Shared Function			
IOB_34a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
IOB_32a	SPI_SO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

RGB1	—	General I/O	Open-Drain I/O	In user mode, when RGB function is not used, this pin can be connected to any user logic and used as open-drain I/O. This pin is located in Bank 0.
		LED	Open-Drain Output	In user mode, when using RGB function, this pin can be programmed as open drain 24 mA output to drive external LED.
RGB2	—	General I/O	Open-Drain I/O	In user mode, when RGB function is not used, this pin can be connected to any user logic and used as open-drain I/O. This pin is located in Bank 0.
		LED	Open-Drain Output	In user mode, when using RGB function, this pin can be programmed as open drain 24 mA output to drive external LED.
PIOT_xx	—	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location). These pins are located in Bank 0.
PIOB_xx	—	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location). Pins with xx <= 9 are located in Bank 2, pins with xx> are located in Bank 1.

5.2. Pin Information Summary

Pin Type		iCE40UP3K	iCE40UP5K	
		UWG30	UWG30	SG48
General Purpose I/O Per Bank	Bank 0	7	7	17
	Bank 1	10	10	14
	Bank 2	4	4	8
Total General Purpose I/Os		21	21	39
V_{CC}		1	1	2
V_{CCIO}	Bank 0	1	1	1
	Bank 1	1	1	1
	Bank 2	1	1	1
V_{CCPLL}		1	1	1
V_{PP_2V5}		1	1	1
Dedicated Config Pins		1	1	2
GND		2	2	0[1]
Total Balls		30	30	48

Note:

1. 48-pin QFN package (SG48) requires the package paddle to be connected to GND.

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

		DC and Switching Characteristics	— Added the following figures: • Figure 4.1. Power Up Sequence with SPE_VCCIO1 and VPP_2V5 Not Connected Together. • Figure 4.2. Power Up Sequence with All Supplies Connected Together to 1.8 V. — Updated note in Table 4.5. DC Electrical Characteristics. — Added note in Table 4.6. Supply Current. — Revised User SPI Specifications 1, 2 section. • Removed symbols. • Added notes. — Revised Table 4.11. Internal Oscillators (HFOSC, LFOSC). — Removed note in Table 4.13. sysI/O Single-Ended DC Electrical Characteristics. — Changed to Lattice Design Software tool in Table 4.15. Pin-to-Pin Performance (LVCMOS25). — Changed to Lattice Design Software tool and revised note in Table 4.16. Register-to-Register Performance. — Added sysDSP Timing section. — Added SPRAM Timing section. — Removed LVCMOS12 and added timing values in Table 4.19. Maximum IO Buffer Performance. — Removed LVCMOS12 and added timing values in Table 4.20. iCE40 UltraPlus Family Timing Adders. — Revised max values in Table 4.23. SPI Master or NVCM Configuration Time. — Removed TBD conditions in Table 4.24. sysCONFIG Port Timing Specifications. Revised t_{HD} parameter. — Revised Table 4.25. High Current RGB LED and IR LED Drive.
		Pinout Information	— General update to Signal Descriptions section. — Updated the iCE40UP Part Number Description section. Added FGW49 package. — Added OPNs.
		Supplemental Information	Added reference to TN1314, iCE40 SPRAM Usage Guide.
September 2015	1.1	Architecture	Updated Architecture section. Replaced iCE5UP with iCE40UP.
		Pinout Information	Updated Pin Information Summary section. — Replaced iCE5UP with iCE40UP. — Replaced SWG30 with UWG30.
		Ordering Information	Updated iCE40UP Part Number Description section. — Replaced iCE5UP with iCE40UP. — Replaced SWG30 with UWG30.
			Updated Ordering Part Numbers section. Replaced the table of part
		Further Information	Removed reference to Schematic Symbols.
August 2015	1.0	All	Initial release.