Lattice Semiconductor Corporation - ICE40UP3K-UWG30ITR50 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	350
Number of Logic Elements/Cells	2800
Total RAM Bits	1130496
Number of I/O	21
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	30-UFBGA, WLCSP
Supplier Device Package	30-WLCSP (2.54x2.12)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40up3k-uwg30itr50

Contents

Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, contact your local Lattice representative.

3.1.4. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 UltraPlus devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 UltraPlus global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 3.3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 UltraPlus PLL. There are two FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

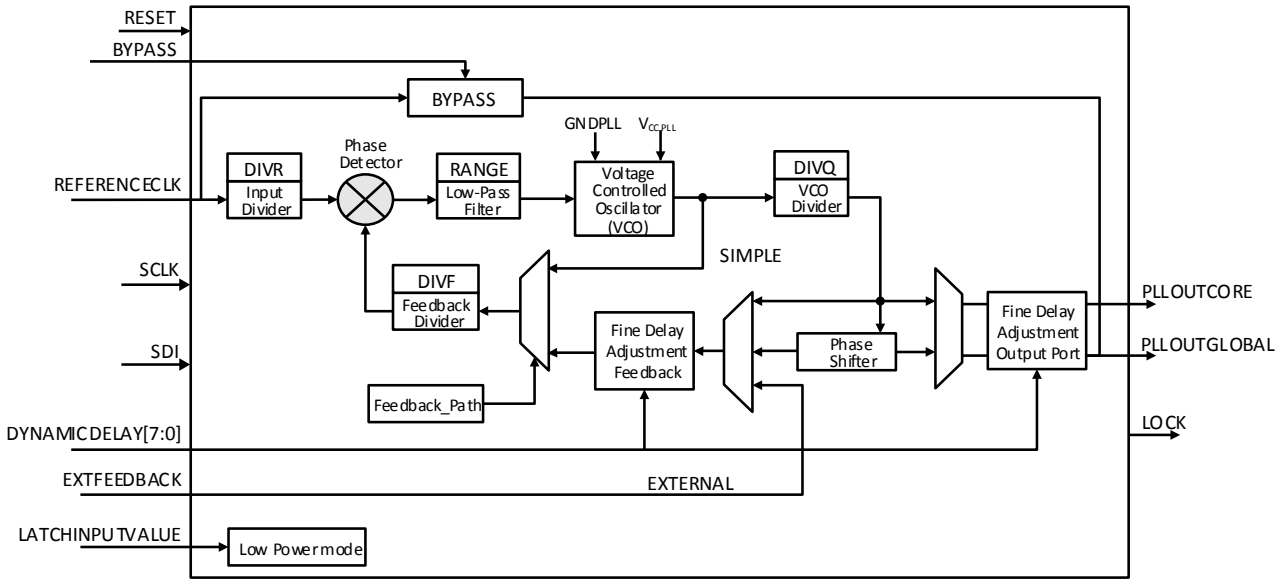

Figure 3.3. PLL Diagram

Table 3.3 provides signal descriptions of the PLL block.

Note: For iCE40 UltraPlus, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock and falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses failing-edge clocks on both Read and Write.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 3.4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

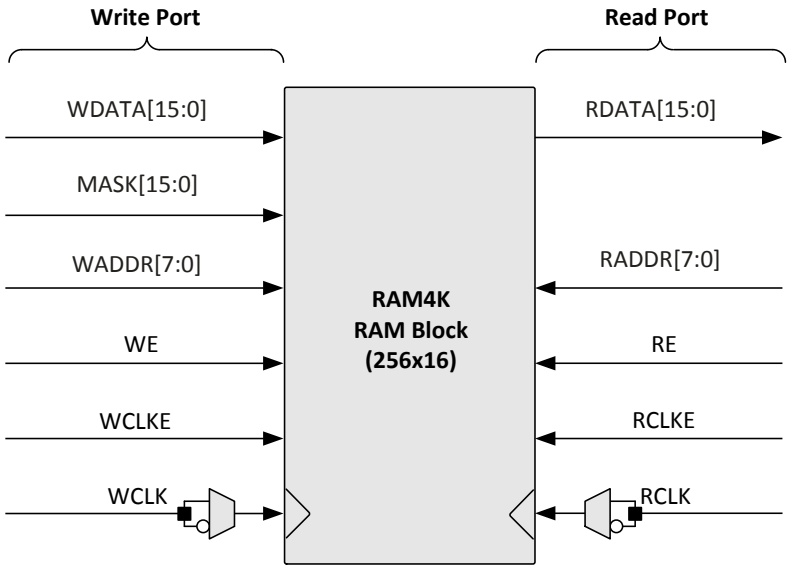

Figure 3.4. sysMEM Memory Primitives

Table 3.5 lists the EBR signals.

Table 3.5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 – Write bit 1 – Do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.

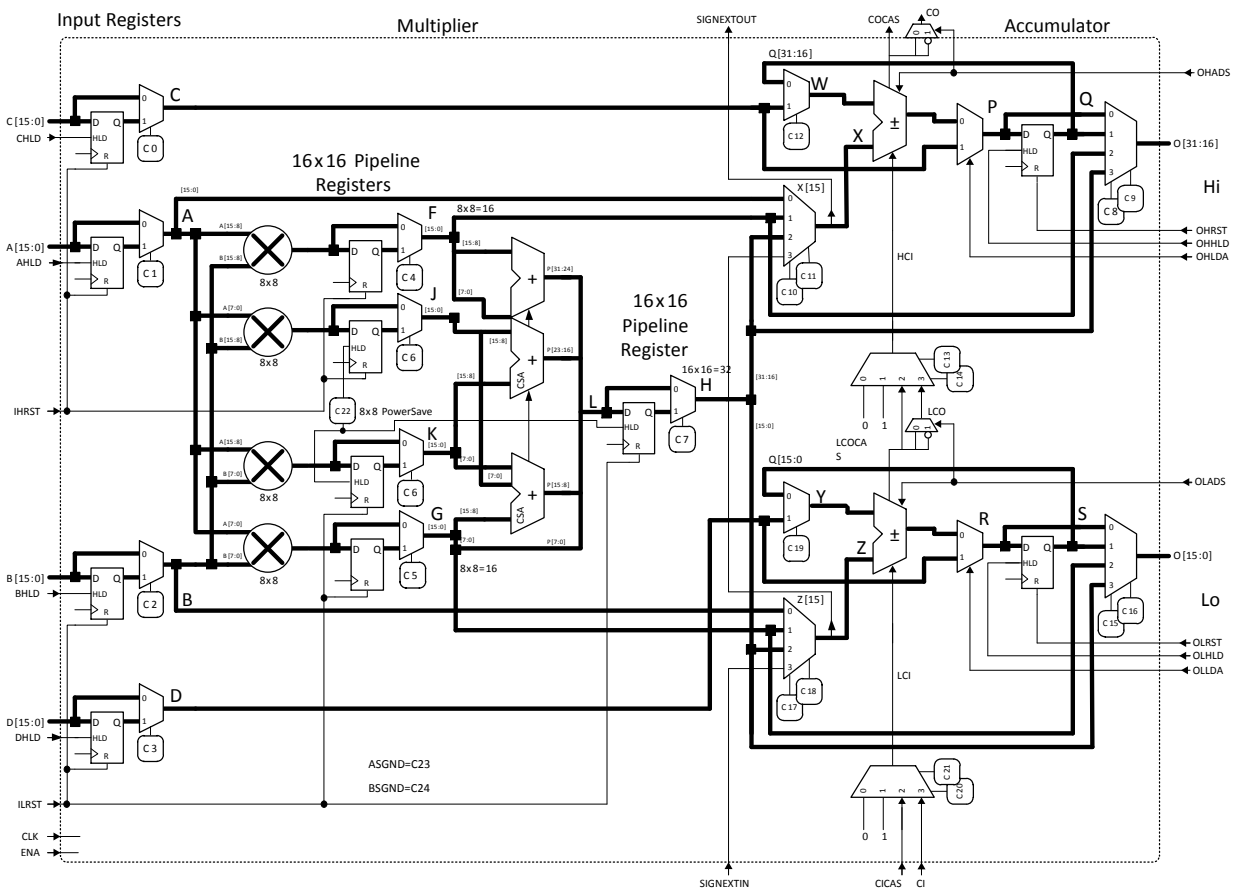

Figure 3.6. sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate)

Table 3.7. Output Block Port Description

Signal	Primitive Port Name	Width	Input/ Output	Function	Default
CLK	CLK	1	Input	Clock Input. Applies to all clocked elements in the sysDSP block	—
ENA	CE	1	Input	Clock Enable Input. Applies to all clocked elements in the sysDSP block. 0 – Not enabled 1 – Enabled	0 – Enabled
A[15:0]	A[15:0]	16	Input	Input to the A Register. Feeds the Multiplier or is a direct input to the Adder Accumulator	16'b0
B[15:0]	B[15:0]	16	Input	Input to the B Register. Feeds the Multiplier or is a direct input to the Adder Accumulator	16'b0
C[15:0]	C[15:0]	16	Input	Input to the C Register. It is a direct input to the Adder Accumulator	16'b0
D[15:0]	D[15:0]	16	Input	Input to the D Register. It is a direct input to the Adder Accumulator	16'b0
AHLD	AHOLD	1	Input	A Register Hold. 0 – Update 1 – Hold	0 – Update

Table 3.7. Output Block Port Description *(Continued)*

Signal	Primitive Port Name	Width	Input/ Output	Function	Default
OLLDA	OLOADBOT	1	Input	Low-order (lower half) Accumulator Register Accumulate/Load control. 0 – Accumulate, register is loaded with Adder/Subtracter results 1 – Load, register is loaded with Input C or C Register	0 – Accumulate
OLADS	ADDSUBBOT	1	Input	Low-order (lower half) Accumulator Add or Subtract select. 0 – Add 1 – Subtract	0 – Add
CICAS	ACCUMCI	1	Input	Cascade Carry/Borrow input from previous sysDSP block	—
CI	CI	1	Input	Carry/Borrow input from lower logic tile	—
COCAS	ACCUMCO	1	Output	Cascade Carry/Borrow output to next sysDSP block	—
CO	CO	1	Output	Carry/Borrow output to higher logic tile	—
SIGNEXTIN	SIGNEXTIN	1	Input	Sign extension input from previous sysDSP block	—
SIGNEXTOUT	SIGNEXTOUT	1	Output	Sing extension output to next sysDSP block	—

The iCE40 UltraPlus sysDSP can support the following functions:

- 8-bit x 8-bit Multiplier
- 16-bit x 16-bit Multiplier
- 16-bit Adder/Subtracter
- 32-bit Adder/Subtracter
- 16-bit Accumulator
- 32-bit Accumulator
- 8-bit x 8-bit Multiply-Accumulate
- 16-bit x 16-bit Multiply-Accumulate

Figure 3.7 on the next page shows the path for an 8-bit x 8-bit Multiplier using the upper half of sysDSP block.

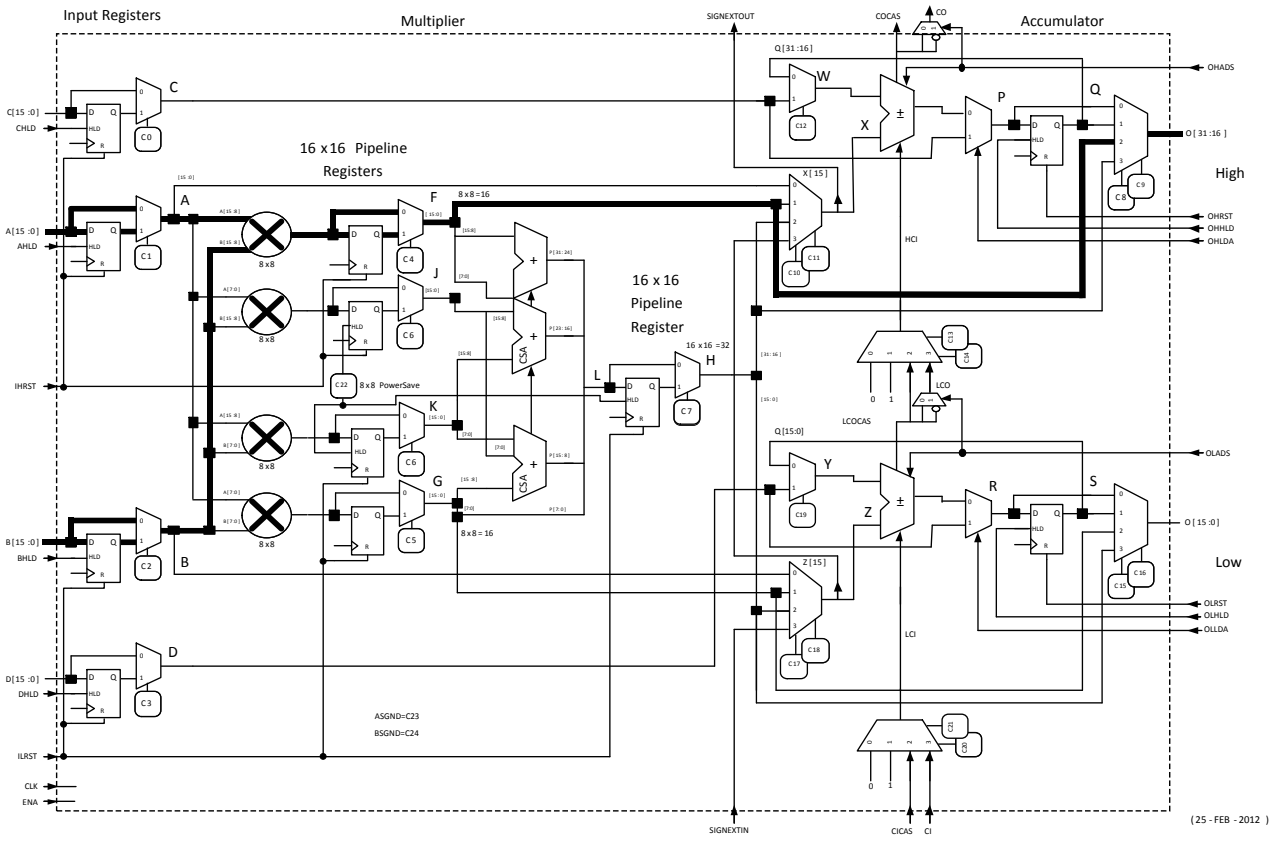

Figure 3.7. sysDSP 8-bit x 8-bit Multiplier

Figure 3.8 shows the path for an 16-bit x 16-bit Multiplier using the upper half of sysDSP block.

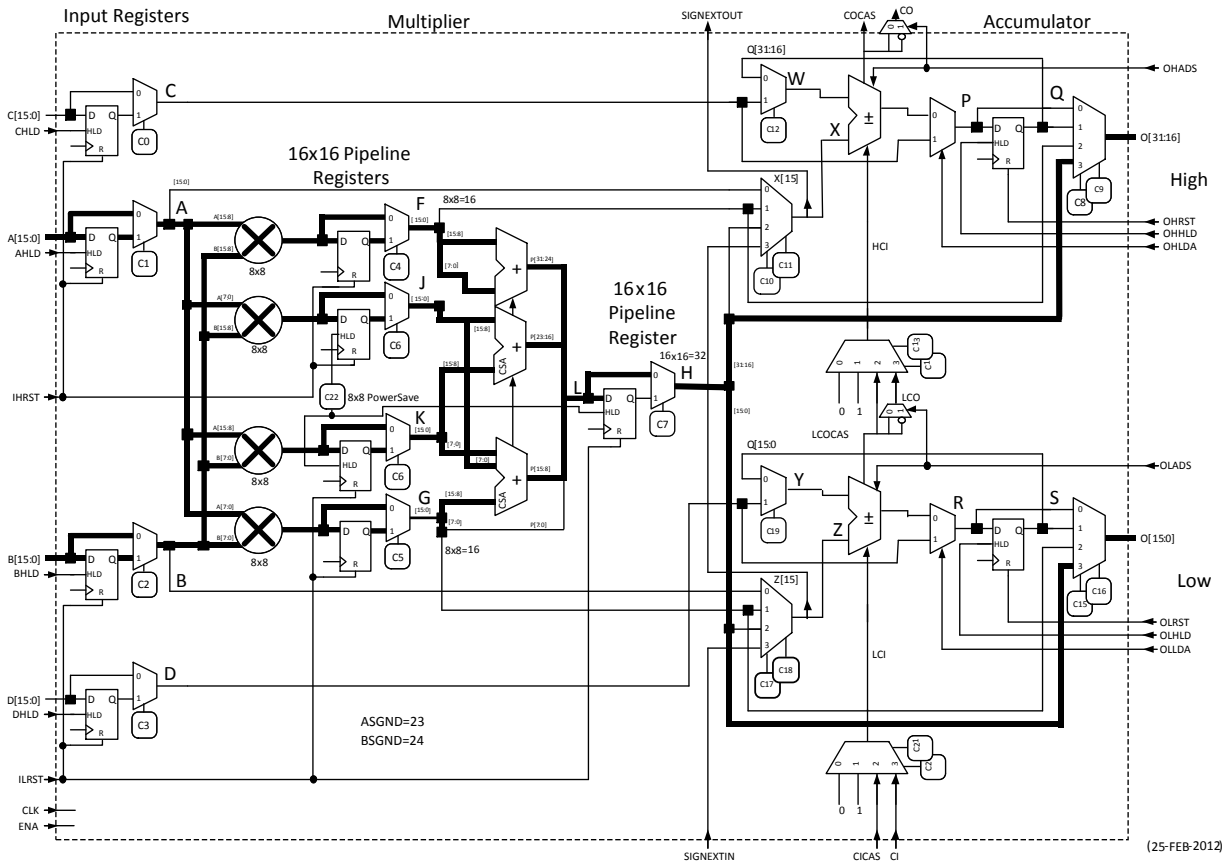

Figure 3.8. DSP 16-bit x 16-bit Multiplier

3.1.8. sysIO Buffer Banks

iCE40 UltraPlus devices have up to three I/O banks with independent V_{CCIO} rails. The configuration SPI interface signals are powered by SPI_V_{CCIO1}. Please refer to the Pin Information Summary table.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

3.1.11. User I²C IP

The iCE40 UltraPlus devices have two I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The pins for the I²C interface are not pre-assigned. User can use any General Purpose I/O pins.

In each of the two cores, there are options to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I²C components.

When the IP core is configured as master, it will be able to control other devices on the I²C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 400 kHz data transfer speed
- General Call support
- Optionally delaying input or output data, or both
- Optional filter on SCL input

For further information on the User I²C, refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

3.1.12. User SPI IP

The iCE40 UltraPlus devices have two SPI IP cores. The pins for the SPI interface are not pre-assigned. User can use any General Purpose I/O pins. Both SPI IP cores can be configured as a SPI master or as a slave. When the SPI IP core is configured as a master, it controls the other SPI enabled devices connected to the SPI Bus. When SPI IP core is configured as a slave, the device will be able to interface to an external SPI master.

The SPI IP core supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer

For further information on the User SPI, refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

3.1.13. RGB High Current Drive I/O Pins

The iCE40 UltraPlus family devices offer multiple high current LED drive outputs in each device in the family to allow the iCE40 UltraPlus product to drive LED signals directly on mobile applications.

There are three outputs on each device that can sink up to 24 mA current. These outputs are open-drain outputs, and provides sinking current to an LED connecting to the positive supply. These three outputs are designed to drive the RBG LEDs, such as the service LED found in a lot of mobile devices. This RGB drive current is user programmable from 4 mA to 24 mA, in increments of 4 mA. This output functions as General Purpose I/O with open-drain when the high current drive is not needed.

3.1.14. RGB PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be used in the user design. This PWM IP provides the flexibility for user to dynamically change the modulation width of each of the RGB LED driver, which changes the color. Also, the user can dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the PWM IP, refer to TN1288, iCE40 LED Driver Usage Guide.

4.15. Internal Oscillators (HFOSC, LFOSC)

Table 4.11. Internal Oscillators (HFOSC, LFOSC)

Parameter		Parameter Description	Spec/Recommended			Unit
Symbol	Conditions		Min	Typ	Max	
f_{CLKHF}	Commercial Temp	HFOSC clock frequency (t_J = 0 °C–85 °C)	-10%	48	10%	MHz
	Industrial Temp	HFOSC clock frequency (t_J = –40 °C–100 °C)	-20%	48	20%	MHz
f_{CLKLF}	—	LFOSC CLKK clock frequency	-10%	10	10%	kHz
DCH_{CLKHF}	Commercial Temp	HFOSC Duty Cycle (t_J = 0 °C–85 °C)	45	50	55	%
	Industrial Temp	HFOSC Duty Cycle (t_J = –40 °C–100 °C)	40	50	60	%
DCH_{CLKLF}	—	LFOSC Duty Cycle (Clock High Period)	45	50	55	%
Tsync_on	—	Oscillator output synchronizer delay	—	—	5	Cycles
Tsync_off	—	Oscillator output disable delay	—	—	5	Cycles

Note: Glitchless enabling and disabling OSC clock outputs.

4.16. sysI/O Recommended Operating Conditions

Table 4.12. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min	Typ	Max
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89

4.17. sysI/O Single-Ended DC Electrical Characteristics

Table 4.13. sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}* (mA)	I_{OH} Max (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO}+0.2 V	0.4	V_{CCIO} – 0.4	8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO}+0.2 V	0.4	V_{CCIO} – 0.4	6	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	V_{CCIO}+0.2 V	0.4	V_{CCIO} – 0.4	4	–4
					0.2	V_{CCIO} – 0.2	0.1	–0.1

4.18. Differential Comparator Electrical Characteristics

Table 4.14. Differential Comparator Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{REF}	Reference Voltage to compare, on V_{INM}	V_{CCIO} = 2.5 V	0.25	V_{CCIO} - 0.25 V	V
V_{DIFFIN_H}	Differential input HIGH (V_{INP} - V_{INM})	V_{CCIO} = 2.5 V	250	—	mV
V_{DIFFIN_L}	Differential input LOW (V_{INP} - V_{INM})	V_{CCIO} = 2.5 V	—	–250	mV
I_{IN}	Input Current, V_{INP} and V_{INM}	V_{CCIO} = 2.5 V	–10	10	µA

4.19. Typical Building Block Function Performance

4.19.1. Pin-to-Pin Performance (LVCMOS25)

Table 4.15. Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Unit
Basic Functions		
16-Bit Decoder	16.5	ns
4:1 Mux	18.0	ns
16:1 Mux	19.5	ns

Notes:

1. The above timing numbers are generated using the Lattice Design Software tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a V_{CC} of 1.14 V at Junction Temperature 85 °C.

4.19.2. Register-to-Register Performance

Table 4.16. Register-to-Register Performance

Function	Timing	Unit
Basic Functions		
16:1 Mux	110	MHz
16-Bit Adder	100	MHz
16-Bit Counter	100	MHz
64-Bit Counter	40	MHz
Embedded Memory Functions		
256 x 16 Pseudo-Dual Port RAM	150	MHz

Notes:

1. The above timing numbers are generated using the Lattice Design Software tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Under worst case operating conditions.

4.20. sysDSP Timing

Over recommended operating conditions.

Table 4.17. sysDSP Timing

Parameter	Description	Min	Max	Unit
$f_{MAX8x8SMULT}$	Max frequency signed MULT8x8 bypassing pipeline register	50	—	MHz
$f_{MAX16x16SMULT}$	Max frequency signed MULT16x16 bypassing pipeline register	50	—	MHz

4.21. SPRAM Timing

Over recommended operating conditions.

Table 4.18. Single Port RAM Timing

Parameter	Description	Min	Max	Unit
$f_{MAXSRAM}$	Max frequency SPRAM (4/8/16-bit Read and Write)	70	—	MHz

4.22. Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

4.26. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 4.22. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Unit
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)	—	10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)	—	16	275	MHz
f_{VCO}	PLL VCO Frequency	—	533	1066	MHz
f_{PFD}[3]	Phase Detector Input Frequency	—	10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	40	60	%
t_{PH}	Output Phase Accuracy	—	—	±12	deg
t_{OPJIT}[1, 5, 6]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	450	ps p-p
		f_{OUT} < 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-Cycle Jitter	f_{OUT} >= 100 MHz	—	750	ps p-p
		f_{OUT} < 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} >= 25 MHz	—	275	ps p-p
		f_{PFD} < 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time	—	—	50	µs
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	f_{PFD} ≥ 20 MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable	—	—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width	—	100	—	ns
t_{RST}	RESET Pulse Width	—	10	—	ns
t_{RSTREC}	RESET Recovery Time	—	10	—	µs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width	—	100	—	VCO Cycles

Notes:

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

4.27. SPI Master or NVCM Configuration Time

Table 4.23. SPI Master or NVCM Configuration Time

Symbol	Parameter	Conditions	Max	Unit
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	140	ms
		All devices – Medium frequency	50	ms
		All devices – High frequency	26	ms

Notes:

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

4.28. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 4.24. sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
All Configuration Mode						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 UltraPlus device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{SU}	CCLK setup time		6.16	—	—	ns
t_{HD}	CCLK hold time		1	—	—	ns

Notes:

1. Supported with 1.2 V V_{CC} and at 25 °C.
2. Extended range f_{MAX} Write operations support up to 53 MHz with 1.2 V V_{CC} and at 25 °C.
3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.

5. Pinout Information

5.1. Signal Descriptions

5.1.1. Power Supply Pins

Signal Name	Function	I/O	Description
V_{CC}	Power	—	Core Power Supply
V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	Power	—	Power for I/Os in Bank 0, 1, and 2.
V_{PP_2V5}	Power	—	Power for NVCM programming and operations.
V_{CCPLL}	Power	—	Power for PLL.
GND	GROUND	—	Ground
GND_LED	GROUND	—	Ground for LED drivers. Should connect to GND on board.

5.1.2. Configuration Pins

Signal Name		Function	I/O	Description
General I/O	Shared Function			
CRESET_B	—	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kΩ pull-up to SPI_V_{CCIO1}.
IOB_xxx	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO1}.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function. In 30-pin WLCSP, this pin connects to IOB_12a, which also is shared as global signal G4 in user mode.

5.1.3. Configuration SPI Pins

Signal Name		Function	I/O	Description
General I/O	Shared Function			
IOB_34a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
IOB_32a	SPI_SO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

IOB_33b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
IOB_35b	SPI_SS_B	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

5.1.4. Global Pins

Signal Name		Function	I/O	Description
General I/O	Shared Function			
IOT_46b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G0 pin drives the GBUF0 global buffer.
IOT_45a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G1 pin drives the GBUF1 global buffer.
IOB_25b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G3 pin drives the GBUF3 global buffer.
IOB_12a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G4 pin drives the GBUF4 global buffer.
IOB_11b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G5 pin drives the GBUF5 global buffer.
IOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G6 pin drives the GBUF6 global buffer.

5.1.5. General I/O, LED Pins

Signal Name		Function	I/O	Description
Gerenal I/O	Shared Function			
RGB0	—	General I/O	Open-Drain I/O	In user mode, when RGB function is not used, this pin can be connected to any user logic and used as open-drain I/O. This pin is located in Bank 0.
		LED	Open-Drain Output	In user mode, when using RGB function, this pin can be programmed as open drain 24 mA output to drive external LED.

RGB1	—	General I/O	Open-Drain I/O	In user mode, when RGB function is not used, this pin can be connected to any user logic and used as open-drain I/O. This pin is located in Bank 0.
		LED	Open-Drain Output	In user mode, when using RGB function, this pin can be programmed as open drain 24 mA output to drive external LED.
RGB2	—	General I/O	Open-Drain I/O	In user mode, when RGB function is not used, this pin can be connected to any user logic and used as open-drain I/O. This pin is located in Bank 0.
		LED	Open-Drain Output	In user mode, when using RGB function, this pin can be programmed as open drain 24 mA output to drive external LED.
PIOT_xx	—	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location). These pins are located in Bank 0.
PIOB_xx	—	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location). Pins with xx <= 9 are located in Bank 2, pins with xx> are located in Bank 1.

5.2. Pin Information Summary

Pin Type		iCE40UP3K	iCE40UP5K	
		UWG30	UWG30	SG48
General Purpose I/O Per Bank	Bank 0	7	7	17
	Bank 1	10	10	14
	Bank 2	4	4	8
Total General Purpose I/Os		21	21	39
V_{CC}		1	1	2
V_{CCIO}	Bank 0	1	1	1
	Bank 1	1	1	1
	Bank 2	1	1	1
V_{CCPLL}		1	1	1
V_{PP_2V5}		1	1	1
Dedicated Config Pins		1	1	2
GND		2	2	0[1]
Total Balls		30	30	48

Note:

1. 48-pin QFN package (SG48) requires the package paddle to be connected to GND.

		DC and Switching Characteristics	— Added the following figures: • Figure 4.1. Power Up Sequence with SPE_VCCIO1 and VPP_2V5 Not Connected Together. • Figure 4.2. Power Up Sequence with All Supplies Connected Together to 1.8 V. — Updated note in Table 4.5. DC Electrical Characteristics. — Added note in Table 4.6. Supply Current. — Revised User SPI Specifications 1, 2 section. • Removed symbols. • Added notes. — Revised Table 4.11. Internal Oscillators (HFOSC, LFOSC). — Removed note in Table 4.13. sysI/O Single-Ended DC Electrical Characteristics. — Changed to Lattice Design Software tool in Table 4.15. Pin-to-Pin Performance (LVCMOS25). — Changed to Lattice Design Software tool and revised note in Table 4.16. Register-to-Register Performance. — Added sysDSP Timing section. — Added SPRAM Timing section. — Removed LVCMOS12 and added timing values in Table 4.19. Maximum IO Buffer Performance. — Removed LVCMOS12 and added timing values in Table 4.20. iCE40 UltraPlus Family Timing Adders. — Revised max values in Table 4.23. SPI Master or NVCM Configuration Time. — Removed TBD conditions in Table 4.24. sysCONFIG Port Timing Specifications. Revised t_{HD} parameter. — Revised Table 4.25. High Current RGB LED and IR LED Drive.
		Pinout Information	— General update to Signal Descriptions section. — Updated the iCE40UP Part Number Description section. Added FGW49 package. — Added OPNs.
		Supplemental Information	Added reference to TN1314, iCE40 SPRAM Usage Guide.
September 2015	1.1	Architecture	Updated Architecture section. Replaced iCE5UP with iCE40UP.
		Pinout Information	Updated Pin Information Summary section. — Replaced iCE5UP with iCE40UP. — Replaced SWG30 with UWG30.
		Ordering Information	Updated iCE40UP Part Number Description section. — Replaced iCE5UP with iCE40UP. — Replaced SWG30 with UWG30.
			Updated Ordering Part Numbers section. Replaced the table of part
		Further Information	Removed reference to Schematic Symbols.
August 2015	1.0	All	Initial release.