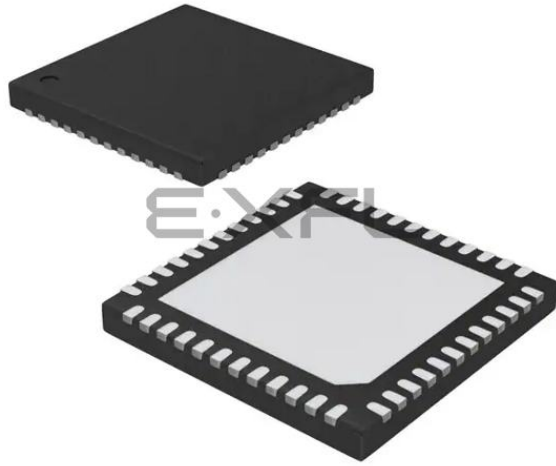




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	660
Number of Logic Elements/Cells	5280
Total RAM Bits	1171456
Number of I/O	39
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40up5k-sg48itr50

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DFF	D-style Flip-Flop
DSP	Digital Signal Processor
EBR	Embedded Block RAM
HFOSC	High Frequency Oscillator
I ² C	Inter-Integrated Circuit
LFOSC	Low Frequency Oscillator
LUT	Look Up Table
LVC MOS	Low-Voltage Complementary Metal Oxide Semiconductor
NVCM	Non Volatile Configuration Memory
PCLK	Primary Clock
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PLB	Programmable Logic Blocks
PLL	Phase Locked Loops
SoC	System on a Chip
SPI	Serial Peripheral Interface
SPR	Single Port RAM
WLCSP	Wafer Level Chip Scale Packaging

1. General Description

iCE40 UltraPlus family from Lattice Semiconductor is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. iCE40 UltraPlus is compatible with Lattice's iCE40 Ultra family devices, containing all the functions iCE40 Ultra family has except the high current IR LED driver. In addition, the iCE40 UltraPlus features an additional 1 Mb SRAM, additional DSP blocks, with additional LUTs, all which can be used to support an always-on Voice Recognition function in the mobile devices, without the need to keep the higher power consuming voice codec on all the time.

The iCE40 UltraPlus family includes integrated SPI and I²C blocks to interface with virtually all mobile sensors and application processors. In addition, the iCE40 UltraPlus family also features two I/O pins that can support the interface to I3C devices. There are two on-chip oscillators, 10 kHz and 48 MHz, the LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The iCE40 UltraPlus family also features DSP functional block to off-load Application Processor to pre-process information sent from the mobile device, such as voice data. The RGB PWM IP, with the three 24 mA constant current RGB outputs on the iCE40 UltraPlus provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The iCE40 UltraPlus family of devices are targeting for mobile applications to perform all the functions in iCE40 Ultra devices, such as Service LED, GPIO Expander, SDIO Level Shift, and other custom functions. In addition, the iCE40 UltraPlus family devices are also targeting for Voice Recognition application.

The iCE40 UltraPlus family features two device densities, 2800 to 5280 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I²C interface ports or general purpose I/O's. Two of the iCE40 UltraPlus I/Os can be used to interface to higher performance I3C. It also has up to 120 kb of Block RAMs, plus 1024 kb of Single Port SRAMs to work with user logic.

1.1. Features

- Flexible Logic Architecture
 - Two devices with 2800 to 5280 LUTs
 - Offered in WLCS and QFN packages
- Ultra-low Power Devices
 - Advanced 40 nm low power process
 - As low as 100 μ A standby current typical
- Embedded Memory
 - Up to 1024 kb Single Port SRAM
 - Up to 120 kb sysMEM™ Embedded Block RAM
- Two Hardened I²C Interfaces
 - Two I/O pins to support I3C interface
- Two Hardened SPI Interfaces
- Two On-Chip Oscillators
 - Low Frequency Oscillator – 10 kHz
 - High Frequency Oscillator – 48 MHz
- 24 mA Current Drive RGB LED Outputs
 - Three drive outputs in each device
 - User selectable sink current up to 24 mA
- On-chip DSP
 - Signed and unsigned 8-bit or 16-bit functions
 - Functions include Multiplier, Accumulator, and Multiply-Accumulate (MAC)
- Flexible On-Chip Clocking
 - Eight low skew global signal resource, six can be directly driven from external pins
 - One PLL with dynamic interface per device
- Flexible Device Configuration
 - SRAM is configured through:
 - Standard SPI Interface
 - Internal Nonvolatile Configuration Memory (NVCM)
- Ultra-Small Form Factor
 - As small as 2.15 mm × 2.55 mm
- Applications
 - Always-On Voice Recognition Application
 - Smartphones
 - Tablets and Consumer Handheld Devices
 - Handheld Commercial and Industrial Devices
 - Multi Sensor Management Applications
 - Sensor Pre-processing and Sensor Fusion
 - Always-On Sensor Applications
 - USB 3.1 Type C Cable Detect / Power Delivery Applications

2. Product Family

Table 2.1 lists device information and packages of the iCE40 UltraPlus family.

Table 2.1. iCE40 UltraPlus Family Selection Guide

Part Number	iCE40UP3K	iCE40UP5K
Logic Cells (LUT + Flip-Flop)	2800	5280
EBR Memory Blocks	20	30
EBR Memory Bits (Kbits)	80	120
SPRAM Memory Blocks	4	4
SPRAM Memory Bits (Kbits)	1024	1024
NVCM	Yes	Yes
PLL	1	1
DSP Blocks (MULT16 with 32-bit Accumulator)	4	8
Hardened I ² C, SPI	2, 2	2, 2
HF Oscillator (48 MHz)	1	1
LF Oscillator (10 KHz)	1	1
24 mA LED Sink	3	3
PWM IP Block	Yes	Yes
Packages, ball pitch, dimension	Total User I/O Count	
30-ball WLCSP, 0.4 mm, 2.15 mm x 2.55 mm	21	21
48-ball QFN, 0.5 mm, 7.0 mm x 7.0 mm	-	39

2.1. Overview

The iCE40 UltraPlus family of ultra-low power FPGAs has three devices with densities ranging from 2800 to 5280 Look-Up Tables (LUTs) fabricated in a 40 nm Low Power CMOS process. In addition to LUT-based, low-cost programmable logic, these devices also feature Embedded Block RAM (EBR), Single Port RAM (SPRAM), on-chip Oscillators (LFOSC, HFOSC), two hardened I²C Controllers, two hardened SPI Controllers, PWM IP, three 24 mA RGB LED open-drain drivers, I³C interface pins, and DSP blocks. These features allow the devices to be used in low-cost, high-volume consumer and mobile applications.

The iCE40 UltraPlus FPGAs are available in very small form factor packages, as small as 2.15 mm x 2.55 mm. The small form factor allows the device to easily fit into a lot of mobile applications, where space can be limited. Table 2.1 lists the LUT densities, package and I/O pin count.

The iCE40 UltraPlus devices offer I/O features such as pull-up resistors. Pull-up features are controllable on a “per pin” basis. In addition, the iCE40 UltraPlus devices offer two I/Os with dynamic control on the pull-up resistors to support I³C interface.

The RGB PWM IP in the iCE40 UltraPlus devices provides controls for driving the 24 mA LED Sink driver, including color controls, LED ON/OFF time, and breathe rate.

The iCE40 UltraPlus devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash, or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 UltraPlus family of devices. Popular logic synthesis tools provide synthesis library support for iCE40 UltraPlus. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 UltraPlus device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 UltraPlus FPGA family. Lattice also can provide fully verified bitstream for some of the widely used target functions in mobile device applications, such as ultra-low power sensor management, gesture recognition, IR remote, barcode emulator functions. Users can use these functions as offered by

Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, contact your local Lattice representative.

3. Architecture

3.1. Architecture Overview

The iCE40 UltraPlus family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I²C controllers, two user configurable SPI controllers, blocks of sysMEM™ Embedded Block RAM (EBR) and Single Port RAM (SPRAM) surrounded by Programmable I/O (PIO). Figure 3.1 shows the block diagram of the iCE40UP5K device.

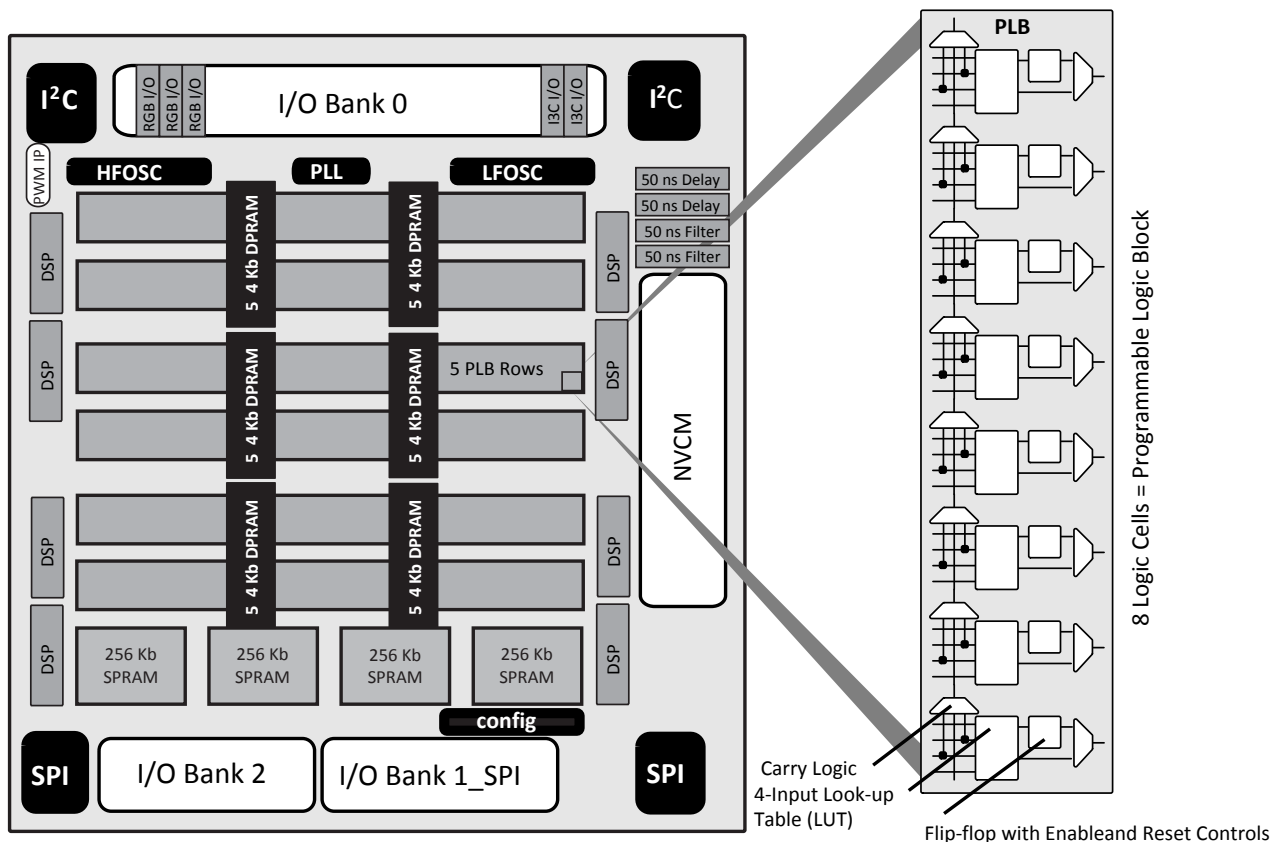


Figure 3.1. iCE40UP5K Device, Top View

The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 UltraPlus family, there are three sysIO banks, one on top and two at the bottom. User can connect some VCCIOs together, if all the I/Os are using the same voltage standard. See the [Power-up Supply Sequence](#) section. The sysMEM EBRs are large 4 kb, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

In addition to the EBR, the iCE40 UltraPlus devices also feature four 256 kb SPRAM blocks that can be cascaded to create up to 1 Mb block. It is useful for temporary storage of large quantities of information.

Table 3.3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLLOUT output. 0 – PLL generated signal 1 – REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

3.1.5. sysMEM Embedded Block RAM Memory

Larger iCE40 UltraPlus device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as listed in [Table 3.4](#).

Table 3.4. sysMEM Block Configurations

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4 k)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4 k)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4 k)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4 k)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

Note: For iCE40 UltraPlus, the primitive name without “Nxx” uses rising-edge Read and Write clocks. “NR” uses rising-edge Write clock and falling-edge Read clock. “NW” uses falling-edge Write clock and rising-edge Read clock. “NRNW” uses falling-edge clocks on both Read and Write.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 3.4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

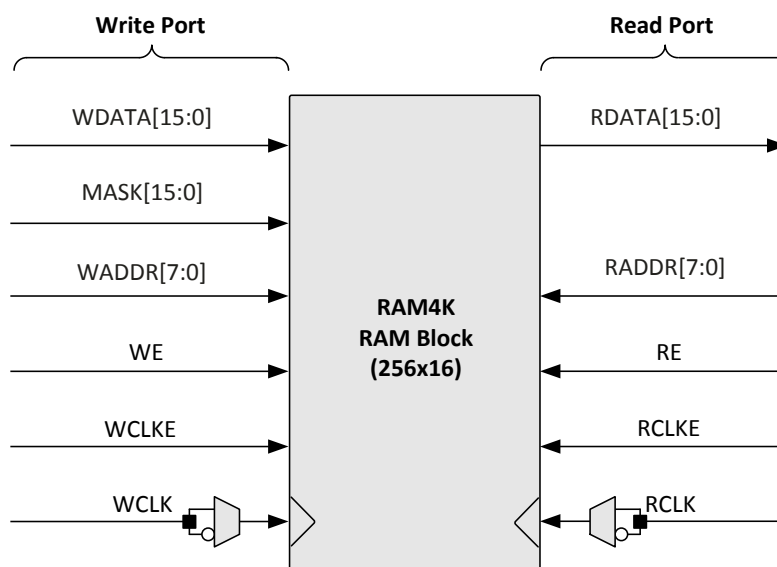


Figure 3.4. sysMEM Memory Primitives

Table 3.5 lists the EBR signals.

Table 3.5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 – Write bit 1 – Do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.

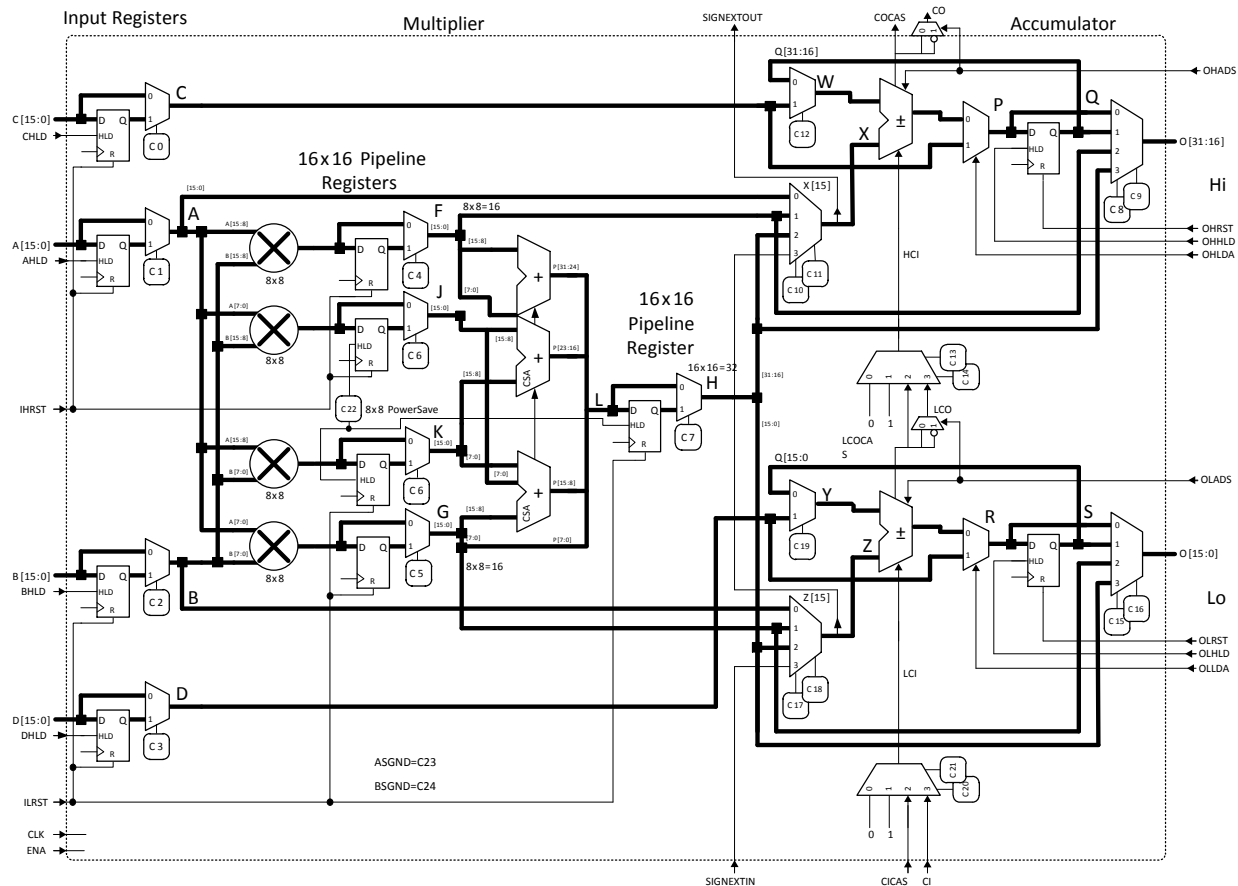


Figure 3.6. sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate)

Table 3.7. Output Block Port Description

Signal	Primitive Port Name	Width	Input/Output	Function	Default
CLK	CLK	1	Input	Clock Input. Applies to all clocked elements in the sysDSP block	—
ENA	CE	1	Input	Clock Enable Input. Applies to all clocked elements in the sysDSP block. 0 – Not enabled 1 – Enabled	0 – Enabled
A[15:0]	A[15:0]	16	Input	Input to the A Register. Feeds the Multiplier or is a direct input to the Adder Accumulator	16'b0
B[15:0]	B[15:0]	16	Input	Input to the B Register. Feeds the Multiplier or is a direct input to the Adder Accumulator	16'b0
C[15:0]	C[15:0]	16	Input	Input to the C Register. It is a direct input to the Adder Accumulator	16'b0
D[15:0]	D[15:0]	16	Input	Input to the D Register. It is a direct input to the Adder Accumulator	16'b0
AHLD	AHOLD	1	Input	A Register Hold. 0 – Update 1 – Hold	0 – Update

Table 3.7. Output Block Port Description (Continued)

Signal	Primitive Port Name	Width	Input/Output	Function	Default
BHLD	BHOLD	1	Input	B Register Hold. 0 – Update 1 – Hold	0 – Update
CHLD	CHOLD	1	Input	C Register Hold. 0 – Update 1 – Hold	0 – Update
DHLD	DHOLD	1	Input	D Register Hold. 0 – Update 1 – Hold	0 – Update
IHRST	IRSTTOP	1	Input	Reset input to A and C input registers, and the pipeline registers in the upper half of the Multiplier Section. 0 – No reset 1 – Reset	0 – No reset
ILRST	IRSTBOT	1	Input	Reset input to B and D input registers, and the pipeline registers in the lower half of the Multiplier Section. It also resets the Multiplier result pipeline register. 0 – No reset 1 – Reset	0 – No reset
O[31:0]	O[31:0]	32	Output	Output of the sysDSP block. This output can be: - O[31:0] – 32-bit result of 16x16 Multiplier or MAC - O[31:16] – 16-bit result of 8x8 upper half Multiplier or MAC - O[15:0] – 16-bit result of 8x8 lower half Multiplier or MAC	—
OHHLD	OHOLDTOP	1	Input	High-order (upper half) Accumulator Register Hold. 0 – Update 1 – Hold	0 – Update
OHRST	ORSTTOP	1	Input	Reset input to high-order (upper half) bits of the Accumulator Register. 0 – No reset 1 – Reset	0 – No reset
OHLDA	OLOADTOP	1	Input	High-order (upper half) Accumulator Register Accumulate/Load control. 0 – Accumulate, register is loaded with Adder/Subtractor results 1 – Load, register is loaded with Input C or C Register	0 – Accumulate
OHADS	ADDSUBTOP	1	Input	High-order (upper half) Accumulator Add or Subtract select. 0 – Add 1 – Subtract	0 – Add
OLHLD	OHOLDBOT	1	Input	Low-order (lower half) Accumulator Register Hold. 0 – Update 1 – Hold	0 – Update
OLRST	ORSTBOT	1	Input	Reset input to Low-order (lower half) bits of the Accumulator Register. 0 – No reset 1 – Reset	0 – No reset

3.1.15. Non-Volatile Configuration Memory

All iCE40 UltraPlus devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, refer to TN1248, [iCE40 Programming and Configuration](#).

3.2. iCE40 UltraPlus Programming and Configuration

This section describes the programming and configuration of the iCE40 UltraPlus family.

3.2.1. Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_VCCIO1 power supply.

3.2.2. Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 UltraPlus, refer to TN1248, [iCE40 Programming and Configuration](#).

3.2.3. Power Saving Options

The iCE40 UltraPlus devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. [Table 3.11](#) describes the function of these features.

Table 3.11. iCE40 UltraPlus Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

4. DC and Switching Characteristics

4.1. Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage V_{CC}	-0.5	1.42	V
Output Supply Voltage V_{CCIO}	-0.5	3.60	V
NVCM Supply Voltage V_{PP_2V5}	-0.5	3.60	V
PLL Supply Voltage V_{CCPLL}	-0.5	1.42	V
I/O Tri-state Voltage Applied	-0.5	3.60	V
Dedicated Input Voltage Applied	-0.5	3.60	V
Storage Temperature (Ambient)	-65	150	°C
Junction Temperature (T_J)	-65	125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V _{CC} ¹	Core Supply Voltage		1.14	1.26	V
V _{PP_2V5}	V _{PP_2V5} NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71 ⁴	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V _{CCIO} ^{1, 2, 3}	I/O Driver Supply Voltage	V _{CCIO_0} , SPI_V _{CCIO1} , V _{CCIO_2}	1.71	3.46	V
V _{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t _{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t _{JIND}	Junction Temperature, Industrial Operation		−40	100	°C
t _{PROG}	Junction Temperature NVCM Programming		10.00	30.00	°C

Notes:

1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. See the [Power-up Supply Sequence](#) section. V_{CC} and V_{CCPLL} are recommended to be tied together to the same supply with an RC-based noise filter between them. Refer to TN1252, [iCE40 Hardware Checklist](#).
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration modes subject to the condition that none of the HFOSC/LFOSC and RGB LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

4.3. Power Supply Ramp Rates

Table 4.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies	0.6	10	V/ms

Notes:

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. See the Power-up Supply Sequence section below.

4.4. Power-On Reset

All iCE40 UltraPlus devices have on-chip Power-On-Reset (POR) circuitry to ensure proper initialization of the device. Only three supply rails are monitored by the POR circuitry as follows: (1) VCC, (2) SPI_VCCIO1 and (3) VPP_2V5. All other supply pins have no effect on the power-on reset feature of the device. Note that all supply voltage pins must be connected to power supplies for normal operation (including device configuration).

4.5. Power-up Supply Sequence

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5 V, or higher, before any subsequent power supplies in the sequence are applied.

1. **VCC** and **VCCPLL** should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the VCCPLL. Refer to TN1252, [iCE40 Hardware Checklist](#).
2. **SPI_VCCIO1** should be the next supply, and can be applied any time after the previous supplies (VCC and VCCPLL) have reached as level of 0.5 V or higher.
3. **VPP_2V5** should be the next supply, and can be applied any time after previous supplies (VCC, VCCPLL and SPI_VCCIO1) have reached a level of 0.5 V or higher.
4. **Other Supplies** (VCCIO0 and VCCIO2) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (VCC and VCCPLL) have reached a level of 0.5 V or greater. There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are re-powered up again.

4.6. External Reset

When all power supplies have reached their minimum operating voltage defined in the Minimum Operation Condition Table, it is required to either keep CRESET_B LOW, or toggle CRESET_B from HIGH to LOW, for a duration of $t_{\text{CRESET_B}}$, and release it to go HIGH, to start configuration download from either the internal NVCM or the external Flash memory. Figure 4.1 shows Power-Up sequence when SPI_VCCIO1 and VPP_2V5 are not connected together, and the CRESET_B signal triggers configuration download. shows when SPI_VCCIO1 and VPP_2V5 connected together. All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

4.23. Maximum sysIO Buffer Performance

Table 4.19. Maximum sysIO Buffer Performance

I/O Standard	Max Speed	Unit
Inputs		
LVC MOS33	250	MHz
LVC MOS25	250	MHz
LVC MOS18	250	MHz
Outputs		
LVC MOS33	250	MHz
LVC MOS25	250	MHz
LVC MOS18	155	MHz
LVC MOS12	70	MHz

Note: Measured with a toggling pattern.

4.24. iCE40 UltraPlus Family Timing Adders

Over recommended commercial operating conditions.

Table 4.20. iCE40 UltraPlus Family Timing Adders

Buffer Type	Description	Timing (Typ)	Units
Input Adjusters			
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	0.18	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	0.19	ns
Output Adjusters			
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	-0.12	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	1.32	ns
LVC MOS12	LVC MOS, $V_{CCIO} = 1.2\text{ V}$	5.38	ns

Notes:

1. Timing adders are relative to LVC MOS25 and characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. Commercial timing numbers are shown.

4.28. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 4.24. sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
All Configuration Mode						
t _{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t _{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t _{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 UltraPlus device is clearing its internal configuration memory		1200	—	—	μs
f _{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read ¹	—	15	—	MHz
t _{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t _{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t _{STSU}	CCLK setup time		12	—	—	ns
t _{STH}	CCLK hold time		12	—	—	ns
t _{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI³						
f _{MCLK}	MCLK clock frequency	Low Frequency	7.0	12.0	17.0	MHz
		Medium Frequency ²	21.0	33.0	45.0	MHz
		High Frequency ²	33.0	53.0	71.0	MHz
t _{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	μs
t _{SU}	CCLK setup time		6.16	—	—	ns
t _{HD}	CCLK hold time		1	—	—	ns

Notes:

- Supported with 1.2 V V_{CC} and at 25 °C.
- Extended range f_{MAX} Write operations support up to 53 MHz with 1.2 V V_{CC} and at 25 °C.
- t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.

Supplemental Information

For Further Information

A variety of technical documents for the iCE40 UltraPlus family are available on the Lattice web site.

- TN1248, [iCE40 Programming and Configuration](#)
- TN1274, [iCE40 SPI/I2C Hardened IP Usage Guide](#)
- TN1276, [Advanced iCE40 SPI/I2C Hardened IP Usage Guide](#)
- TN1250, [Memory Usage Guide for iCE40 Devices](#)
- TN1251, [iCE40 sysCLOCK PLL Design and Usage Guide](#)
- TN1252, [iCE40 Hardware Checklist](#)
- TN1288, [iCE40 LED Driver Usage Guide](#)
- TN1295, [DSP Function Usage Guide for iCE40 Devices](#)
- TN1296, [iCE40 Oscillator Usage Guide](#)
- TN1314, [iCE40 SPRAM Usage Guide](#)
- iCE40 UltraPlus Pinout Files
- iCE40 UltraPlus Pin Migration Files
- [Thermal Management](#) document
- [Package Diagrams](#)
- [Lattice design tools](#)

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

		DC and Switching Characteristics	— Added the following figures: • Figure 4.1. Power Up Sequence with SPE_VCCIO1 and VPP_2V5 Not Connected Together. • Figure 4.2. Power Up Sequence with All Supplies Connected Together to 1.8 V. — Updated note in Table 4.5. DC Electrical Characteristics. — Added note in Table 4.6. Supply Current. — Revised User SPI Specifications 1, 2 section. • Removed symbols. • Added notes. — Revised Table 4.11. Internal Oscillators (HFOSC, LFOSC). — Removed note in Table 4.13. sysI/O Single-Ended DC Electrical Characteristics. — Changed to Lattice Design Software tool in Table 4.15. Pin-to-Pin Performance (LVCMOS25). — Changed to Lattice Design Software tool and revised note in Table 4.16. Register-to-Register Performance. — Added sysDSP Timing section. — Added SPRAM Timing section. — Removed LVCMOS12 and added timing values in Table 4.19. Maximum IO Buffer Performance. — Removed LVCMOS12 and added timing values in Table 4.20. iCE40 UltraPlus Family Timing Adders. — Revised max values in Table 4.23. SPI Master or NVCM Configuration Time. — Removed TBD conditions in Table 4.24. sysCONFIG Port Timing Specifications. Revised t_{HD} parameter. — Revised Table 4.25. High Current RGB LED and IR LED Drive.
		Pinout Information	— General update to Signal Descriptions section. — Updated the iCE40UP Part Number Description section. Added FGW49 package. — Added OPNs.
		Supplemental Information	Added reference to TN1314, iCE40 SPRAM Usage Guide .
September 2015	1.1	Architecture	Updated Architecture section. Replaced iCE5UP with iCE40UP.
		Pinout Information	Updated Pin Information Summary section. — Replaced iCE5UP with iCE40UP. — Replaced SWG30 with UWG30.
		Ordering Information	Updated iCE40UP Part Number Description section. — Replaced iCE5UP with iCE40UP. — Replaced SWG30 with UWG30.
		Further Information	Updated Ordering Part Numbers section. Replaced the table of part
August 2015	1.0	All	Initial release.