Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	660
Number of Logic Elements/Cells	5280
Total RAM Bits	1171456
Number of I/O	21
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	30-UFBGA, WLCSP
Supplier Device Package	30-WLCSP (2.54x2.12)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40up5k-uwg30itr

Figures

1. General Description

iCE40 UltraPlus family from Lattice Semiconductor is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. iCE40 UltraPlus is compatible with Lattice's iCE40 Ultra family devices, containing all the functions iCE40 Ultra family has except the high current IR LED driver. In addition, the iCE40 UltraPlus features an additional 1 Mb SRAM, additional DSP blocks, with additional LUTs, all which can be used to support an always-on Voice Recognition function in the mobile devices, without the need to keep the higher power consuming voice codec on all the time.

The iCE40 UltraPlus family includes integrated SPI and I^2C blocks to interface with virtually all mobile sensors and application processors. In addition, the iCE40 UltraPlus family also features two I/O pins that can support the interface to I3C devices. There are two on-chip oscillators, 10 kHz and 48 MHz, the LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The iCE40 UltraPlus family also features DSP functional block to off-load Application Processor to pre-process information sent from the mobile device, such as voice data. The RGB PWM IP, with the three 24 mA constant current RGB outputs on the iCE40 UltraPlus provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The iCE40 UltraPlus family of devices are targeting for mobile applications to perform all the functions in iCE40 Ultra devices, such as Service LED, GPIO Expander, SDIO Level Shift, and other custom functions. In addition, the iCE40 UltraPlus family devices are also targeting for Voice Recognition application.

The iCE40 UltraPlus family features two device densities, 2800 to 5280 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I^2C interface ports or general purpose I/O's. Two of the iCE40 UltraPlus I/Os can be used to interface to higher performance I3C. It also has up to 120 kb of Block RAMs, plus 1024 kb of Single Port SRAMs to work with user logic.

1.1. Features

- Flexible Logic Architecture
  - Two devices with 2800 to 5280 LUTs
  - Offered in WLCS and QFN packages
- Ultra-low Power Devices
  - Advanced 40 nm low power process
  - As low as 100 µA standby current typical
- Embedded Memory
  - Up to 1024 kb Single Port SRAM
  - Up to 120 kb sysMEM™ Embedded Block RAM
- Two Hardened I^2C Interfaces
  - Two I/O pins to support I3C interface
- Two Hardened SPI Interfaces
- Two On-Chip Oscillators
  - Low Frequency Oscillator – 10 kHz
  - High Frequency Oscillator – 48 MHz
- 24 mA Current Drive RGB LED Outputs
  - Three drive outputs in each device
  - User selectable sink current up to 24 mA
- On-chip DSP
  - Signed and unsigned 8-bit or 16-bit functions
  - Functions include Multiplier, Accumulator, and Multiply-Accumulate (MAC)
- Flexible On-Chip Clocking
  - Eight low skew global signal resource, six can be directly driven from external pins
  - One PLL with dynamic interface per device
- Flexible Device Configuration
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- Ultra-Small Form Factor
  - As small as 2.15 mm × 2.55 mm
- Applications
  - Always-On Voice Recognition Application
  - Smartphones
  - Tablets and Consumer Handheld Devices
  - Handheld Commercial and Industrial Devices
  - Multi Sensor Management Applications
  - Sensor Pre-processing and Sensor Fusion
  - Always-On Sensor Applications
  - USB 3.1 Type C Cable Detect / Power Delivery Applications

Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, contact your local Lattice representative.

3. Architecture

3.1. Architecture Overview

The iCE40 UltraPlus family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I^{2}C controllers, two user configurable SPI controllers, blocks of sysMEM™ Embedded Block RAM (EBR) and Single Port RAM (SPRAM) surrounded by Programmable I/O (PIO). Figure 3.1 shows the block diagram of the iCE40UP5K device.
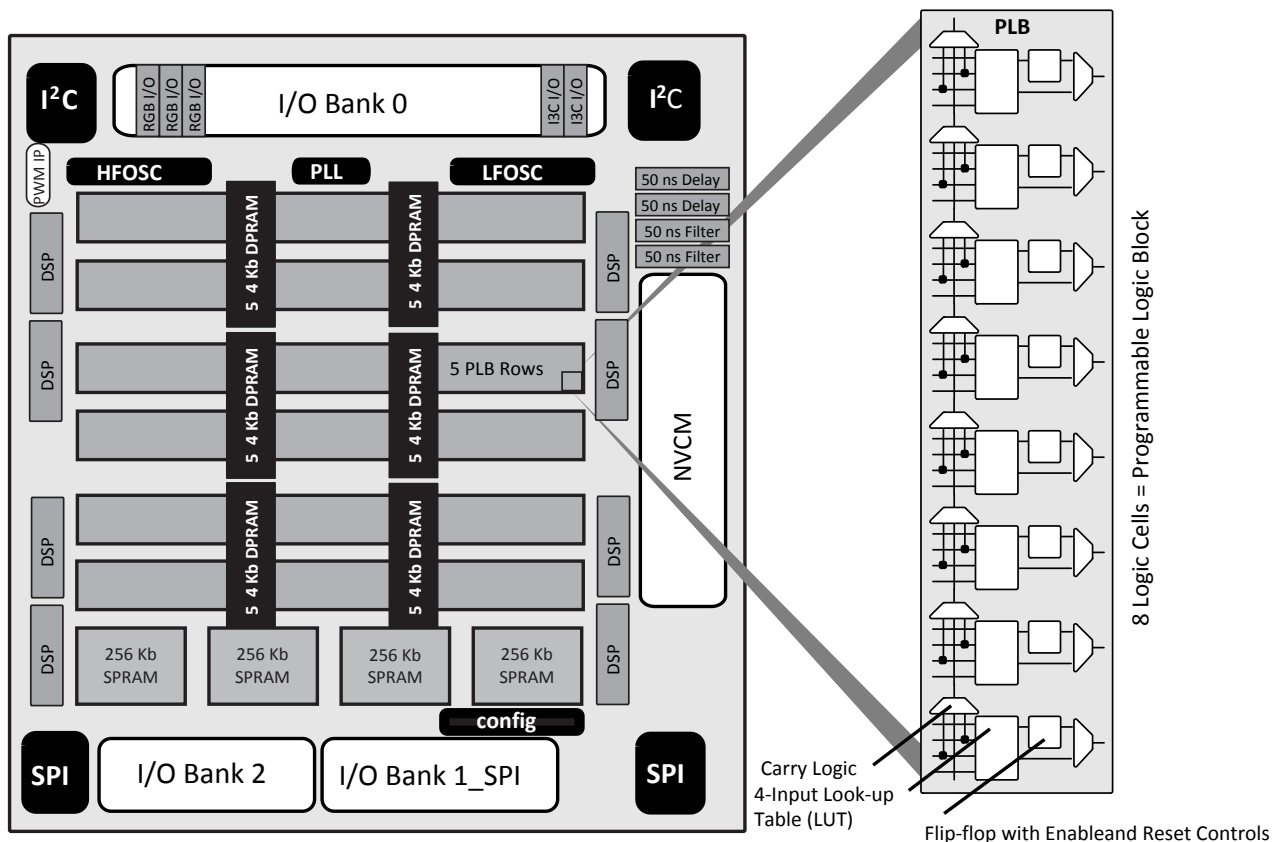
Figure 3.1. iCE40UP5K Device, Top View

The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 UltraPlus family, there are three sysIO banks, one on top and two at the bottom. User can connect some V$_{CCIO}$s together, if all the I/Os are using the same voltage standard. See the Power-up Supply Sequence section. The sysMEM EBRs are large 4 kb, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

In addition to the EBR, the iCE40 UltraPlus devices also feature four 256 kb SPRAM blocks that can be cascaded to create up to 1 Mb block. It is useful for temporary storage of large quantities of information.

3.1.4. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 UltraPlus devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 UltraPlus global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 3.3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 UltraPlus PLL. There are two FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.
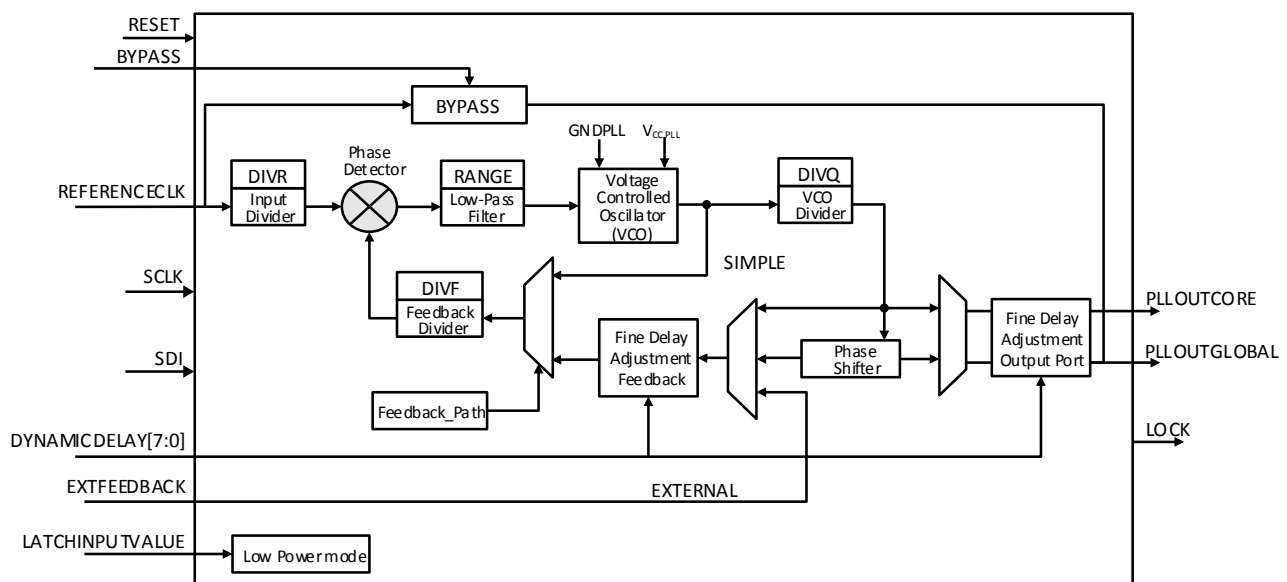

Figure 3.3. PLL Diagram

Table 3.3 provides signal descriptions of the PLL block.

Table 3.3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLLOUT output. 0 – PLL generated signal 1 – REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

3.1.5. sysMEM Embedded Block RAM Memory

Larger iCE40 UltraPlus device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as listed in Table 3.4.

Table 3.4. sysMEM Block Configurations

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4 k)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4 k)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4 k)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4 k)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

Note: For iCE40 UltraPlus, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock and falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses failing-edge clocks on both Read and Write.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 3.4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.
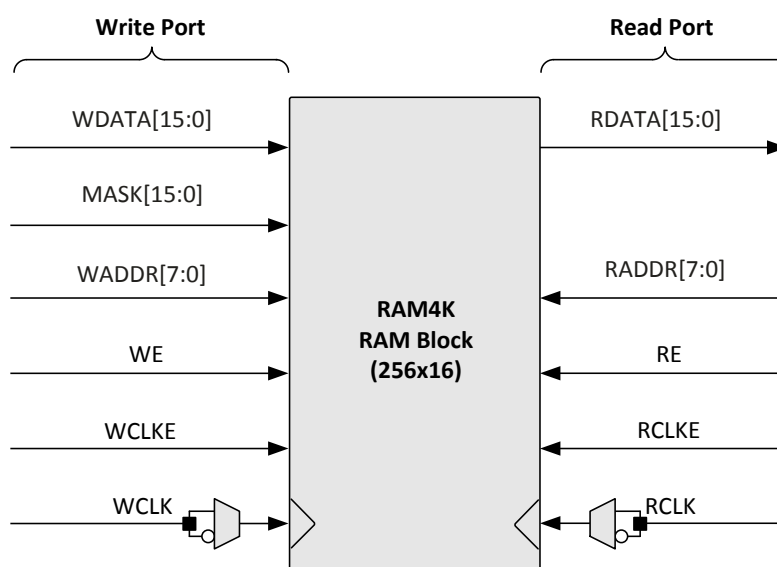
Figure 3.4. sysMEM Memory Primitives

Table 3.5 lists the EBR signals.

Table 3.5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 – Write bit 1 – Do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.

Table 3.6. SPRAM Signal Descriptions

Signal Name	Direction	Description
ADDRESS[13:0]	Input	Address input
DATAIN[15:0]	Input	Write Data input
MASKWREN[3:0]	Input	Nibble WE control
WREN	Input	Write Enable
CHIPSELECT	Input	Enable SPRAM
CLOCK	Input	Clock input
STANDY	Input	Standby Mode
SLEEP	Input	Sleep Mode
POWEROFF	Input	Switch off power source to SPRAM
DATAOUT[15:0]	Output	Output Data

For further information on sysMEM SPRAM block, refer to TN1314, iCE40 SPRAM Usage Guide.

3.1.7. sysDSP

The iCE40 UltraPlus family provides an efficient sysDSP architecture that is very suitable for low-cost Digital Signal Processing (DSP) functions for mobile applications. Typical functions used in these applications are Multiply, Accumulate, and Multiply-Accumulate. The block can also be used for simple Add and Subtract functions.

iCE40 UltraPlus sysDSP Architecture Features

The iCE40 UltraPlus sysDSP supports many functions that include the following:
- Single 16-bit x 16-bit Multiplier, or two independent 8-bit x 8-bit Multipliers
- Optional independent pipeline control on Input Register, Output Register, and Intermediate Reg faster clock performance
- Single 32-bit Accumulator, or two independent 16-bit Accumulators
- Single 32-bit, or two independent 16-bit Adder/Subtracter functions, registered or asynchronous
- Cascadable to create wider Accumulator blocks

Figure 3.6 shows the block diagram of the sysDSP block. The block consists of the Multiplier section with a bypassable Output register, Input Register, and Intermediate register between Multiplier and AC timing to achieve the highest performance.
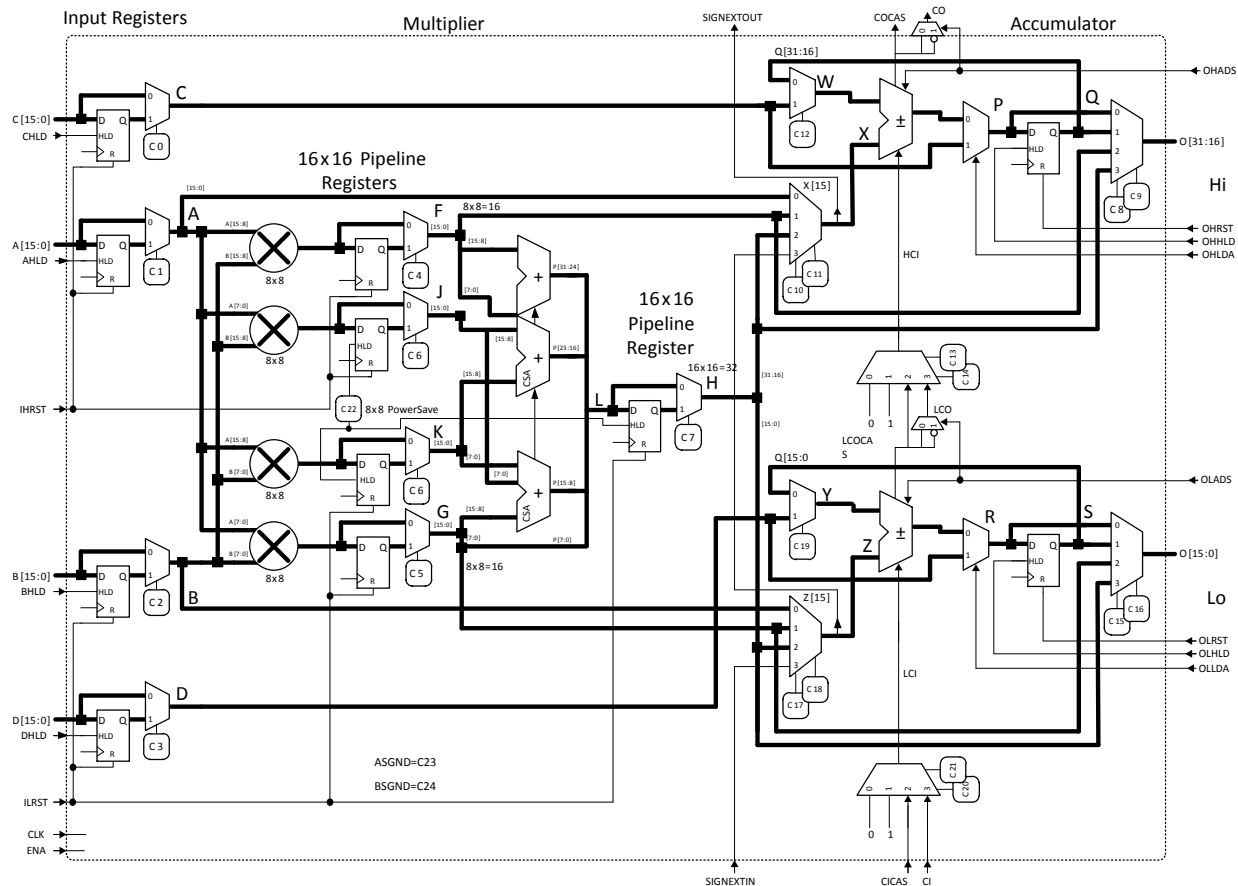
Figure 3.6. sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate)

Table 3.7. Output Block Port Description

Signal	Primitive Port Name	Width	Input/ Output	Function	Default
CLK	CLK	1	Input	Clock Input. Applies to all clocked elements in the sysDSP block	—
ENA	CE	1	Input	Clock Enable Input. Applies to all clocked elements in the sysDSP block. 0 – Not enabled 1 – Enabled	0 – Enabled
A[15:0]	A[15:0]	16	Input	Input to the A Register. Feeds the Multiplier or is a direct input to the Adder Accumulator	16'b0
B[15:0]	B[15:0]	16	Input	Input to the B Register. Feeds the Multiplier or is a direct input to the Adder Accumulator	16'b0
C[15:0]	C[15:0]	16	Input	Input to the C Register. It is a direct input to the Adder Accumulator	16'b0
D[15:0]	D[15:0]	16	Input	Input to the D Register. It is a direct input to the Adder Accumulator	16'b0
AHLD	AHOLD	1	Input	A Register Hold. 0 – Update 1 – Hold	0 – Update

Table 3.7. Output Block Port Description *(Continued)*

Signal	Primitive Port Name	Width	Input/Output	Function	Default
OLLDA	OLOADBOT	1	Input	Low-order (lower half) Accumulator Register Accumulate/Load control. 0 – Accumulate, register is loaded with Adder/Subtracter results 1 – Load, register is loaded with Input C or C Register	0 – Accumulate
OLADS	ADDSUBBOT	1	Input	Low-order (lower half) Accumulator Add or Subtract select. 0 – Add 1 – Subtract	0 – Add
CICAS	ACCUMCI	1	Input	Cascade Carry/Borrow input from previous sysDSP block	—
CI	CI	1	Input	Carry/Borrow input from lower logic tile	—
COCAS	ACCUMCO	1	Output	Cascade Carry/Borrow output to next sysDSP block	—
CO	CO	1	Output	Carry/Borrow output to higher logic tile	—
SIGNEXTIN	SIGNEXTIN	1	Input	Sign extension input from previous sysDSP block	—
SIGNEXTOUT	SIGNEXTOUT	1	Output	Sing extension output to next sysDSP block	—

The iCE40 UltraPlus sysDSP can support the following functions:
- 8-bit x 8-bit Multiplier
- 16-bit x 16-bit Multiplier
- 16-bit Adder/Subtracter
- 32-bit Adder/Subtracter
- 16-bit Accumulator
- 32-bit Accumulator
- 8-bit x 8-bit Multiply-Accumulate
- 16-bit x 16-bit Multiply-Accumulate

Figure 3.7 on the next page shows the path for an 8-bit x 8-bit Multiplier using the upper half of sysDSP block.
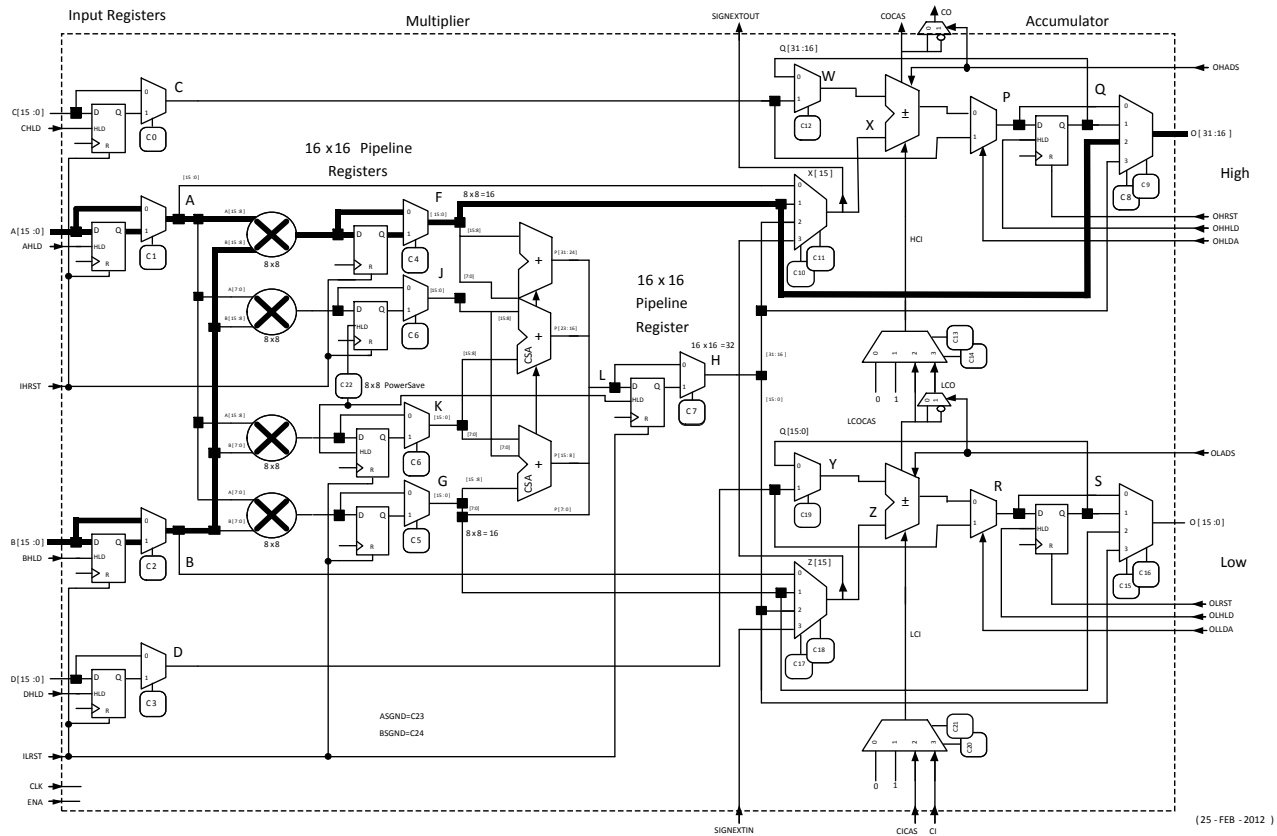
Figure 3.7. sysDSP 8-bit x 8-bit Multiplier

Figure 3.8 shows the path for an 16-bit x 16-bit Multiplier using the upper half of sysDSP block.

3.1.11. User I^{2}C IP

The iCE40 UltraPlus devices have two I^{2}C IP cores. Either of the two cores can be configured either as an I^{2}C master or as an I^{2}C slave. The pins for the I^{2}C interface are not pre-assigned. User can use any General Purpose I/O pins.

In each of the two cores, there are options to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I^{2}C components.

When the IP core is configured as master, it will be able to control other devices on the I^{2}C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I^{2}C Master. The I^{2}C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 400 kHz data transfer speed
- General Call support
- Optionally delaying input or output data, or both
- Optional filter on SCL input

For further information on the User I^{2}C, refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

3.1.12. User SPI IP

The iCE40 UltraPlus devices have two SPI IP cores. The pins for the SPI interface are not pre-assigned. User can use any General Purpose I/O pins. Both SPI IP cores can be configured as a SPI master or as a slave. When the SPI IP core is configured as a master, it controls the other SPI enabled devices connected to the SPI Bus. When SPI IP core is configured as a slave, the device will be able to interface to an external SPI master.

The SPI IP core supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer

For further information on the User SPI, refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

3.1.13. RGB High Current Drive I/O Pins

The iCE40 UltraPlus family devices offer multiple high current LED drive outputs in each device in the family to allow the iCE40 UltraPlus product to drive LED signals directly on mobile applications.

There are three outputs on each device that can sink up to 24 mA current. These outputs are open-drain outputs, and provides sinking current to an LED connecting to the positive supply. These three outputs are designed to drive the RBG LEDs, such as the service LED found in a lot of mobile devices. This RGB drive current is user programmable from 4 mA to 24 mA, in increments of 4 mA. This output functions as General Purpose I/O with open-drain when the high current drive is not needed.

3.1.14. RGB PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be used in the user design. This PWM IP provides the flexibility for user to dynamically change the modulation width of each of the RGB LED driver, which changes the color. Also, the user can dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the PWM IP, refer to TN1288, iCE40 LED Driver Usage Guide.

3.1.15. Non-Volatile Configuration Memory

All iCE40 UltraPlus devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, refer to TN1248, iCE40 Programming and Configuration.

3.2. iCE40 UltraPlus Programming and Configuration

This section describes the programming and configuration of the iCE40 UltraPlus family.

3.2.1. Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_V$_{CCIO1}$ power supply.

3.2.2. Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:
- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 UltraPlus, refer to TN1248, iCE40 Programming and Configuration.

3.2.3. Power Saving Options

The iCE40 UltraPlus devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 3.11 describes the function of these features.

Table 3.11. iCE40 UltraPlus Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

4. DC and Switching Characteristics

4.1. Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage V_{CC}	−0.5	1.42	V
Output Supply Voltage V_{CCIO}	−0.5	3.60	V
NVCM Supply Voltage V_{PP_2V5}	−0.5	3.60	V
PLL Supply Voltage V_{CCPLL}	−0.5	1.42	V
I/O Tri-state Voltage Applied	−0.5	3.60	V
Dedicated Input Voltage Applied	−0.5	3.60	V
Storage Temperature (Ambient)	−65	150	°C
Junction Temperature (T_J)	−65	125	°C

Notes:
1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	V_{PP_2V5} NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71[4]	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t_{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation		−40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10.00	30.00	°C

Notes:
1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. See the Power-up Supply Sequence section. V_{CC} and V_{CCPLL} are recommended to be tied together to the same supply with an RC-based noise filter between them. Refer to TN1252, iCE40 Hardware Checklist.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration modes subject to the condition that none of the HFOSC/LFOSC and RGB LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.
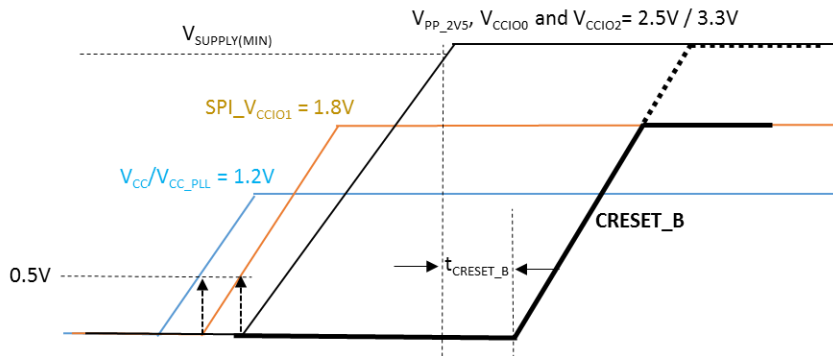
Figure 4.1. Power Up Sequence with SPE_VCCIO1 and VPP_2V5 Not Connected Together
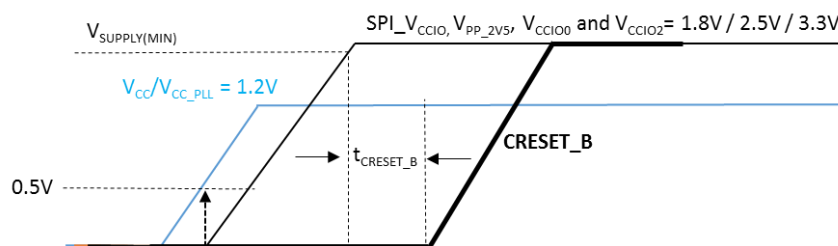
Figure 4.2. Power Up Sequence with All Supplies Connected Together to 1.8 V

4.7. Power-On-Reset Voltage Levels

Table 4.4. Power-On-Reset Voltage Levels

Symbol	Parameter		Min	Max	Unit
V_{PORUP}	Power-On-Reset ramp up trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5})	V_{CC}	0.62	0.92	V
		SPI_V_{CCIO1}	0.87	1.50	V
		V_{PP_2V5}	0.90	1.53	V
V_{PORDN}	Power-On-Reset ramp down trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5})	V_{CC}	—	0.79	V
		SPI_V_{CCIO1}	—	1.50	V
		V_{PP_2V5}	—	1.53	V

Note: These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

4.8. ESD Performance

Please contact Lattice Semiconductor for additional information.

4.11. User I²C Specifications

Table 4.7. User I²C Specifications

Symbol	Parameter	Spec (STD Mode)			Spec (FAST Mode)			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Maximum SCL clock frequency	—	—	100	—	—	400	kHz
t_{HI}	SCL clock HIGH Time	4	—	—	0.6	—	—	µs
t_{LO}	SCL clock LOW Time	4.7	—	—	1.3	—	—	µs
$t_{SU,DAT}$	Setup time (DATA)	250	—	—	100	—	—	ns
$t_{HD,DAT}$	Hold time (DATA)	0	—	—	0	—	—	ns
$t_{SU,STA}$	Setup time (START condition)	4.7	—	—	0.6	—	—	µs
$t_{HD,STA}$	Hold time (START condition)	4	—	—	0.6	—	—	µs
$t_{SU,STO}$	Setup time (STOP condition)	4	—	—	0.6	—	—	µs
t_{BUF}	Bus free time between STOP and START	4.7	—	—	1.3	—	—	µs
$t_{CO,DAT}$	SCL LOW to DATAOUT valid	—	—	3.4	—	—	0.9	µs

4.12. I²C 50 ns Delay

Table 4.8. I²C 50 ns Delay

Symbol	Parameter	Spec			Unit
		Min	Typ	Max	
T_{DELAY}	Delay through 50 ns Delay Block	—	50	—	ns

4.13. I²C 50 ns Filter

Table 4.9. I²C 50 ns Filter

Symbol	Parameter	Spec			Unit
		Min	Typ	Max	
$T_{FILTER-H}$	HIGH Pulse Filter through 50 ns Filter Block	—	50	—	ns
$T_{FILTER-L}$	LOW Pulse Filter through 50 ns Filter Block	—	50	—	ns

4.14. User SPI Specifications [1, 2]

Table 4.10. User SPI Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{MAX}	Maximum SCK clock frequency	—	—	45	MHz

Notes:

1. All setup and hold time parameters on external SPI interface are design-specific and, therefore, generated by the Lattice Design Software too. These parameters include the following:
   - $t_{SUmaster}$ master Setup Time (master mode)
   - $t_{HOLDmaster}$ master Hold time (master mode)
   - $t_{SUslave}$ slave Setup Time (slave mode)
   - $t_{HOLDslave}$ slave Hold time (slave mode)
   - $t_{SCK2OUT}$ SCK to Out Delay (slave mode)
2. The SCLK duty cycle needs to be specified in the Lattice Design Software as a timing constraint in order to ensure proper timing check on SCLK HIGH and LOW (t_{HI}, t_{LO}) time.

4.23. Maximum sysIO Buffer Performance

Table 4.19. Maximum sysIO Buffer Performance

I/O Standard	Max Speed	Unit
Inputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz
LVCMOS12	70	MHz

Note: Measured with a toggling pattern.

4.24. iCE40 UltraPlus Family Timing Adders

Over recommended commercial operating conditions.

Table 4.20. iCE40 UltraPlus Family Timing Adders

Buffer Type	Description	Timing (Typ)	Units
Input Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	ns
Output Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	-0.12	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	ns
LVCMOS12	LVCMOS, V_{CCIO} = 1.2 V	5.38	ns

Notes:
1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. Commercial timing numbers are shown.

4.29. RGB LED Drive

Table 4.25. RGB LED

Symbol	Parameter	Min	Max	Unit
ILED_ACCURACY	RGB0, RGB1, RGB2 Sink Current Accuracy to selected current @ V_{LEDOUT} >= 0.5 V	−12	+12	%
ILED_MATCH	RGB0, RGB1, RGB2 Sink Current Matching among the 3 outputs @ V_{LEDOUT} >= 0.5	−5	+5	%

4.30. Switching Test Conditions

Figure 4.3 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 4.26..
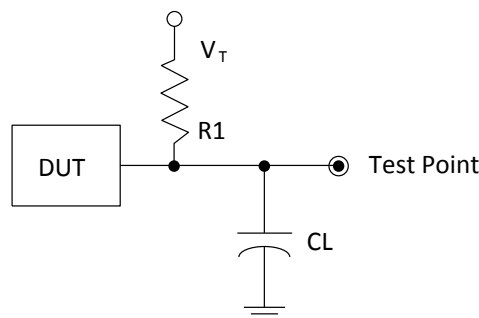

Figure 4.3. Output Test Load, LVCMOS Standards

Table 4.26. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L ≥ H, H ≥ L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = V_{CCIO}/2	—
			LVCMOS 1.8 = V_{CCIO}/2	—
LVCMOS 3.3 (Z ≥ H)	188	0 pF	1.5 V	V_{OL}
LVCMOS 3.3 (Z ≥ L)			1.5 V	V_{OH}
Other LVCMOS (Z ≥ H)			V_{CCIO}/2	V_{OL}
Other LVCMOS (Z ≥ L)			V_{CCIO}/2	V_{OH}
LVCMOS (H ≥ Z)			$V_{OH} - 0.15$ V	V_{OL}
LVCMOS (L ≥ Z)			$V_{OL} - 0.15$ V	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

IOB_33b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
IOB_35b	SPI_SS_B	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

5.1.4. Global Pins

Signal Name		Function	I/O	Description
General I/O	**Shared Function**			
IOT_46b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G0 pin drives the GBUF0 global buffer.
IOT_45a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G1 pin drives the GBUF1 global buffer.
IOB_25b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G3 pin drives the GBUF3 global buffer.
IOB_12a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G4 pin drives the GBUF4 global buffer.
IOB_11b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G5 pin drives the GBUF5 global buffer.
IOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/ reset net. The G6 pin drives the GBUF6 global buffer.

5.1.5. General I/O, LED Pins

Signal Name		Function	I/O	Description
Gerenal I/O	**Shared Function**			
RGB0	—	General I/O	Open-Drain I/O	In user mode, when RGB function is not used, this pin can be connected to any user logic and used as open-drain I/O. This pin is located in Bank 0.
		LED	Open-Drain Output	In user mode, when using RGB function, this pin can be programmed as open drain 24 mA output to drive external LED.

Supplemental Information

For Further Information

A variety of technical documents for the iCE40 UltraPlus family are available on the Lattice web site.

- TN1248, iCE40 Programming and Configuration
- TN1274, iCE40 SPI/I2C Hardened IP Usage Guide
- TN1276, Advanced iCE40 SPI/I2C Hardened IP Usage Guide
- TN1250, Memory Usage Guide for iCE40 Devices
- TN1251, iCE40 sysCLOCK PLL Design and Usage Guide
- TN1252, iCE40 Hardware Checklist
- TN1288, iCE40 LED Driver Usage Guide
- TN1295, DSP Function Usage Guide for iCE40 Devices
- TN1296, iCE40 Oscillator Usage Guide
- TN1314, iCE40 SPRAM Usage Guide
- iCE40 UltraPlus Pinout Files
- iCE40 UltraPlus Pin Migration Files
- Thermal Management document
- Package Diagrams
- Lattice design tools