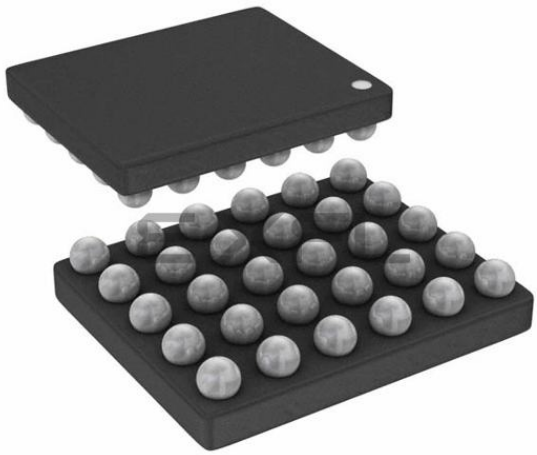
Lattice Semiconductor Corporation - ICE40UP5K-UWG30ITR1K Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	660
Number of Logic Elements/Cells	5280
Total RAM Bits	1171456
Number of I/O	21
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	30-UFBGA, WLCSP
Supplier Device Package	30-WLCSP (2.54x2.12)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40up5k-uwg30itr1k

Tables

1. General Description

iCE40 UltraPlus family from Lattice Semiconductor is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. iCE40 UltraPlus is compatible with Lattice's iCE40 Ultra family devices, containing all the functions iCE40 Ultra family has except the high current IR LED driver. In addition, the iCE40 UltraPlus features an additional 1 Mb SRAM, additional DSP blocks, with additional LUTs, all which can be used to support an always-on Voice Recognition function in the mobile devices, without the need to keep the higher power consuming voice codec on all the time.

The iCE40 UltraPlus family includes integrated SPI and I^2C blocks to interface with virtually all mobile sensors and application processors. In addition, the iCE40 UltraPlus family also features two I/O pins that can support the interface to I3C devices. There are two on-chip oscillators, 10 kHz and 48 MHz, the LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The iCE40 UltraPlus family also features DSP functional block to off-load Application Processor to pre-process information sent from the mobile device, such as voice data. The RGB PWM IP, with the three 24 mA constant current RGB outputs on the iCE40 UltraPlus provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The iCE40 UltraPlus family of devices are targeting for mobile applications to perform all the functions in iCE40 Ultra devices, such as Service LED, GPIO Expander, SDIO Level Shift, and other custom functions. In addition, the iCE40 UltraPlus family devices are also targeting for Voice Recognition application.

The iCE40 UltraPlus family features two device densities, 2800 to 5280 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I^2C interface ports or general purpose I/O's. Two of the iCE40 UltraPlus I/Os can be used to interface to higher performance I3C. It also has up to 120 kb of Block RAMs, plus 1024 kb of Single Port SRAMs to work with user logic.

1.1. Features

- Flexible Logic Architecture
  - Two devices with 2800 to 5280 LUTs
  - Offered in WLCS and QFN packages
- Ultra-low Power Devices
  - Advanced 40 nm low power process
  - As low as 100 µA standby current typical
- Embedded Memory
  - Up to 1024 kb Single Port SRAM
  - Up to 120 kb sysMEM™ Embedded Block RAM
- Two Hardened I^2C Interfaces
  - Two I/O pins to support I3C interface
- Two Hardened SPI Interfaces
- Two On-Chip Oscillators
  - Low Frequency Oscillator – 10 kHz
  - High Frequency Oscillator – 48 MHz
- 24 mA Current Drive RGB LED Outputs
  - Three drive outputs in each device
  - User selectable sink current up to 24 mA
- On-chip DSP
  - Signed and unsigned 8-bit or 16-bit functions
  - Functions include Multiplier, Accumulator, and Multiply-Accumulate (MAC)
- Flexible On-Chip Clocking
  - Eight low skew global signal resource, six can be directly driven from external pins
  - One PLL with dynamic interface per device
- Flexible Device Configuration
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- Ultra-Small Form Factor
  - As small as 2.15 mm × 2.55 mm
- Applications
  - Always-On Voice Recognition Application
  - Smartphones
  - Tablets and Consumer Handheld Devices
  - Handheld Commercial and Industrial Devices
  - Multi Sensor Management Applications
  - Sensor Pre-processing and Sensor Fusion
  - Always-On Sensor Applications
  - USB 3.1 Type C Cable Detect / Power Delivery Applications

Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, contact your local Lattice representative.

3. Architecture

3.1. Architecture Overview

The iCE40 UltraPlus family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I^2C controllers, two user configurable SPI controllers, blocks of sysMEM™ Embedded Block RAM (EBR) and Single Port RAM (SPRAM) surrounded by Programmable I/O (PIO). Figure 3.1 shows the block diagram of the iCE40UP5K device.

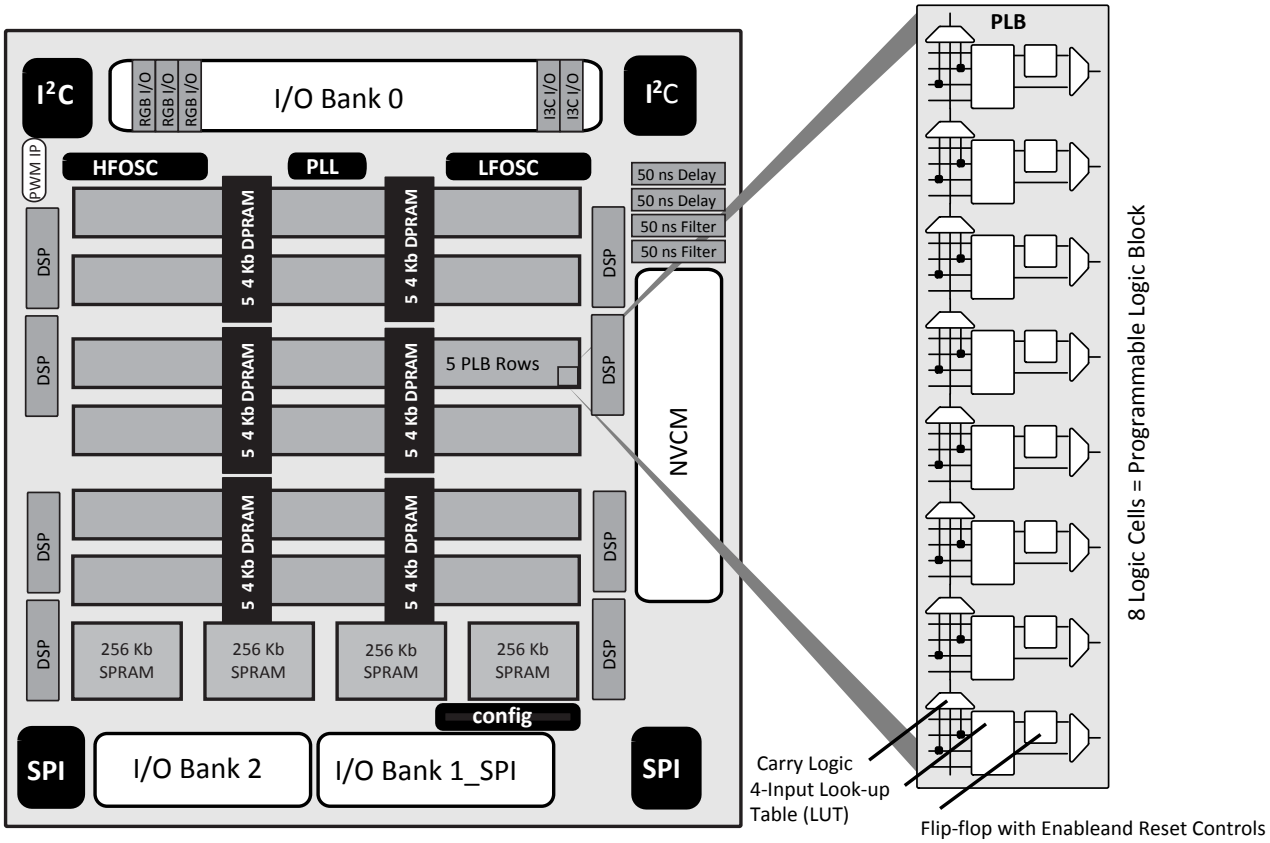

Figure 3.1. iCE40UP5K Device, Top View

The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 UltraPlus family, there are three sysIO banks, one on top and two at the bottom. User can connect some V_{CCIO}s together, if all the I/Os are using the same voltage standard. See the Power-up Supply Sequence section. The sysMEM EBRs are large 4 kb, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

In addition to the EBR, the iCE40 UltraPlus devices also feature four 256 kb SPRAM blocks that can be cascaded to create up to 1 Mb block. It is useful for temporary storage of large quantities of information.

Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

***Note**: If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

3.1.2. Routing

There are many resources provided in the iCE40 UltraPlus devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

3.1.3. Clock/Control Distribution Network

Each iCE40 UltraPlus device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 3.2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 3.2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	✓	✓	—
GBUF1		✓	—	✓
GBUF2		✓	✓	—
GBUF3		✓	—	✓
GBUF4		✓	✓	—
GBUF5		✓	—	✓
GBUF6		✓	✓	—
GBUF7		✓	—	✓

The maximum frequency for the global buffers are listed in Table 4.21.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 UltraPlus device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 UltraPlus device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

3.1.4. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 UltraPlus devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 UltraPlus global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 3.3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 UltraPlus PLL. There are two FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

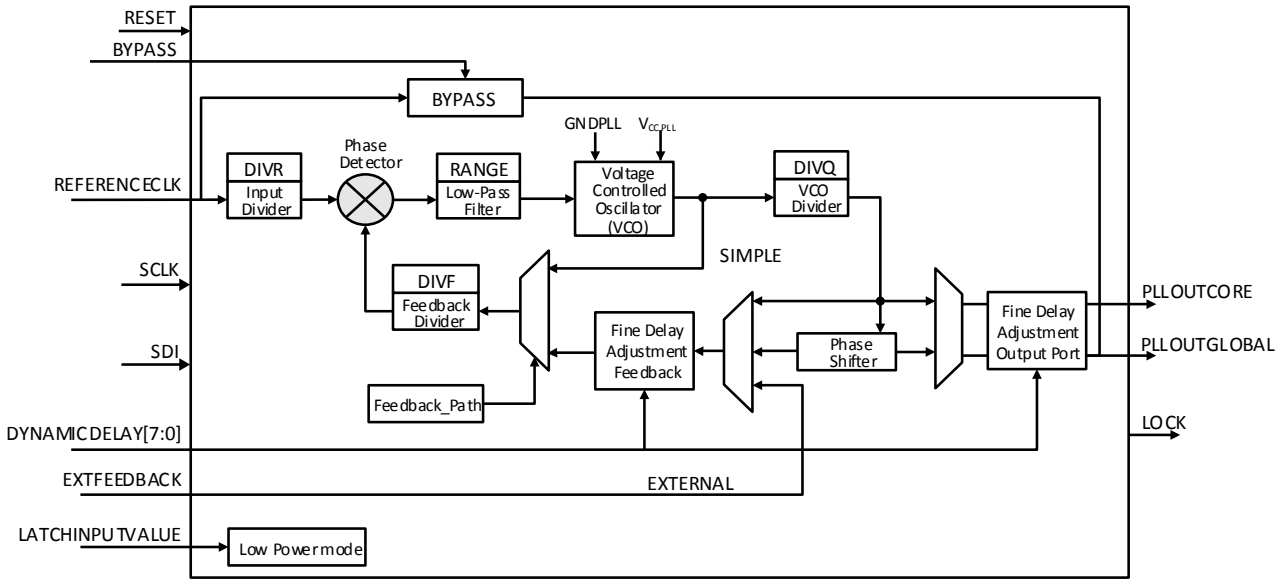

Figure 3.3. PLL Diagram

Table 3.3 provides signal descriptions of the PLL block.

Table 3.3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLLOUT output. 0 – PLL generated signal 1 – REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

3.1.5. sysMEM Embedded Block RAM Memory

Larger iCE40 UltraPlus device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as listed in Table 3.4.

Table 3.4. sysMEM Block Configurations

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4 k)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4 k)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4 k)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4 k)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

Table 3.6. SPRAM Signal Descriptions

Signal Name	Direction	Description
ADDRESS[13:0]	Input	Address input
DATAIN[15:0]	Input	Write Data input
MASKWREN[3:0]	Input	Nibble WE control
WREN	Input	Write Enable
CHIPSELECT	Input	Enable SPRAM
CLOCK	Input	Clock input
STANDY	Input	Standby Mode
SLEEP	Input	Sleep Mode
POWEROFF	Input	Switch off power source to SPRAM
DATAOUT[15:0]	Output	Output Data

For further information on sysMEM SPRAM block, refer to TN1314, iCE40 SPRAM Usage Guide.

3.1.7. sysDSP

The iCE40 UltraPlus family provides an efficient sysDSP architecture that is very suitable for low-cost Digital Signal Processing (DSP) functions for mobile applications. Typical functions used in these applications are Multiply, Accumulate, and Multiply-Accumulate. The block can also be used for simple Add and Subtract functions.

iCE40 UltraPlus sysDSP Architecture Features

The iCE40 UltraPlus sysDSP supports many functions that include the following:

- Single 16-bit x 16-bit Multiplier, or two independent 8-bit x 8-bit Multipliers
- Optional independent pipeline control on Input Register, Output Register, and Intermediate Reg faster clock performance
- Single 32-bit Accumulator, or two independent 16-bit Accumulators
- Single 32-bit, or two independent 16-bit Adder/Subtracter functions, registered or asynchronous
- Cascadable to create wider Accumulator blocks

Figure 3.6 shows the block diagram of the sysDSP block. The block consists of the Multiplier section with a bypassable Output register, Input Register, and Intermediate register between Multiplier and AC timing to achieve the highest performance.

Table 3.7. Output Block Port Description *(Continued)*

Signal	Primitive Port Name	Width	Input/ Output	Function	Default
BHLD	BHOLD	1	Input	B Register Hold. 0 – Update 1 – Hold	0 – Update
CHLD	CHOLD	1	Input	C Register Hold. 0 – Update 1 – Hold	0 – Update
DHLD	DHOLD	1	Input	D Register Hold. 0 – Update 1 – Hold	0 – Update
IHRST	IRSTTOP	1	Input	Reset input to A and C input registers, and the pipeline registers in the upper half of the Multiplier Section. 0 – No reset 1 – Reset	0 – No reset
ILRST	IRSTBOT	1	Input	Reset input to B and D input registers, and the pipeline registers in the lower half of the Multiplier Section. It also resets the Multiplier result pipeline register. 0 – No reset 1 – Reset	0 – No reset
O[31:0]	O[31:0]	32	Output	Output of the sysDSP block. This output can be: • O[31:0] – 32-bit result of 16x16 Multiplier or MAC • O[31:16] – 16-bit result of 8x8 upper half Multiplier or MAC • O[15:0] – 16-bit result of 8x8 lower half Multiplier or MAC	—
OHHLD	OHOLDTOP	1	Input	High-order (upper half) Accumulator Register Hold. 0 – Update 1 – Hold	0 – Update
OHRST	ORSTTOP	1	Input	Reset input to high-order (upper half) bits of the Accumulator Register. 0 – No reset 1 – Reset	0 – No reset
OHLDA	OLOADTOP	1	Input	High-order (upper half) Accumulator Register Accumulate/Load control. 0 – Accumulate, register is loaded with Adder/Subtracter results 1 – Load, register is loaded with Input C or C Register	0 – Accumulate
OHADS	ADDSUBTOP	1	Input	High-order (upper half) Accumulator Add or Subtract select. 0 – Add 1 – Subtract	0 – Add
OLHLD	OHOLDBOT	1	Input	Low-order (lower half) Accumulator Register Hold. 0 – Update 1 – Hold	0 – Update
OLRST	ORSTBOT	1	Input	Reset input to Low-order (lower half) bits of the Accumulator Register. 0 –No reset 1 – Reset	0 – No reset

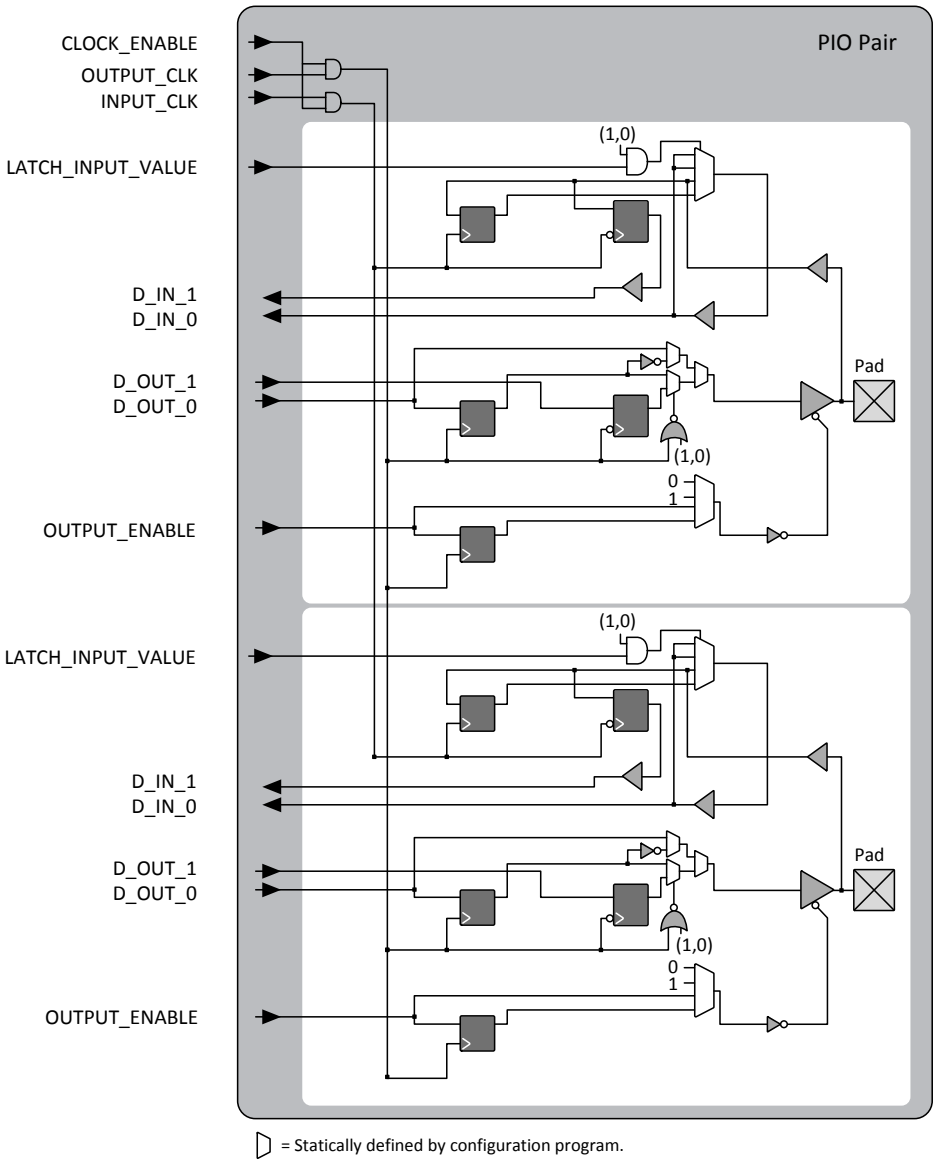

Figure 3.10. iCE I/O Register Block Diagram

Table 3.8. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

4. DC and Switching Characteristics

4.1. Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage V_{CC}	–0.5	1.42	V
Output Supply Voltage V_{CCIO}	–0.5	3.60	V
NVCM Supply Voltage V_{PP_2V5}	–0.5	3.60	V
PLL Supply Voltage V_{CCPLL}	–0.5	1.42	V
I/O Tri-state Voltage Applied	–0.5	3.60	V
Dedicated Input Voltage Applied	–0.5	3.60	V
Storage Temperature (Ambient)	–65	150	°C
Junction Temperature (T_J)	–65	125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	V_{PP_2V5} NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71[4]	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t_{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10.00	30.00	°C

Notes:

1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. See the Power-up Supply Sequence section. V_{CC} and V_{CCPLL} are recommended to be tied together to the same supply with an RC-based noise filter between them. Refer to TN1252, iCE40 Hardware Checklist.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration modes subject to the condition that none of the HFOSC/LFOSC and RGB LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

4.3. Power Supply Ramp Rates

Table 4.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies	0.6	10	V/ms

Notes:

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. See the Power-up Supply Sequence section below.

4.4. Power-On Reset

All iCE40 UltraPlus devices have on-chip Power-On-Reset (POR) circuitry to ensure proper initialization of the device. Only three supply rails are monitored by the POR circuitry as follows: (1) VCC, (2) SPI_VCCIO1 and (3) VPP_2V5. All other supply pins have no effect on the power-on reset feature of the device. Note that all supply voltage pins must be connected to power supplies for normal operation (including device configuration).

4.5. Power-up Supply Sequence

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5 V, or higher, before any subsequent power supplies in the sequence are applied.

1. **VCC** and **VCCPLL** should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the VCCPLL. Refer to TN1252, iCE40 Hardware Checklist.
2. **SPI_VCCIO1** should be the next supply, and can be applied any time after the previous supplies (VCC and VCCPLL) have reached as level of 0.5 V or higher.
3. **VPP_2V5** should be the next supply, and can be applied any time after previous supplies (VCC, VCCPLL and SPI_VCCIO1) have reached a level of 0.5 V or higher.
4. **Other Supplies** (VCCIO0 and VCCIO2) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (VCC and VCCPLL) have reached a level of 0.5 V or greater. There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are re-powered up again.

4.6. External Reset

When all power supplies have reached their minimum operating voltage defined in the Minimum Operation Condition Table, it is required to either keep CRESET_B LOW, or toggle CRESET_B from HIGH to LOW, for a duration of tCRESET_B, and release it to go HIGH, to start configuration download from either the internal NVCM or the external Flash memory. Figure 4.1 shows Power-Up sequence when SPI_VCCIO1 and VPP_2V5 are not connected together, and the CRESET_B signal triggers configuration download. shows when SPI_VCCIO1 and VPP_2V5 connected together. All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

4.11. User I²C Specifications

Table 4.7. User I²C Specifications

Symbol	Parameter	Spec (STD Mode)			Spec (FAST Mode)			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Maximum SCL clock frequency	—	—	100	—	—	400	kHz
t_{HI}	SCL clock HIGH Time	4	—	—	0.6	—	—	µs
t_{LO}	SCL clock LOW Time	4.7	—	—	1.3	—	—	µs
$t_{SU,DAT}$	Setup time (DATA)	250	—	—	100	—	—	ns
$t_{HD,DAT}$	Hold time (DATA)	0	—	—	0	—	—	ns
$t_{SU,STA}$	Setup time (START condition)	4.7	—	—	0.6	—	—	µs
$t_{HD,STA}$	Hold time (START condition)	4	—	—	0.6	—	—	µs
$t_{SU,STO}$	Setup time (STOP condition)	4	—	—	0.6	—	—	µs
t_{BUF}	Bus free time between STOP and START	4.7	—	—	1.3	—	—	µs
$t_{CO,DAT}$	SCL LOW to DATAOUT valid	—	—	3.4	—	—	0.9	µs

4.12. I²C 50 ns Delay

Table 4.8. I²C 50 ns Delay

Symbol	Parameter	Spec			Unit
		Min	Typ	Max	
T_{DELAY}	Delay through 50 ns Delay Block	—	50	—	ns

4.13. I²C 50 ns Filter

Table 4.9. I²C 50 ns Filter

Symbol	Parameter	Spec			Unit
		Min	Typ	Max	
$T_{FILTER-H}$	HIGH Pulse Filter through 50 ns Filter Block	—	50	—	ns
$T_{FILTER-L}$	LOW Pulse Filter through 50 ns Filter Block	—	50	—	ns

4.14. User SPI Specifications [1, 2]

Table 4.10. User SPI Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{MAX}	Maximum SCK clock frequency	—	—	45	MHz

Notes:

1. All setup and hold time parameters on external SPI interface are design-specific and, therefore, generated by the Lattice Design Software too. These parameters include the following:
   - $t_{SUmaster}$ master Setup Time (master mode)
   - $t_{HOLDmaster}$ master Hold time (master mode)
   - $t_{SUslave}$ slave Setup Time (slave mode)
   - $t_{HOLDslave}$ slave Hold time (slave mode)
   - $t_{SCK2OUT}$ SCK to Out Delay (slave mode)
2. The SCLK duty cycle needs to be specified in the Lattice Design Software as a timing constraint in order to ensure proper timing check on SCLK HIGH and LOW (t_{HI}, t_{LO}) time.

4.25. iCE40 UltraPlus External Switching Characteristics

Over recommended commercial operating conditions.

Table 4.21. iCE40 UltraPlus External Switching Characteristics

Parameter	Description	Device	Min	Max	Unit
Clocks					
Global Clock					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All Devices	—	185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All Devices	2	—	ns
t_{ISKEW_GBUF}	Global Buffer Clock Skew Within a Device	All Devices	—	530	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All Devices	—	9.0	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)*					
t_{SKEW_IO}	Data bus skew across a bank of IOs	All Devices	—	510	ps
t_{CO}	Clock to Output – PIO Output Register	All Devices	—	10.0	ns
t_{SU}	Clock to Data Setup – PIO Input Register	All Devices	–0.5	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	All Devices	5.55	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)					
t_{COPLL}	Clock to Output – PIO Output Register	All Devices	—	2.4	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	All Devices	7.3	—	ns
t_{HPLL}	Clock to Data Hold – PIO Input Register	All Devices	–1.1	—	ns

***Note**: All the data is from the worst case.

4.28. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 4.24. sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
All Configuration Mode						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 UltraPlus device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{SU}	CCLK setup time		6.16	—	—	ns
t_{HD}	CCLK hold time		1	—	—	ns

Notes:

1. Supported with 1.2 V V_{CC} and at 25 °C.
2. Extended range f_{MAX} Write operations support up to 53 MHz with 1.2 V V_{CC} and at 25 °C.
3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.

RGB1	—	General I/O	Open-Drain I/O	In user mode, when RGB function is not used, this pin can be connected to any user logic and used as open-drain I/O. This pin is located in Bank 0.
		LED	Open-Drain Output	In user mode, when using RGB function, this pin can be programmed as open drain 24 mA output to drive external LED.
RGB2	—	General I/O	Open-Drain I/O	In user mode, when RGB function is not used, this pin can be connected to any user logic and used as open-drain I/O. This pin is located in Bank 0.
		LED	Open-Drain Output	In user mode, when using RGB function, this pin can be programmed as open drain 24 mA output to drive external LED.
PIOT_xx	—	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location). These pins are located in Bank 0.
PIOB_xx	—	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location). Pins with xx <= 9 are located in Bank 2, pins with xx> are located in Bank 1.

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

		DC and Switching Characteristics	— Added the following figures: • Figure 4.1. Power Up Sequence with SPE_VCCIO1 and VPP_2V5 Not Connected Together. • Figure 4.2. Power Up Sequence with All Supplies Connected Together to 1.8 V. — Updated note in Table 4.5. DC Electrical Characteristics. — Added note in Table 4.6. Supply Current. — Revised User SPI Specifications 1, 2 section. • Removed symbols. • Added notes. — Revised Table 4.11. Internal Oscillators (HFOSC, LFOSC). — Removed note in Table 4.13. sysI/O Single-Ended DC Electrical Characteristics. — Changed to Lattice Design Software tool in Table 4.15. Pin-to-Pin Performance (LVCMOS25). — Changed to Lattice Design Software tool and revised note in Table 4.16. Register-to-Register Performance. — Added sysDSP Timing section. — Added SPRAM Timing section. — Removed LVCMOS12 and added timing values in Table 4.19. Maximum IO Buffer Performance. — Removed LVCMOS12 and added timing values in Table 4.20. iCE40 UltraPlus Family Timing Adders. — Revised max values in Table 4.23. SPI Master or NVCM Configuration Time. — Removed TBD conditions in Table 4.24. sysCONFIG Port Timing Specifications. Revised t_{HD} parameter. — Revised Table 4.25. High Current RGB LED and IR LED Drive.
		Pinout Information	— General update to Signal Descriptions section. — Updated the iCE40UP Part Number Description section. Added FGW49 package. — Added OPNs.
		Supplemental Information	Added reference to TN1314, iCE40 SPRAM Usage Guide.
September 2015	1.1	Architecture	Updated Architecture section. Replaced iCE5UP with iCE40UP.
		Pinout Information	Updated Pin Information Summary section. — Replaced iCE5UP with iCE40UP. — Replaced SWG30 with UWG30.
		Ordering Information	Updated iCE40UP Part Number Description section. — Replaced iCE5UP with iCE40UP. — Replaced SWG30 with UWG30.
			Updated Ordering Part Numbers section. Replaced the table of part
		Further Information	Removed reference to Schematic Symbols.
August 2015	1.0	All	Initial release.

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