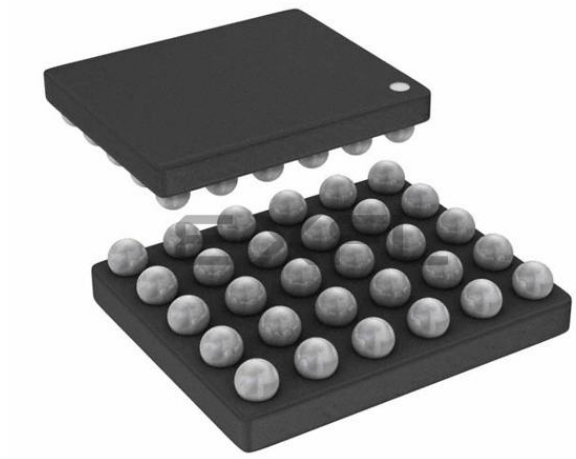
Lattice Semiconductor Corporation - ICE40UP5K-UWG30ITR50 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	660
Number of Logic Elements/Cells	5280
Total RAM Bits	1171456
Number of I/O	21
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	30-UFBGA, WLCSP
Supplier Device Package	30-WLCSP (2.54x2.12)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40up5k-uwg30itr50

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DFF	D-style Flip-Flop
DSP	Digital Signal Processor
EBR	Embedded Block RAM
HFOSC	High Frequency Oscillator
I^2C	Inter-Integrated Circuit
LFOSC	Low Frequency Oscillator
LUT	Look Up Table
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
NVCM	Non Volatile Configuration Memory
PCLK	Primary Clock
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PLB	Programmable Logic Blocks
PLL	Phase Locked Loops
SoC	System on a Chip
SPI	Serial Peripheral Interface
SPR	Single Port RAM
WLCSP	Wafer Level Chip Scale Packaging

1. General Description

iCE40 UltraPlus family from Lattice Semiconductor is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. iCE40 UltraPlus is compatible with Lattice's iCE40 Ultra family devices, containing all the functions iCE40 Ultra family has except the high current IR LED driver. In addition, the iCE40 UltraPlus features an additional 1 Mb SRAM, additional DSP blocks, with additional LUTs, all which can be used to support an always-on Voice Recognition function in the mobile devices, without the need to keep the higher power consuming voice codec on all the time.

The iCE40 UltraPlus family includes integrated SPI and I^2C blocks to interface with virtually all mobile sensors and application processors. In addition, the iCE40 UltraPlus family also features two I/O pins that can support the interface to I3C devices. There are two on-chip oscillators, 10 kHz and 48 MHz, the LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The iCE40 UltraPlus family also features DSP functional block to off-load Application Processor to pre-process information sent from the mobile device, such as voice data. The RGB PWM IP, with the three 24 mA constant current RGB outputs on the iCE40 UltraPlus provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The iCE40 UltraPlus family of devices are targeting for mobile applications to perform all the functions in iCE40 Ultra devices, such as Service LED, GPIO Expander, SDIO Level Shift, and other custom functions. In addition, the iCE40 UltraPlus family devices are also targeting for Voice Recognition application.

The iCE40 UltraPlus family features two device densities, 2800 to 5280 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/I^2C interface ports or general purpose I/O's. Two of the iCE40 UltraPlus I/Os can be used to interface to higher performance I3C. It also has up to 120 kb of Block RAMs, plus 1024 kb of Single Port SRAMs to work with user logic.

1.1. Features

- Flexible Logic Architecture
  - Two devices with 2800 to 5280 LUTs
  - Offered in WLCS and QFN packages
- Ultra-low Power Devices
  - Advanced 40 nm low power process
  - As low as 100 µA standby current typical
- Embedded Memory
  - Up to 1024 kb Single Port SRAM
  - Up to 120 kb sysMEM™ Embedded Block RAM
- Two Hardened I^2C Interfaces
  - Two I/O pins to support I3C interface
- Two Hardened SPI Interfaces
- Two On-Chip Oscillators
  - Low Frequency Oscillator – 10 kHz
  - High Frequency Oscillator – 48 MHz
- 24 mA Current Drive RGB LED Outputs
  - Three drive outputs in each device
  - User selectable sink current up to 24 mA
- On-chip DSP
  - Signed and unsigned 8-bit or 16-bit functions
  - Functions include Multiplier, Accumulator, and Multiply-Accumulate (MAC)
- Flexible On-Chip Clocking
  - Eight low skew global signal resource, six can be directly driven from external pins
  - One PLL with dynamic interface per device
- Flexible Device Configuration
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- Ultra-Small Form Factor
  - As small as 2.15 mm × 2.55 mm
- Applications
  - Always-On Voice Recognition Application
  - Smartphones
  - Tablets and Consumer Handheld Devices
  - Handheld Commercial and Industrial Devices
  - Multi Sensor Management Applications
  - Sensor Pre-processing and Sensor Fusion
  - Always-On Sensor Applications
  - USB 3.1 Type C Cable Detect / Power Delivery Applications

3.1.4. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 UltraPlus devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 UltraPlus global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 3.3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 UltraPlus PLL. There are two FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

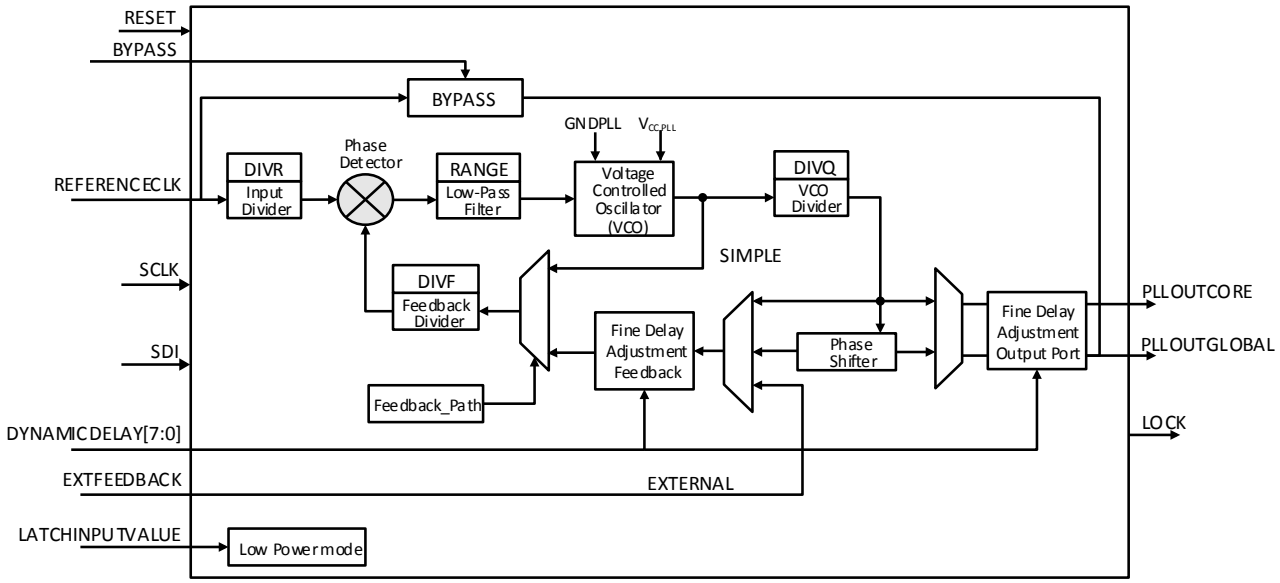

Figure 3.3. PLL Diagram

Table 3.3 provides signal descriptions of the PLL block.

Note: For iCE40 UltraPlus, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock and falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses failing-edge clocks on both Read and Write.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 3.4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

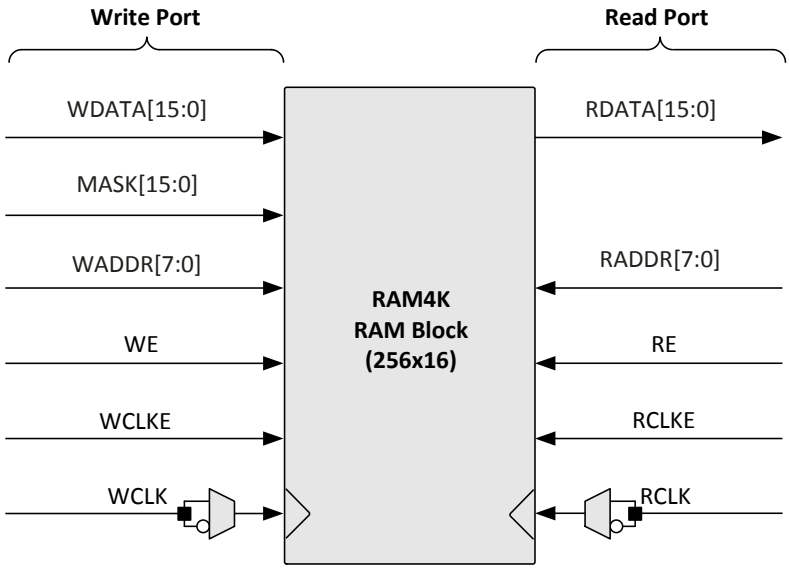

Figure 3.4. sysMEM Memory Primitives

Table 3.5 lists the EBR signals.

Table 3.5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 – Write bit 1 – Do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.

RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, refer to TN1250, Memory Usage Guide for iCE40 Devices.

3.1.6. sysMEM Single Port RAM Memory (SPRAM)

The SPRAM block is implemented to be accessed only as single port. Each block of SPRAM is designed to be 16K x 16 (256 kbits) in size. See Figure 3.5.

SPRAM Data Width

The SPRAM is designed with fixed 16-bit data width. However, the block contains nibble mask control on the write input that allows the user logic to operate the SPRAM as x4 or x8 with this control on the write side, and user logic to select which nible/byte in the read side.

SPRAM Initialization and ROM Operation

There is no pre-load into the SPRAM during device configuration, therefore, the SPRAM is not initialized after configuration.

SPRAM Cascading

Deeper SPRAM can be created using multiple SPRAM blocks, up to four blocks (64K x 16)

SPRAM Power Modes

There are three power modes in the SPRAM that the users can select during normal operation. This reduces the SPRAM block power when it Is not needed, allow lower power consumption in an always-on application. These modes are:

- **Standby Mode**: SPRAM stops all activity, and SPRAM freezes in its current state. Memory contents are retained, memory outputs are retained, and all register contents are retained.
- **Sleep Mode**: SPRAM block is shut down on all peripheral circuit, except the memory core. Memory contents are retained, memory outputs and register contents are clear and become unknown.
- **Power Off Mode**: Power source to the SPRAM is disconnected. This is the lowest power state. Memory contents are lost. Memory outputs are unknown.

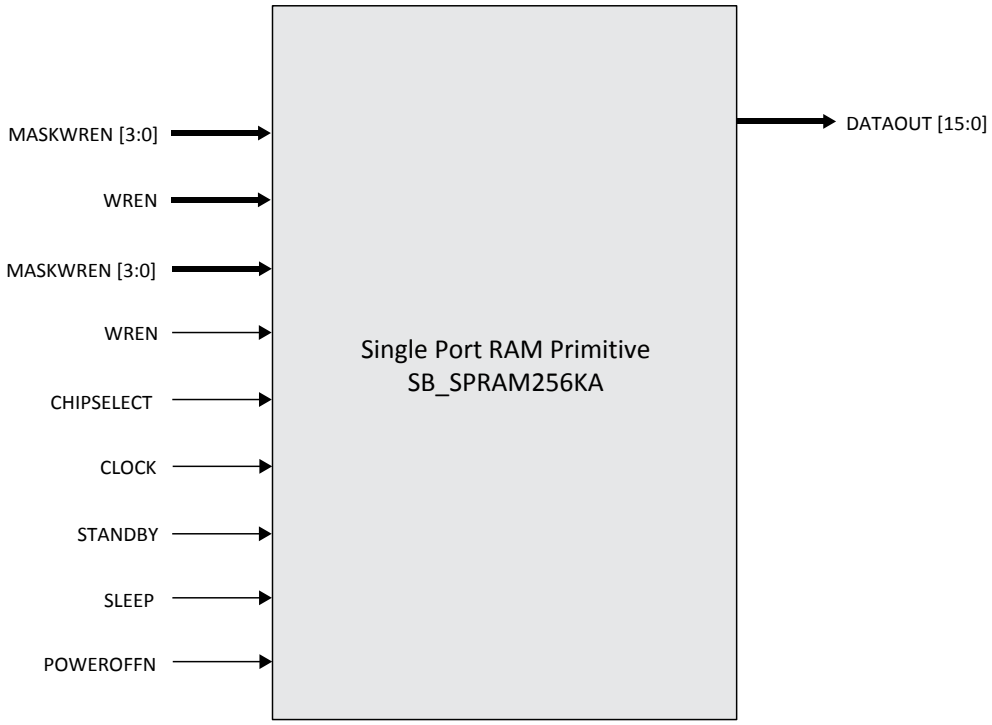

Figure 3.5. SPRAM Primitive

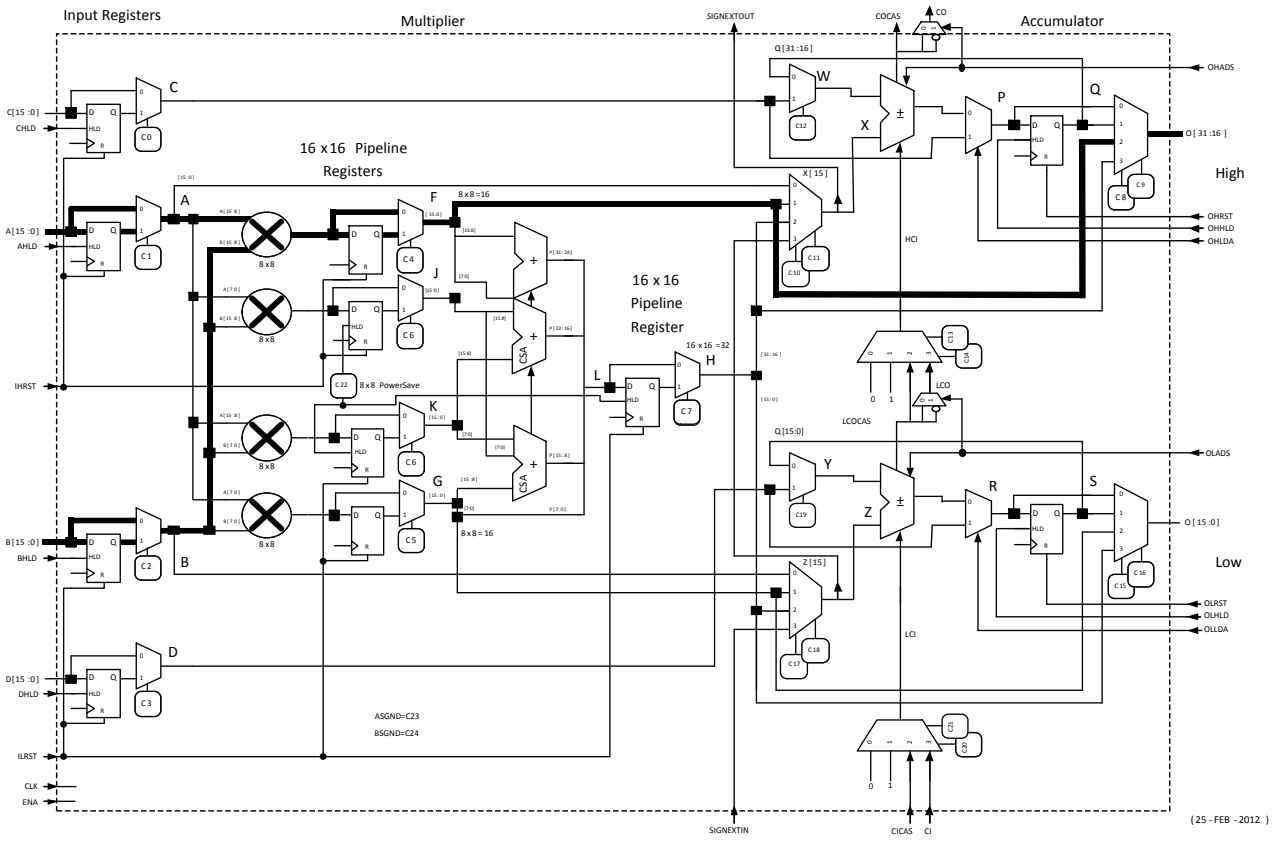

Figure 3.7. sysDSP 8-bit x 8-bit Multiplier

Figure 3.8 shows the path for an 16-bit x 16-bit Multiplier using the upper half of sysDSP block.

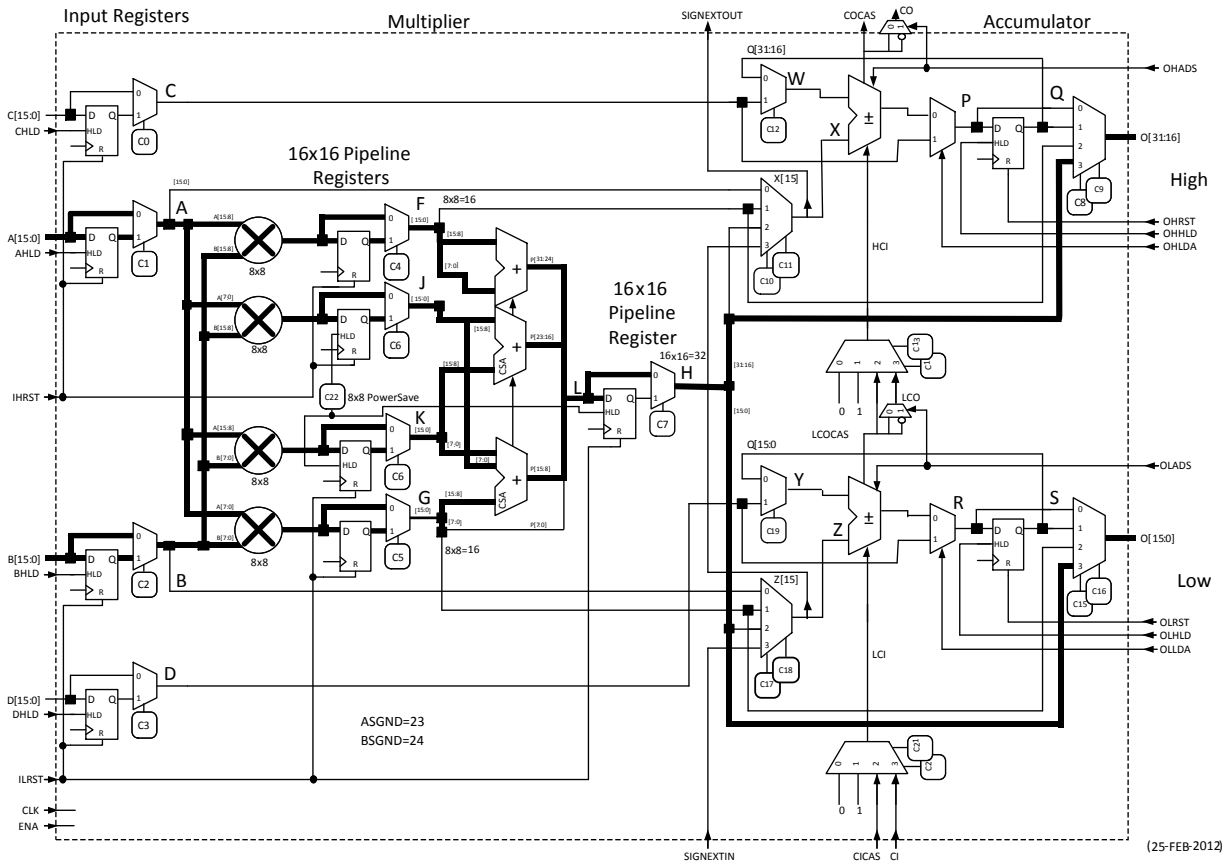

Figure 3.8. DSP 16-bit x 16-bit Multiplier

3.1.8. sysIO Buffer Banks

iCE40 UltraPlus devices have up to three I/O banks with independent V_{CCIO} rails. The configuration SPI interface signals are powered by SPI_V_{CCIO1}. Please refer to the Pin Information Summary table.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

3.1.15. Non-Volatile Configuration Memory

All iCE40 UltraPlus devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, refer to TN1248, iCE40 Programming and Configuration.

3.2. iCE40 UltraPlus Programming and Configuration

This section describes the programming and configuration of the iCE40 UltraPlus family.

3.2.1. Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_V_{CCIO1} power supply.

3.2.2. Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 UltraPlus, refer to TN1248, iCE40 Programming and Configuration.

3.2.3. Power Saving Options

The iCE40 UltraPlus devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 3.11 describes the function of these features.

Table 3.11. iCE40 UltraPlus Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

4.3. Power Supply Ramp Rates

Table 4.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies	0.6	10	V/ms

Notes:

1. Assumes monotonic ramp rates.
2. Power up sequence must be followed. See the Power-up Supply Sequence section below.

4.4. Power-On Reset

All iCE40 UltraPlus devices have on-chip Power-On-Reset (POR) circuitry to ensure proper initialization of the device. Only three supply rails are monitored by the POR circuitry as follows: (1) VCC, (2) SPI_VCCIO1 and (3) VPP_2V5. All other supply pins have no effect on the power-on reset feature of the device. Note that all supply voltage pins must be connected to power supplies for normal operation (including device configuration).

4.5. Power-up Supply Sequence

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5 V, or higher, before any subsequent power supplies in the sequence are applied.

1. **VCC** and **VCCPLL** should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the VCCPLL. Refer to TN1252, iCE40 Hardware Checklist.
2. **SPI_VCCIO1** should be the next supply, and can be applied any time after the previous supplies (VCC and VCCPLL) have reached as level of 0.5 V or higher.
3. **VPP_2V5** should be the next supply, and can be applied any time after previous supplies (VCC, VCCPLL and SPI_VCCIO1) have reached a level of 0.5 V or higher.
4. **Other Supplies** (VCCIO0 and VCCIO2) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (VCC and VCCPLL) have reached a level of 0.5 V or greater. There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are re-powered up again.

4.6. External Reset

When all power supplies have reached their minimum operating voltage defined in the Minimum Operation Condition Table, it is required to either keep CRESET_B LOW, or toggle CRESET_B from HIGH to LOW, for a duration of tCRESET_B, and release it to go HIGH, to start configuration download from either the internal NVCM or the external Flash memory. Figure 4.1 shows Power-Up sequence when SPI_VCCIO1 and VPP_2V5 are not connected together, and the CRESET_B signal triggers configuration download. shows when SPI_VCCIO1 and VPP_2V5 connected together. All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

4.11. User I²C Specifications

Table 4.7. User I²C Specifications

Symbol	Parameter	Spec (STD Mode)			Spec (FAST Mode)			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Maximum SCL clock frequency	—	—	100	—	—	400	kHz
t_{HI}	SCL clock HIGH Time	4	—	—	0.6	—	—	µs
t_{LO}	SCL clock LOW Time	4.7	—	—	1.3	—	—	µs
$t_{SU,DAT}$	Setup time (DATA)	250	—	—	100	—	—	ns
$t_{HD,DAT}$	Hold time (DATA)	0	—	—	0	—	—	ns
$t_{SU,STA}$	Setup time (START condition)	4.7	—	—	0.6	—	—	µs
$t_{HD,STA}$	Hold time (START condition)	4	—	—	0.6	—	—	µs
$t_{SU,STO}$	Setup time (STOP condition)	4	—	—	0.6	—	—	µs
t_{BUF}	Bus free time between STOP and START	4.7	—	—	1.3	—	—	µs
$t_{CO,DAT}$	SCL LOW to DATAOUT valid	—	—	3.4	—	—	0.9	µs

4.12. I²C 50 ns Delay

Table 4.8. I²C 50 ns Delay

Symbol	Parameter	Spec			Unit
		Min	Typ	Max	
T_{DELAY}	Delay through 50 ns Delay Block	—	50	—	ns

4.13. I²C 50 ns Filter

Table 4.9. I²C 50 ns Filter

Symbol	Parameter	Spec			Unit
		Min	Typ	Max	
$T_{FILTER-H}$	HIGH Pulse Filter through 50 ns Filter Block	—	50	—	ns
$T_{FILTER-L}$	LOW Pulse Filter through 50 ns Filter Block	—	50	—	ns

4.14. User SPI Specifications [1, 2]

Table 4.10. User SPI Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{MAX}	Maximum SCK clock frequency	—	—	45	MHz

Notes:

1. All setup and hold time parameters on external SPI interface are design-specific and, therefore, generated by the Lattice Design Software too. These parameters include the following:
   - $t_{SUmaster}$ master Setup Time (master mode)
   - $t_{HOLDmaster}$ master Hold time (master mode)
   - $t_{SUslave}$ slave Setup Time (slave mode)
   - $t_{HOLDslave}$ slave Hold time (slave mode)
   - $t_{SCK2OUT}$ SCK to Out Delay (slave mode)
2. The SCLK duty cycle needs to be specified in the Lattice Design Software as a timing constraint in order to ensure proper timing check on SCLK HIGH and LOW (t_{HI}, t_{LO}) time.

4.15. Internal Oscillators (HFOSC, LFOSC)

Table 4.11. Internal Oscillators (HFOSC, LFOSC)

Parameter		Parameter Description	Spec/Recommended			Unit
Symbol	Conditions		Min	Typ	Max	
f_{CLKHF}	Commercial Temp	HFOSC clock frequency (t_J = 0 °C–85 °C)	-10%	48	10%	MHz
	Industrial Temp	HFOSC clock frequency (t_J = –40 °C–100 °C)	-20%	48	20%	MHz
f_{CLKLF}	—	LFOSC CLKK clock frequency	-10%	10	10%	kHz
DCH_{CLKHF}	Commercial Temp	HFOSC Duty Cycle (t_J = 0 °C–85 °C)	45	50	55	%
	Industrial Temp	HFOSC Duty Cycle (t_J = –40 °C–100 °C)	40	50	60	%
DCH_{CLKLF}	—	LFOSC Duty Cycle (Clock High Period)	45	50	55	%
Tsync_on	—	Oscillator output synchronizer delay	—	—	5	Cycles
Tsync_off	—	Oscillator output disable delay	—	—	5	Cycles

Note: Glitchless enabling and disabling OSC clock outputs.

4.16. sysI/O Recommended Operating Conditions

Table 4.12. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min	Typ	Max
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89

4.17. sysI/O Single-Ended DC Electrical Characteristics

Table 4.13. sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}* (mA)	I_{OH} Max (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO}+0.2 V	0.4	V_{CCIO} – 0.4	8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO}+0.2 V	0.4	V_{CCIO} – 0.4	6	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	V_{CCIO}+0.2 V	0.4	V_{CCIO} – 0.4	4	–4
					0.2	V_{CCIO} – 0.2	0.1	–0.1

4.25. iCE40 UltraPlus External Switching Characteristics

Over recommended commercial operating conditions.

Table 4.21. iCE40 UltraPlus External Switching Characteristics

Parameter	Description	Device	Min	Max	Unit
Clocks					
Global Clock					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All Devices	—	185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All Devices	2	—	ns
t_{ISKEW_GBUF}	Global Buffer Clock Skew Within a Device	All Devices	—	530	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All Devices	—	9.0	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)*					
t_{SKEW_IO}	Data bus skew across a bank of IOs	All Devices	—	510	ps
t_{CO}	Clock to Output – PIO Output Register	All Devices	—	10.0	ns
t_{SU}	Clock to Data Setup – PIO Input Register	All Devices	–0.5	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	All Devices	5.55	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)					
t_{COPLL}	Clock to Output – PIO Output Register	All Devices	—	2.4	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	All Devices	7.3	—	ns
t_{HPLL}	Clock to Data Hold – PIO Input Register	All Devices	–1.1	—	ns

***Note**: All the data is from the worst case.

4.26. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 4.22. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Unit
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)	—	10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)	—	16	275	MHz
f_{VCO}	PLL VCO Frequency	—	533	1066	MHz
f_{PFD}[3]	Phase Detector Input Frequency	—	10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	40	60	%
t_{PH}	Output Phase Accuracy	—	—	±12	deg
t_{OPJIT}[1, 5, 6]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	450	ps p-p
		f_{OUT} < 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-Cycle Jitter	f_{OUT} >= 100 MHz	—	750	ps p-p
		f_{OUT} < 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} >= 25 MHz	—	275	ps p-p
		f_{PFD} < 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time	—	—	50	µs
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	f_{PFD} ≥ 20 MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable	—	—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width	—	100	—	ns
t_{RST}	RESET Pulse Width	—	10	—	ns
t_{RSTREC}	RESET Recovery Time	—	10	—	µs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width	—	100	—	VCO Cycles

Notes:

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

4.27. SPI Master or NVCM Configuration Time

Table 4.23. SPI Master or NVCM Configuration Time

Symbol	Parameter	Conditions	Max	Unit
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	140	ms
		All devices – Medium frequency	50	ms
		All devices – High frequency	26	ms

Notes:

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

4.28. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 4.24. sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
All Configuration Mode						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 UltraPlus device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{SU}	CCLK setup time		6.16	—	—	ns
t_{HD}	CCLK hold time		1	—	—	ns

Notes:

1. Supported with 1.2 V V_{CC} and at 25 °C.
2. Extended range f_{MAX} Write operations support up to 53 MHz with 1.2 V V_{CC} and at 25 °C.
3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.

4.29. RGB LED Drive

Table 4.25. RGB LED

Symbol	Parameter	Min	Max	Unit
ILED_ACCURACY	RGB0, RGB1, RGB2 Sink Current Accuracy to selected current @ V_{LEDOUT} >= 0.5 V	–12	+12	%
ILED_MATCH	RGB0, RGB1, RGB2 Sink Current Matching among the 3 outputs @ V_{LEDOUT} >= 0.5	–5	+5	%

4.30. Switching Test Conditions

Figure 4.3 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 4.26..

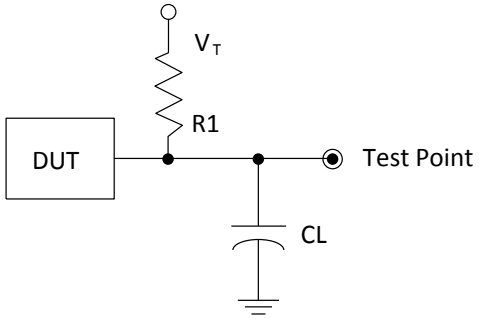

Figure 4.3. Output Test Load, LVCMOS Standards

Table 4.26. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L ≥ H, H ≥ L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z ≥ H)	188	0 pF	1.5 V	V_{OL}
LVCMOS 3.3 (Z ≥ L)			1.5 V	V_{OH}
Other LVCMOS (Z ≥ H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z ≥ L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H ≥ Z)			V_{OH} – 0.15 V	V_{OL}
LVCMOS (L ≥ Z)			V_{OL} – 0.15 V	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

5. Pinout Information

5.1. Signal Descriptions

5.1.1. Power Supply Pins

Signal Name	Function	I/O	Description
V_{CC}	Power	—	Core Power Supply
V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	Power	—	Power for I/Os in Bank 0, 1, and 2.
V_{PP_2V5}	Power	—	Power for NVCM programming and operations.
V_{CCPLL}	Power	—	Power for PLL.
GND	GROUND	—	Ground
GND_LED	GROUND	—	Ground for LED drivers. Should connect to GND on board.

5.1.2. Configuration Pins

Signal Name		Function	I/O	Description
General I/O	Shared Function			
CRESET_B	—	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10 kΩ pull-up to SPI_V_{CCIO1}.
IOB_xxx	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO1}.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function. In 30-pin WLCSP, this pin connects to IOB_12a, which also is shared as global signal G4 in user mode.

5.1.3. Configuration SPI Pins

Signal Name		Function	I/O	Description
General I/O	Shared Function			
IOB_34a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
IOB_32a	SPI_SO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

RGB1	—	General I/O	Open-Drain I/O	In user mode, when RGB function is not used, this pin can be connected to any user logic and used as open-drain I/O. This pin is located in Bank 0.
		LED	Open-Drain Output	In user mode, when using RGB function, this pin can be programmed as open drain 24 mA output to drive external LED.
RGB2	—	General I/O	Open-Drain I/O	In user mode, when RGB function is not used, this pin can be connected to any user logic and used as open-drain I/O. This pin is located in Bank 0.
		LED	Open-Drain Output	In user mode, when using RGB function, this pin can be programmed as open drain 24 mA output to drive external LED.
PIOT_xx	—	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location). These pins are located in Bank 0.
PIOB_xx	—	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location). Pins with xx <= 9 are located in Bank 2, pins with xx> are located in Bank 1.

5.2. Pin Information Summary

Pin Type		iCE40UP3K	iCE40UP5K	
		UWG30	UWG30	SG48
General Purpose I/O Per Bank	Bank 0	7	7	17
	Bank 1	10	10	14
	Bank 2	4	4	8
Total General Purpose I/Os		21	21	39
V_{CC}		1	1	2
V_{CCIO}	Bank 0	1	1	1
	Bank 1	1	1	1
	Bank 2	1	1	1
V_{CCPLL}		1	1	1
V_{PP_2V5}		1	1	1
Dedicated Config Pins		1	1	2
GND		2	2	0[1]
Total Balls		30	30	48

Note:

1. 48-pin QFN package (SG48) requires the package paddle to be connected to GND.