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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	63
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2h44e0agv20000

Table of Contents

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
52	-	-	H7	P71 TIOB4_2 BIN0_1 IC12_1 INT15_1 RX0_0	E	K
53	-	-	G7	P72 TIOA6_0 SIN2_0 ZIN0_1 IC11_1 INT14_2	E	K
54	-	-	H8	P73 TIOB6_0 SOT2_0 (SDA2_0) IC10_1 INT03_2	E	K
55	-	-	J9	P74 SCK2_0 (SCL2_0) DTTI1X_1	E	I
56	46	36	L8	PE0 MD1	C	E
57	47	37	K9	MD0	J	D
58	48	38	L9	PE2 X0	A	A
59	49	39	L10	PE3 X1	A	B
60	50	40	L11	VSS	-	-
61	51	-	K11	VCC	-	-
62	52	41	J10	P10 AN00 SIN1_1 FRCK0_2 INT02_1 MAD07_0 RX1_2	F	M
63	53	42	H10	P11 AN01 SOT1_1 (SDA1_1) IC00_2 MAD08_0 TX1_2	F	L

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
74	64	53	F8	P18 AN08 SCK2_2 (SCL2_2) MAD15_0 DTTI2X_0	F	L
75	65	54	E11	P19 AN09 SIN4_1 IC00_1 INT05_1 MAD16_0	F	M
76	66	55	E10	P1A AN10 SOT4_1 (SDA4_1) IC01_1 MAD17_0	M	L
77	67	56	E9	P1B AN11 SCK4_1 (SCL4_1) IC02_1 MAD18_0	M	L
78	68	-	E8	P1C AN12 CTS4_1 IC03_1 MAD19_0	F	L
79	69	-	D10	P1D AN13 RTS4_1 DTTI0X_1 MAD20_0	F	L
80	70	-	D9	P1E AN14 ADTG_5 FRCK0_1 MAD21_0	F	L
81	-	-	F7	P1F ADTG_4 TIOB6_2 RTO05_1 (PPG04_1)	E	I

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
89	74	-	B11	P20	F	M
				AN18		
				AIN1_1		
				INT05_0		
				MAD24_0		
				RTO25_0		
90	75	60	A11	VSS	-	-
91	76	61	A10	VCC	-	-
92	77	62	B9	P0E	L	I
				TIOB5_2		
				SCS6_1		
				IC13_0		
				MDQM1_0		
93	78	63	A9	P0D	L	I
				TIOA5_2		
				SCK6_1 (SCL6_1)		
				IC12_0		
				MDQM0_0		
94	79	64	C8	P0C	L	I
				TIOA6_1		
				SOT6_1 (SDA6_1)		
				IC11_0		
				MALE_0		
95	80	65	B8	P0B	L	K
				TIOB6_1		
				SIN6_1		
				IC10_0		
				INT00_1		
				MCSX0_0		
96	81	66	A8	P0A	L	K
				SIN1_0		
				FRCK1_0		
				INT12_2		
				MCSX1_0		

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
ADC	ADTG_0	A/D converter external trigger input pin	101	86	-	D6
	ADTG_1		7	7	7	E2
	ADTG_2		23	18	13	H1
	ADTG_3		114	94	74	C3
	ADTG_4		81	-	-	F7
	ADTG_5		80	70	-	D9
	ADTG_6		17	12	12	F2
	ADTG_7		35	30	-	H5
	ADTG_8		110	-	-	D5
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	62	52	41	J10
	AN01		63	53	42	H10
	AN02		64	54	43	H9
	AN03		65	55	44	G10
	AN04		66	56	45	G9
	AN05		67	57	46	G8
	AN06		68	58	47	F10
	AN07		69	59	48	F9
	AN08		74	64	53	F8
	AN09		75	65	54	E11
	AN10		76	66	55	E10
	AN11		77	67	56	E9
	AN12		78	68	-	E8
	AN13		79	69	-	D10
	AN14		80	70	-	D9
	AN15		86	71	57	D11
	AN16		87	72	58	C10
	AN17		88	73	59	C11
	AN18		89	74	-	B11
	AN19		97	82	67	D7
	AN20		98	83	-	C7
	AN21		99	84	-	B7
	AN22		100	85	-	A7
	AN23		101	86	-	D6
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	32	27	-	L2
	TIOA0_1		24	19	14	H2
	TIOA0_2		99	84	-	B7
	TIOB0_0	Base timer ch.0 TIOB pin	37	32	22	J4
	TIOB0_1		14	9	9	E1
	TIOB0_2		100	85	-	A7

Notes on Power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on: VBAT → VCC
VCC → AVCC → AVRH
Turning off: VCC → VBAT
AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

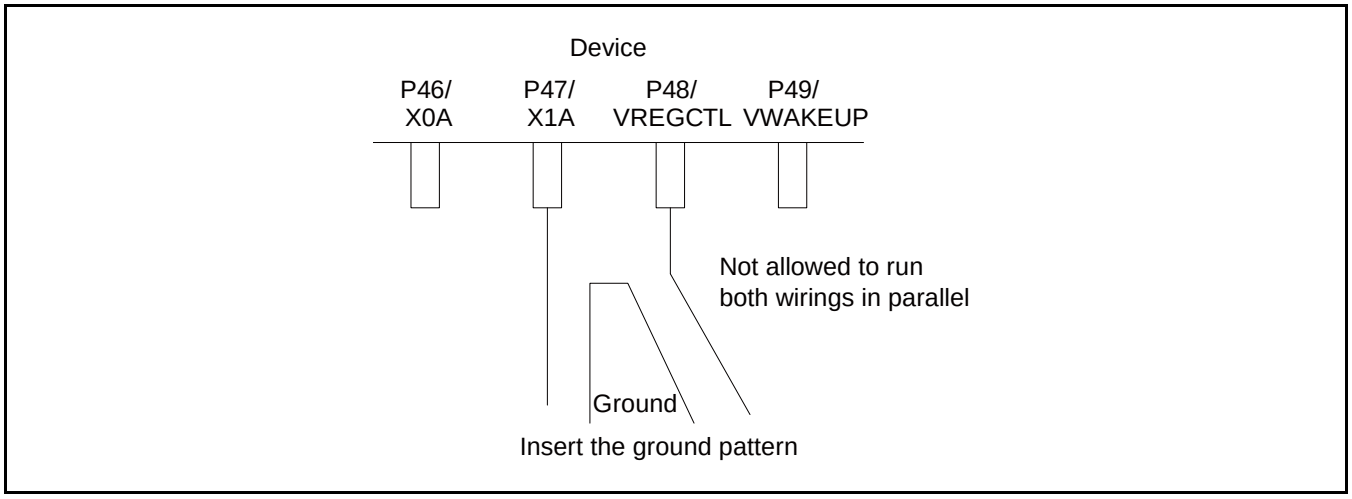
If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Adjoining Wiring on Circuit Board

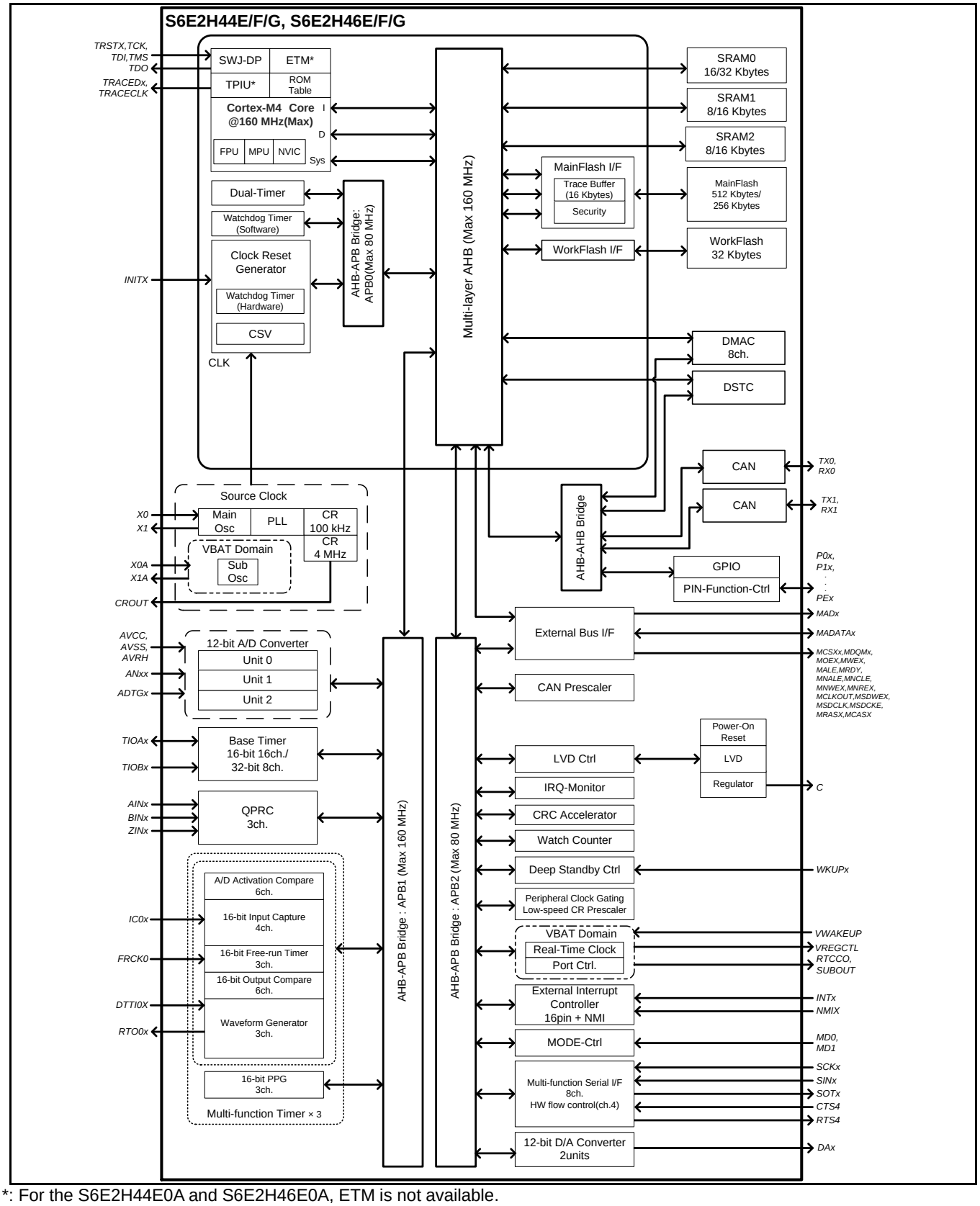
If wiring of the crystal oscillation circuit X1A adjoins and also runs in parallel with the wiring of P48/VREGCTL, there is a possibility that the oscillation erroneously counts because X1A has noise with the change of P48/VREGCTL. Keep as much distance as possible between both wirings and insert the ground pattern between them in order to avoid this possibility.



Handling when Using Debug Pins

When debug pins(TDO/TMS/TDI/TCK/TRSTX or SWO/SWDIO/SWCLK) are set to GPIO or other peripheral functions, only set them as output, do not set them as input.

8. Block Diagram



*: For the S6E2H44E0A and S6E2H46E0A, ETM is not available.

List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	VBAT Power-on reset	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Sode or Deep Standby Stop Mode State		Return from Deep Standby Mode State	VBAT RTC Mode State	Return from VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected	Setting prohibition	-
S	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected	Setting prohibition	-
T	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
T	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ or Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state /When oscillation stops, Hi-Z*	Maintain previous state /When oscillation stops, Hi-Z*	Maintain previous state /When oscillation stops, Hi-Z*	Maintain previous state /When oscillation stops, Hi-Z*	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
U	GPIO selected											

*: When The SOSCNTL bit in the WTOSCCNT Register is 0, Sub crystal oscillator output pin is maintain previous state.
When The SOSCNTL bit in the WTOSCCNT Register is 1, Oscillation is stopped at Stop mode and Deep standby Stop mode.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (VBAT) *1, *3	V_{BAT}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1, *4	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1, *4	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
"L" level maximum output current *5	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	12 mA type
			22.4	mA	I^2C Fm+
"L" level average output current *6	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			12	mA	12 mA type
			20	mA	I^2C Fm+
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total average output current *7	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current *5	I_{OH}	-	- 10	mA	4 mA type
			20	mA	8 mA type
			- 20	mA	12 mA type
"H" level average output current *6	I_{OHAV}	-	- 4	mA	4 mA type
			8	mA	8 mA type
			- 12	mA	12 mA type
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current *7	$\sum I_{OHAV}$	-	- 50	mA	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: V_{BAT} must not drop below V_{SS} - 0.5 V.

*4: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.

*7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.*
  Do not exceed any of these ratings.

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$

- I_{OL}: L level output current
- I_{OH}: H level output current
- V_{OL}: L level output voltage
- V_{OH}: H level output voltage

I_{CC} is a current consumed in device.
It can be analyzed as follows.

$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$

$I_{CC}(INT)$: Current consumed in internal logic and memory, etc. through regulator

$\Sigma I_{CC}(IO)$: Sum of current (I/O switching current) consumed in output pin

For I_{CC} (INT), it can be anticipated by "(1) Current Rating" in "3. DC Characteristics" (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For Icc (IO), it depends on system used by customers.
The calculation formula is shown below.

$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times fsw$

- C_{INT}: Pin internal load capacitance
- C_{EXT}: External load capacitance of output pin
- f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself.

1. Measure current value I_{CC} (Typ) at normal temperature (+25°C).
2. Add maximum leak current value I_{CC} (leak_max) at operating on a value in (1).

$$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$$

Parameter	Symbol	Conditions	Current Value
Maximum leak current at operating	I_{CC}(leak_max)	T_J = +125°C	16.8 mA
		T_J = +105°C	8.6 mA
		T_J = +85°C	5.8 mA

12.4.9 External Bus Timing

External Bus Clock Output Characteristics

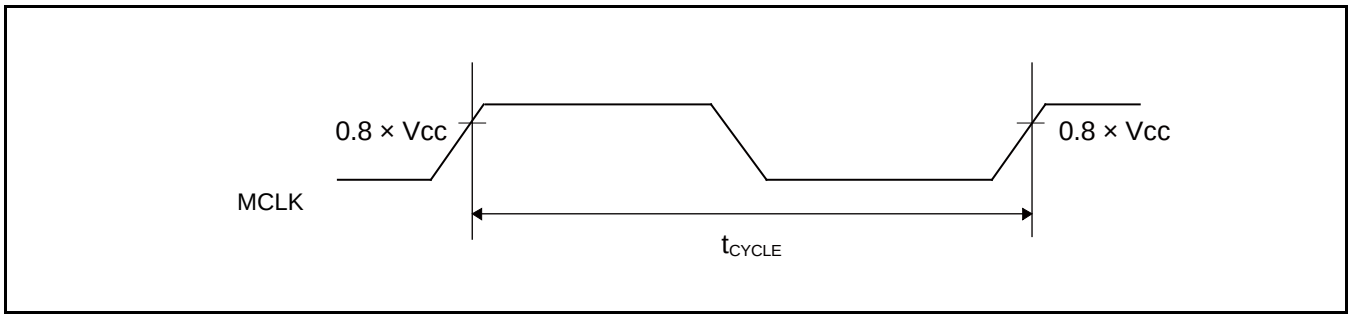
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*1	$V_{CC} \geq 4.5$ V	-	50*2	MHz
			$V_{CC} < 4.5$ V	-	32*3	MHz

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main part(MN709-00001).

*2: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 100 MHz.

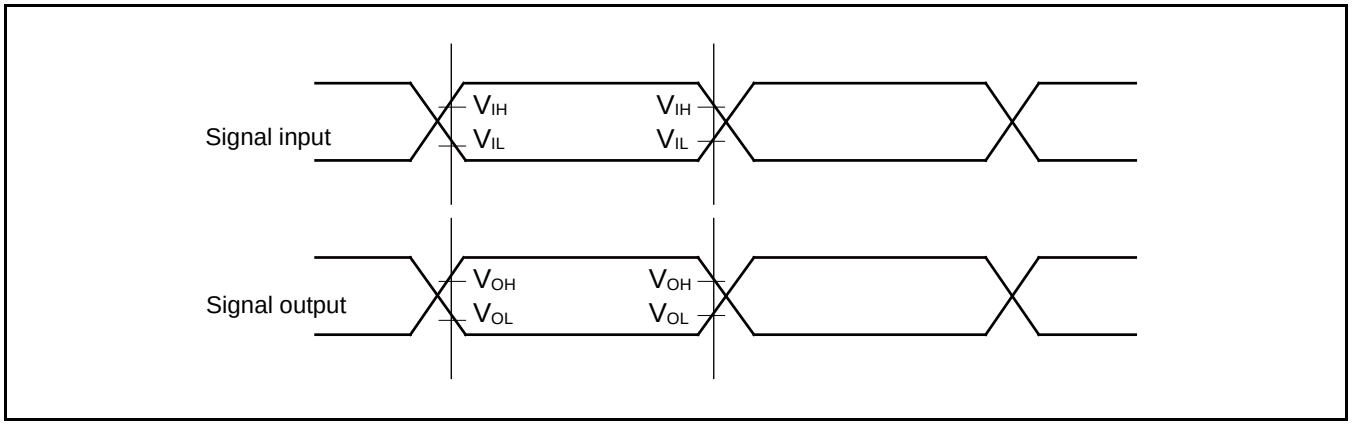
*3: Generate MCLKOUT at setting more than 4 division when the AHB bus clock exceeds 64 MHz.



External Bus Signal Input/output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	

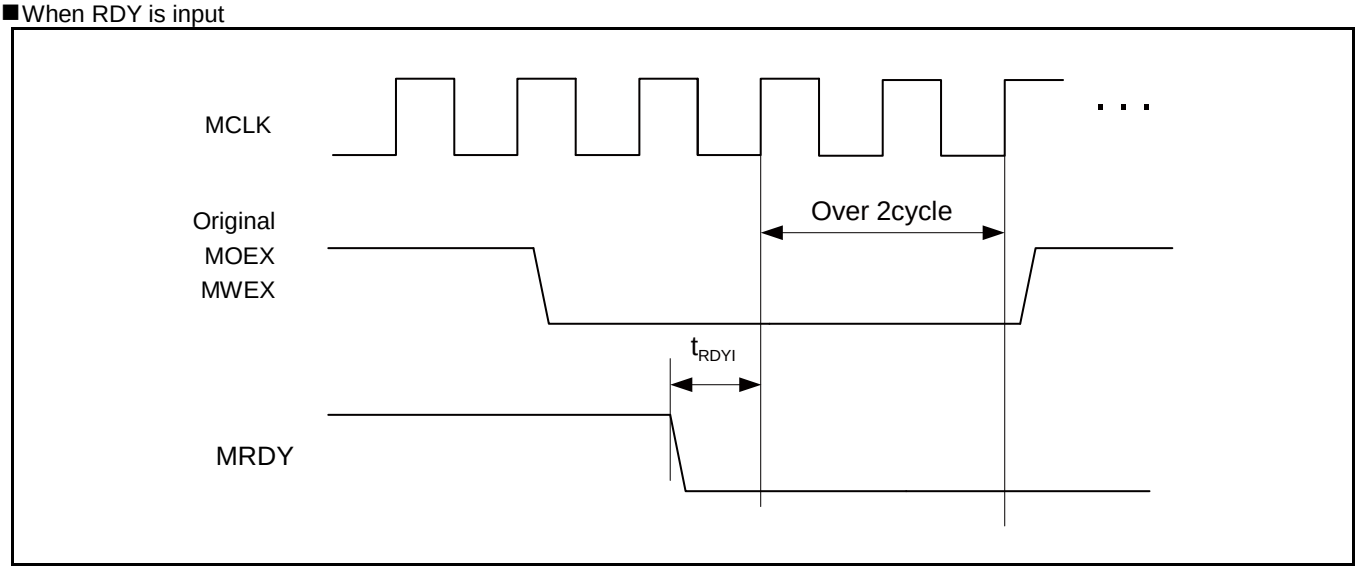


External Ready Input Timing

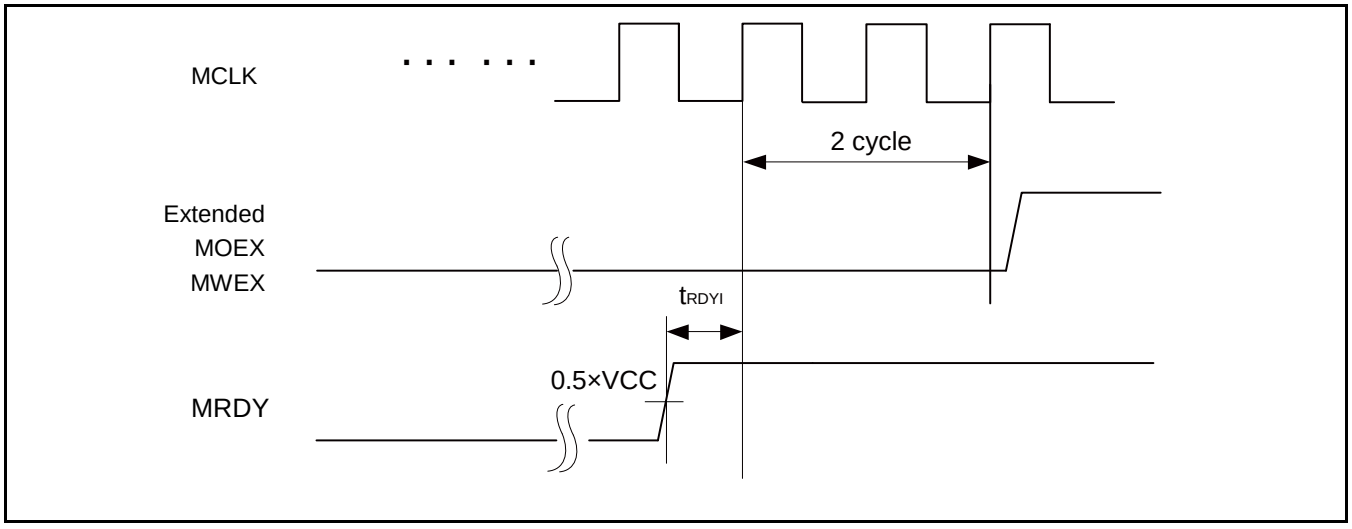
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	$V_{CC} \geq 4.5$ V	19	-	ns	
			$V_{CC} < 4.5$ V	37			

■When RDY is input



■When RDY is released



12.4.11 CSIO Timing

Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*

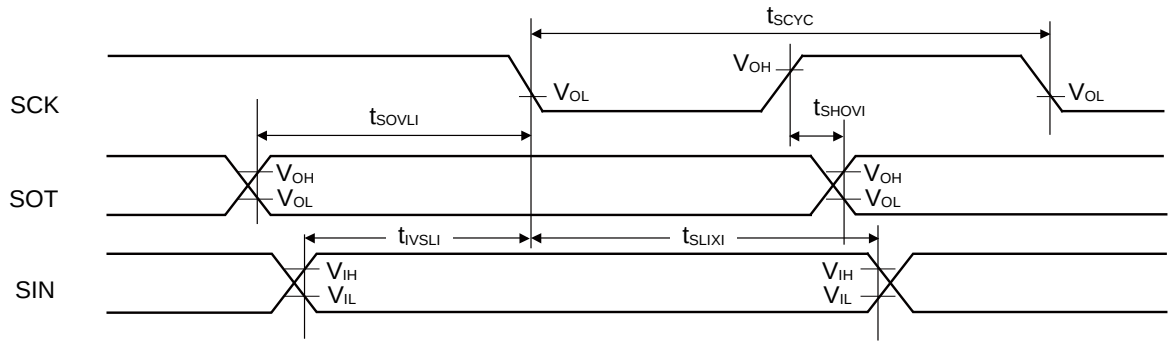
High-speed Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

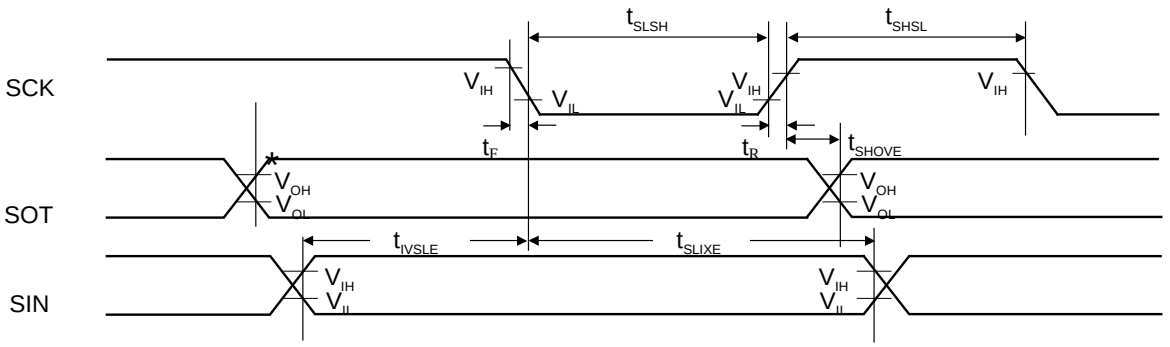
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ – 10	-	$2t_{CYCP}$ – 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
- *No chip select: SIN4_1, SOT4_1, SCK4_1*
- *Chip select: SIN6_1, SOT6_1, SCK6_1, SCS6_1*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*

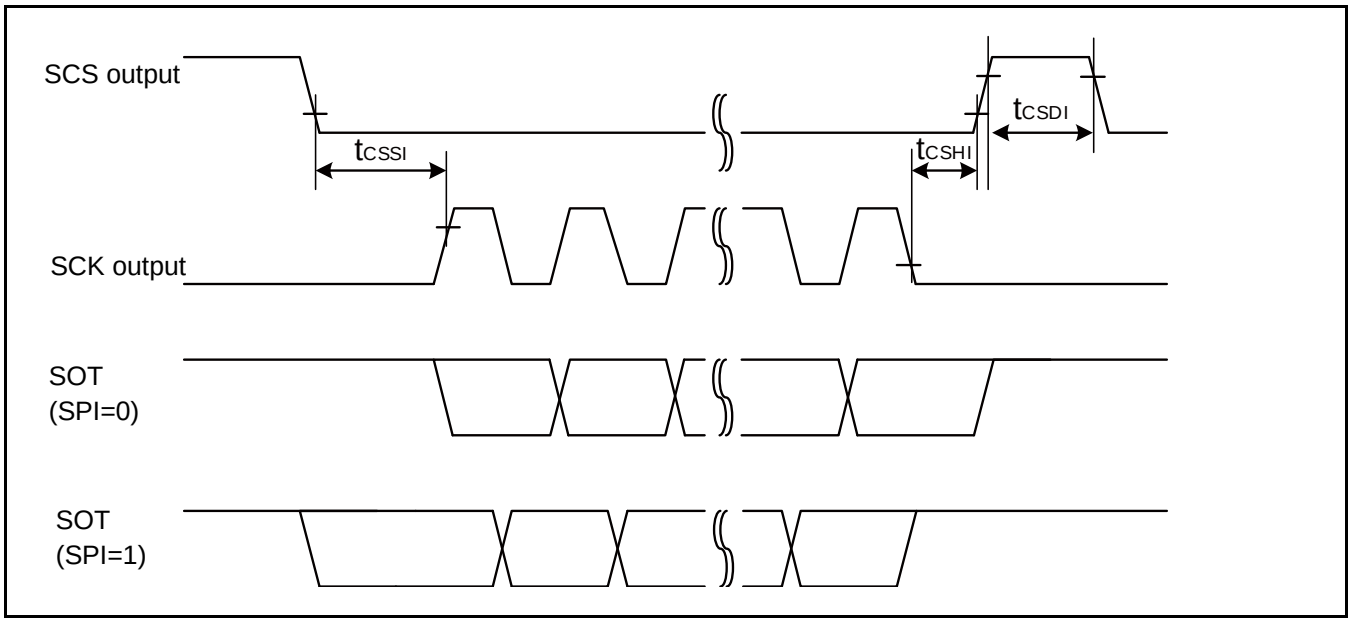


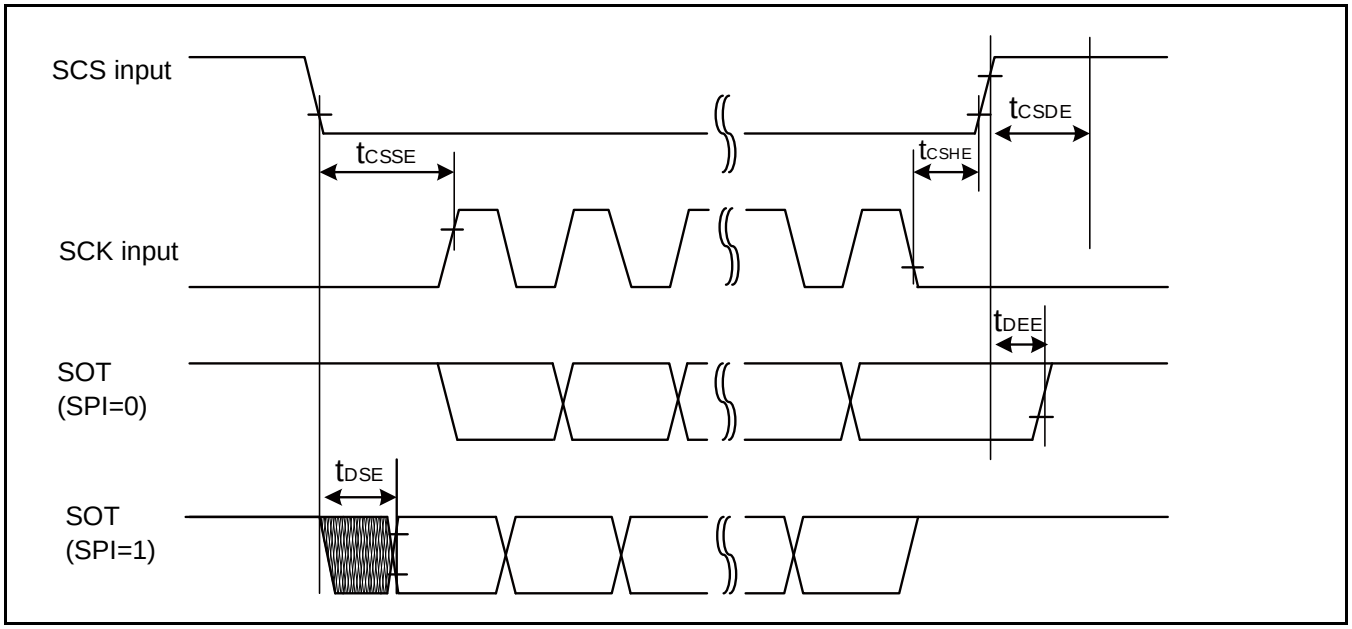
MS bit = 0

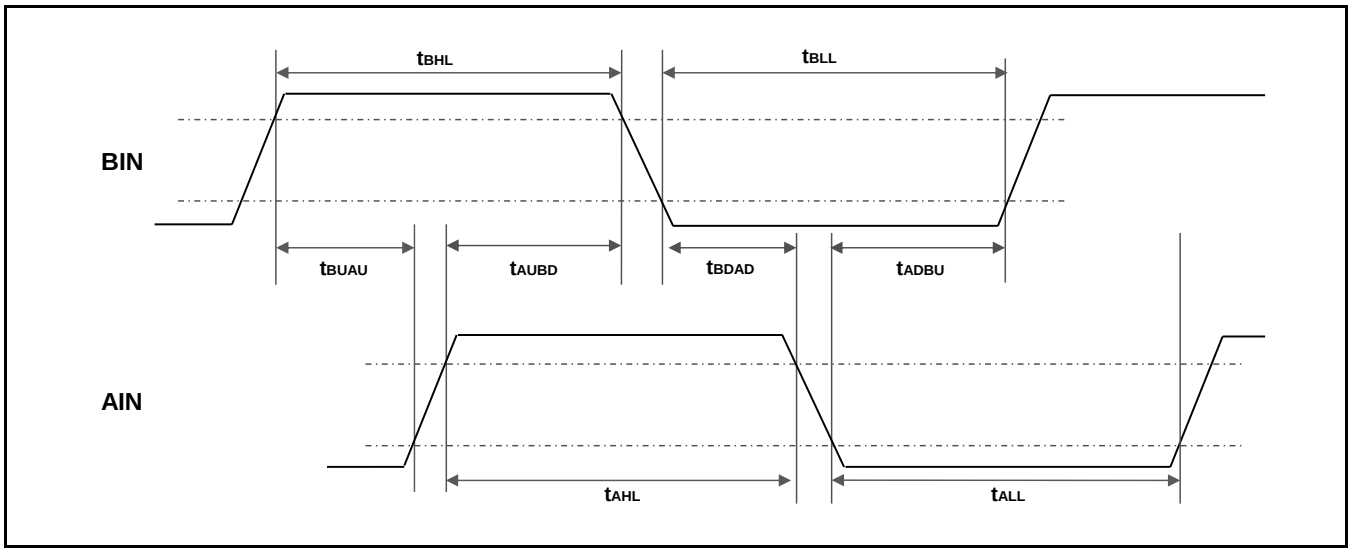


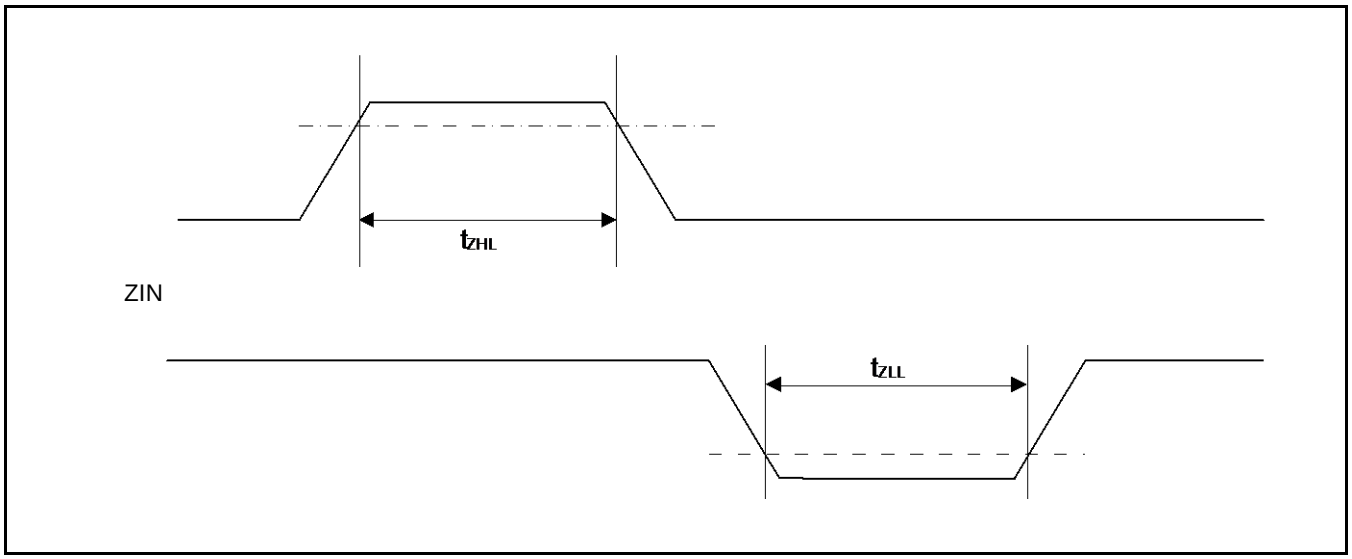
MS bit = 1

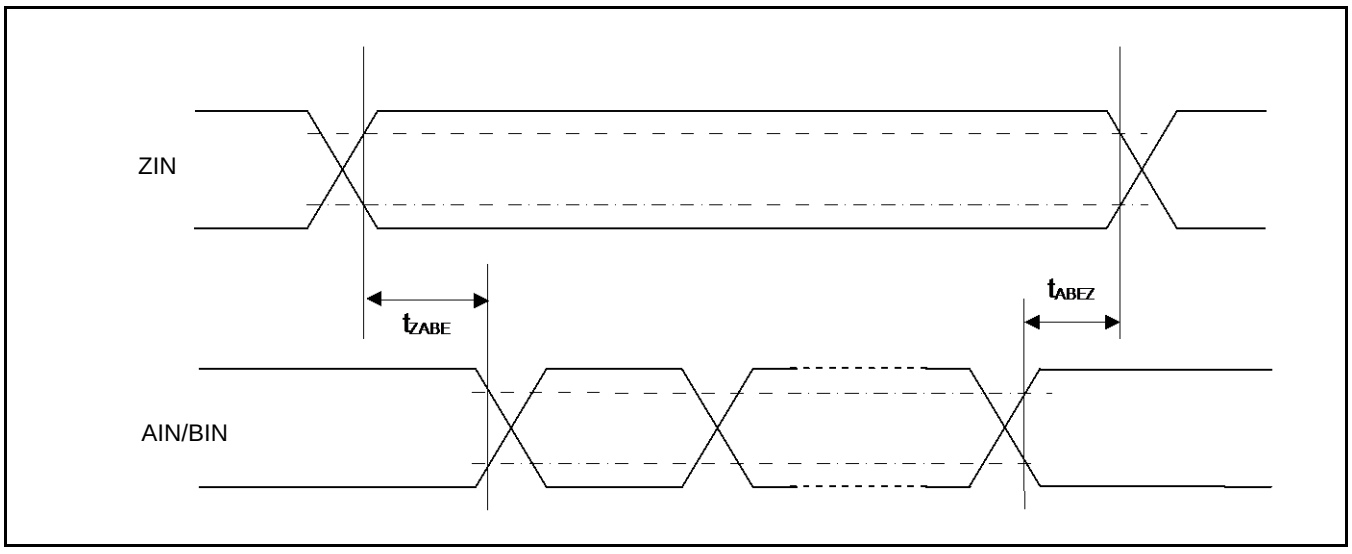
*: Changes when writing to TDR register


SCS output
tCSSI
tCSDI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSDE
tCSSE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)


tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

Document History

Document Title: S6E2H4 Series 32-bit ARM® Cortex®-M4F, FM4 Microcontroller
Document Number: 001-98941

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4869576	YUIA	08/18/2015	New Spec.
*A	4932844	YUIA	10/02/2015	Changed status from Preliminary to Final. Updated 12.2 Recommended Operating Conditions: Added the "Smoothing capacitor (C_S)". Added the “Current Value” in “Maximum leak current at operating”. Updated 12.3.1 Current Rating: Updated Table 12-1 ~ 12-9: Added the “MAX” value. Updated Table 12-11: Added voltage and temperature information. Updated 12.10.1 Recovery Cause: Interrupt/WKUP: Updated Recovery Count Time. Updated 12.10.2 Recovery Cause: Reset: Updated Recovery Count Time.
*B	5027946	YUIA	11/26/2015	Updated 2 Packages: Changed FBGA to“Supported” from “Under development”. Updated 4 Pin Description: Added “Note” about TAP pins. Updated 12.5 12-bit A/D Converter: Updated “Zero transition” and “Full-scale transition” value. Added “Total error”.

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