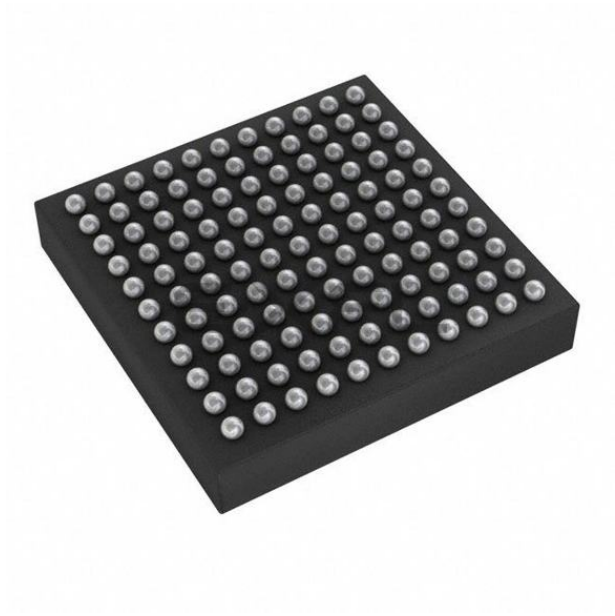

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2h44g0agb3000a

4. Pin Description

List of Pin Numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

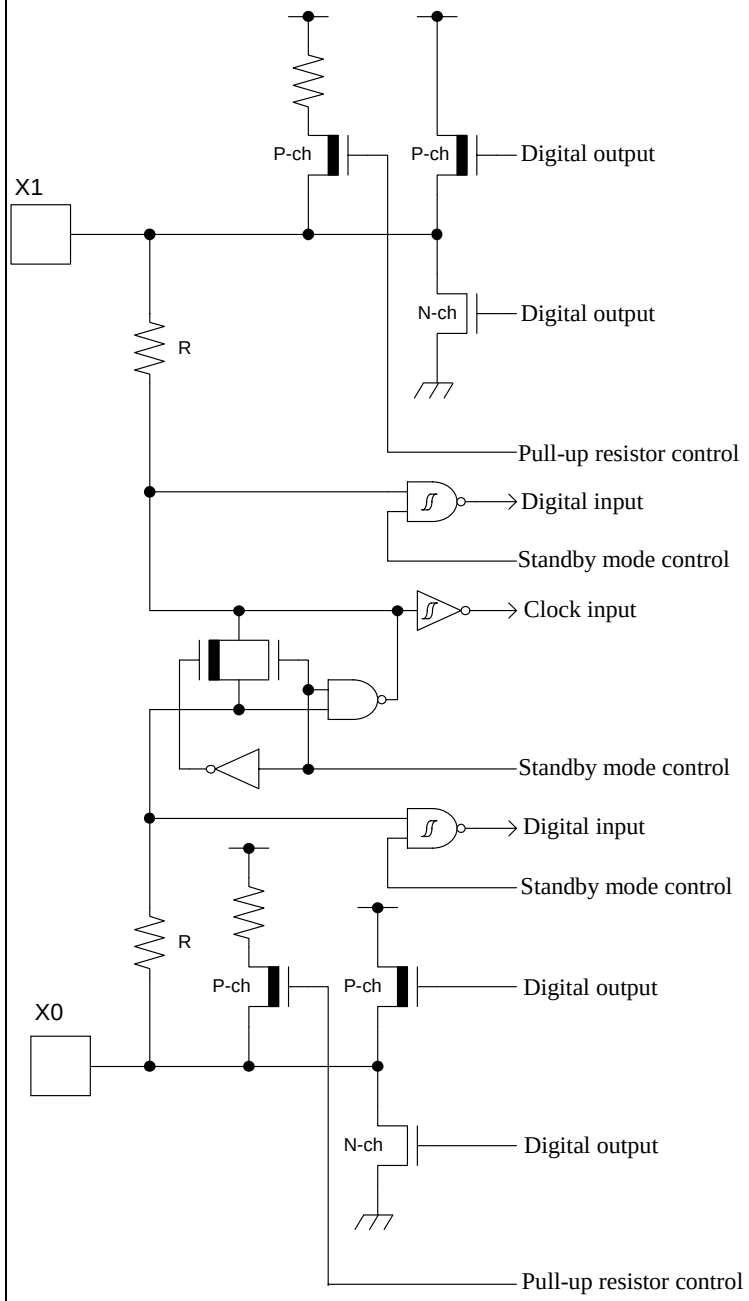
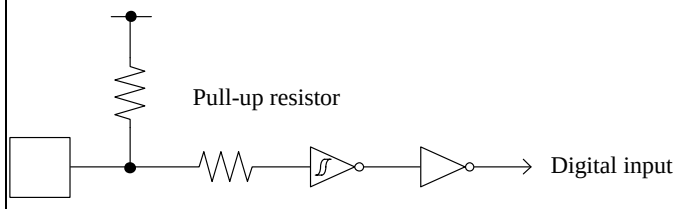
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
1	1	1	B1	VCC	-	-
2	2	2	C1	P50	E	K
				CTS4_0		
				AIN0_2		
				RTO10_0 (PPG10_0)		
				INT00_0		
				MADATA00_0		
3	3	3	C2	P51	E	K
				RTS4_0		
				BIN0_2		
				RTO11_0 (PPG10_0)		
				INT01_0		
				MADATA01_0		
4	4	4	D1	P52	E	I
				SCK4_0 (SCL4_0)		
				ZIN0_2		
				RTO12_0 (PPG12_0)		
				MADATA02_0		
5	5	5	D2	P53	E	I
				TIOA1_2		
				SOT4_0 (SDA4_0)		
				RTO13_0 (PPG12_0)		
				MADATA03_0		
6	6	6	D3	P54	E	K
				TIOB1_2		
				SIN4_0		
				RTO14_0 (PPG14_0)		
				INT02_0		
				MADATA04_0		

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
GPIO	P30	General-purpose I/O port 3	14	9	9	E1
	P31		15	10	10	F4
	P32		16	11	11	F3
	P33		17	12	12	F2
	P34		18	13	-	F1
	P35		19	14	-	G1
	P36		20	15	-	G2
	P37		21	16	-	G3
	P38		22	17	-	G4
	P39		23	18	13	H1
	P3A		24	19	14	H2
	P3B		25	20	15	H3
	P3C		26	21	16	H4
	P3D		27	22	17	J1
	P3E		28	23	18	J2
	P3F		29	24	19	K2
	P40	General-purpose I/O port 4	32	27	-	L2
	P41		33	28	-	J3
	P42		34	29	-	J5
	P43		35	30	-	H5
	P44		36	31	21	K3
	P45		37	32	22	J4
	P46		39	34	24	L4
	P47		40	35	25	K4
	P48		41	36	26	K5
	P49		42	37	27	K6
	P4B		47	42	32	J6
	P4C		48	43	33	J7
	P4D		49	44	34	J8
	P4E		50	45	35	K8
	P50	General-purpose I/O port 5	2	2	2	C1
	P51		3	3	3	C2
	P52		4	4	4	D1
	P53		5	5	5	D2
	P54		6	6	6	D3
	P55		7	7	7	E2
	P56		8	8	8	E3
	P57		9	-	-	E4
	P58		10	-	-	F5
	P59		11	-	-	F6
	P5A		12	-	-	G5
	P5B		13	-	-	G6

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
GPIO	P60	General-purpose I/O port 6	116	96	76	B2
	P61		115	95	75	B3
	P62		114	94	74	C3
	P63		113	93	73	B4
	P64		112	-	-	C4
	P65		111	-	-	D4
	P66		110	-	-	D5
	P67		109	-	-	E5
	P68		108	-	-	E6
	P70	General-purpose I/O port 7	51	-	-	H6
	P71		52	-	-	H7
	P72		53	-	-	G7
	P73		54	-	-	H8
	P74		55	-	-	J9
	P80	General-purpose I/O port 8	118	98	78	A3
	P81		119	99	79	A2
	PE0	General-purpose I/O port E	56	46	36	L8
	PE2		58	48	38	L9
	PE3		59	49	39	L10
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	88	73	59	C11
	SIN0_1		65	55	44	G10
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I2C (operation mode 4).	87	72	58	C10
	SOT0_1 (SDA0_1)		66	56	45	G9
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SCL0 when it is used in an I2C (operation mode 4).	86	71	57	D11
	SCK0_1 (SCL0_1)		67	57	46	G8
Multi-function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	96	81	66	A8
	SIN1_1		62	52	41	J10
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I2C (operation mode 4).	97	82	67	D7
	SOT1_1 (SDA1_1)		63	53	42	H10
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 2) and as SCL1 when it is used in an I2C (operation mode 4).	98	83	-	C7
	SCK1_1 (SCL1_1)		64	54	43	H9

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	7	7	7	E2
	SIN6_1		95	80	65	B8
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I2C (operation mode 4).	8	8	8	E3
	SOT6_1 (SDA6_1)		94	79	64	C8
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation modes 2) and as SCL6 when it is used in an I2C (operation mode 4).	9	-	-	E4
	SCK6_1 (SCL6_1)		93	78	63	A9
	SCS6_1	Multi-function serial interface ch.6 serial chip select pin	92	77	62	B9
Multi-function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	101	86	-	D6
	SIN7_1		50	45	35	K8
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I2C (operation mode 4).	100	85	-	A7
	SOT7_1 (SDA7_1)		49	44	34	J8
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation modes 2) and as SCL7 when it is used in an I2C (operation mode 4).	99	84	-	B7
	SCK7_1 (SCL7_1)		48	43	33	J7
	SCS7_1	Multi-function serial interface ch.7 serial chip select pin	47	42	32	J6

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. – Oscillation feedback resistor : Approximately 1MΩ – With Standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50 kΩ – I_{OH} = -4 mA, I_{OL} = 4 mA
B		– CMOS level hysteresis input – Pull-up resistor : Approximately 50 kΩ

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (FBGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation(other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation *5 (main oscillation)	4MHz	2.1	22	mA	*3 When all peripheral clocks are ON
					1.3	22	mA	*3 When all peripheral clocks are OFF
			Sleep operation (built-in high-speed CR)	4 MHz	1.3	22	mA	*3 When all peripheral clocks are ON
					0.8	21	mA	*3 When all peripheral clocks are OFF
			Sleep operation (sub oscillation)	32 kHz	0.28	21	mA	*3 When all peripheral clocks are ON
					0.27	21	mA	*3 When all peripheral clocks are OFF
			Sleep operation (built-in low-speed CR)	100 kHz	0.29	21	mA	*3 When all peripheral clocks are ON
					0.28	21	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

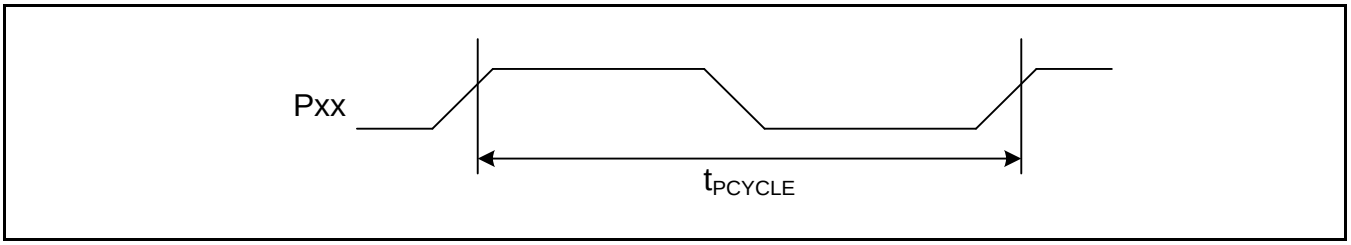
*5: When using the crystal oscillator of 4 M Hz (including the current consumption of the oscillation circuit)

12.4.8 GPIO Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{PCYCLE}	Pxx*	$V_{CC} \geq 4.5$ V	-	50	MHz
			$V_{CC} < 4.5$ V	-	32	MHz

*: GPIO is a target.



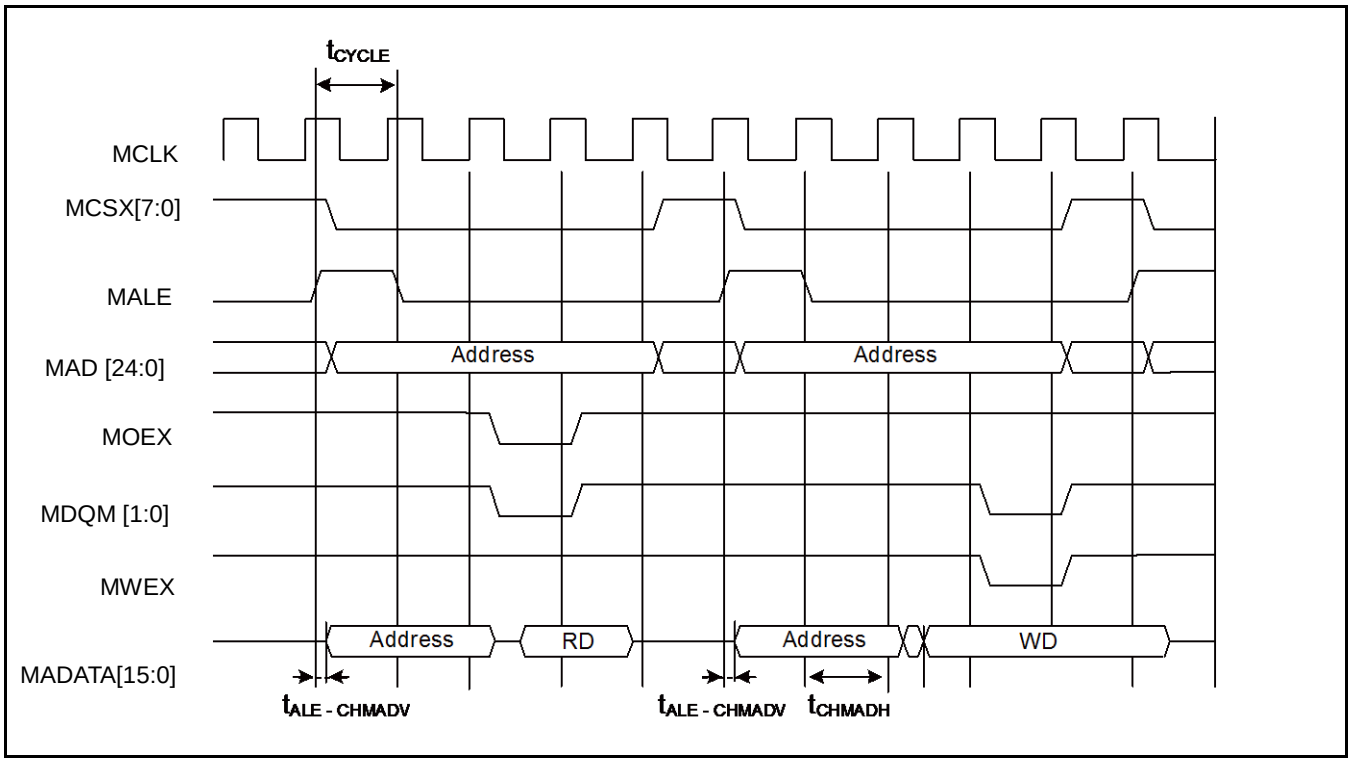
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	10	ns
			$V_{CC} < 4.5$ V		20	
Multiplexed address hold time	t_{CHMADH}		$V_{CC} \geq 4.5$ V	MCLK×n+0	MCLK×n+10	ns
			$V_{CC} < 4.5$ V	MCLK×n+0	MCLK×n+20	

Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*

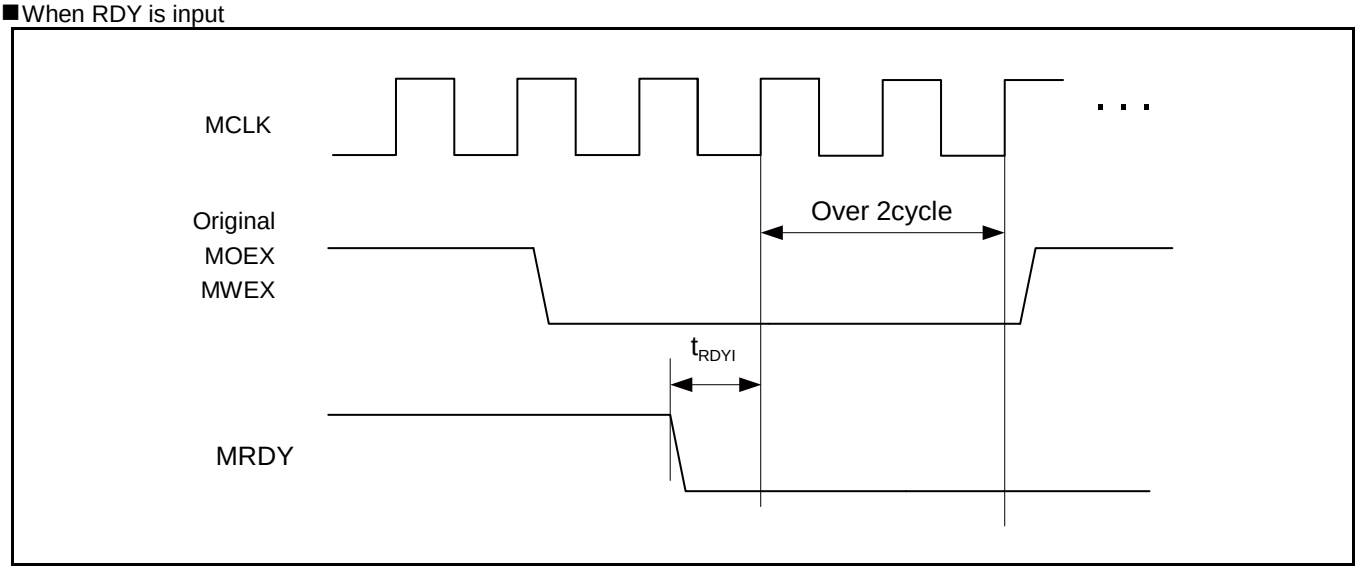


External Ready Input Timing

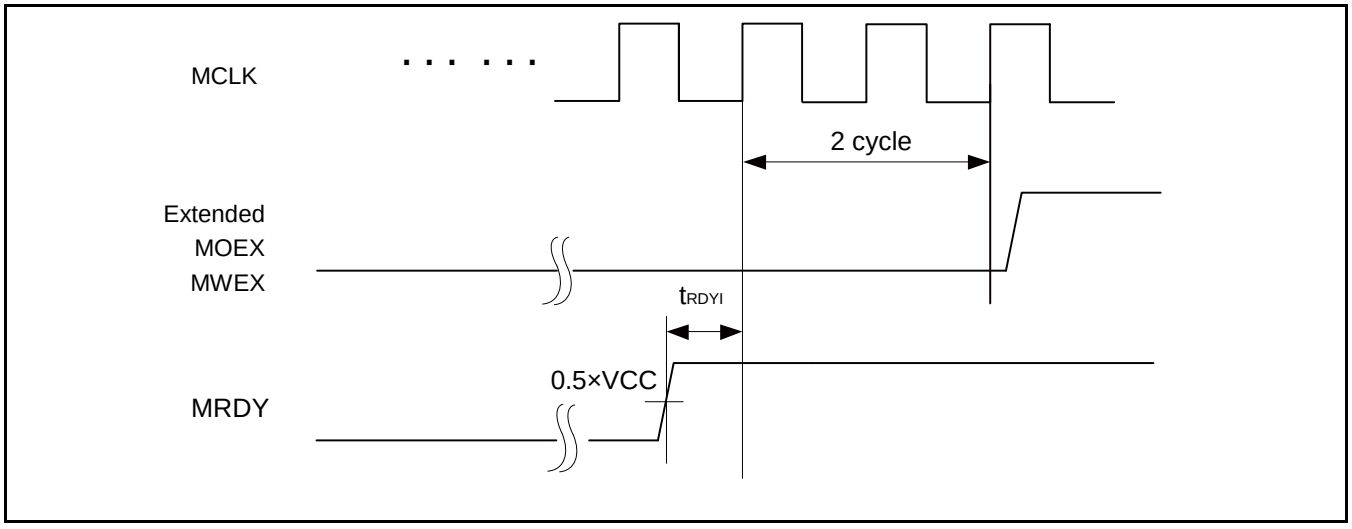
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	$V_{CC} \geq 4.5$ V	19	-	ns	
			$V_{CC} < 4.5$ V	37			

■When RDY is input



■When RDY is released



When Using Synchronous Serial Chip Select (SPI = 1, SCINV = 0, MS=0, CSLVL=1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3tC_{YCP}+30	-	ns
SCS↓→SUT delay time	t_{DSE}		-	40	-	40	ns
SCS↑→SUT delay time	t_{DEE}		0	-	0	-	ns

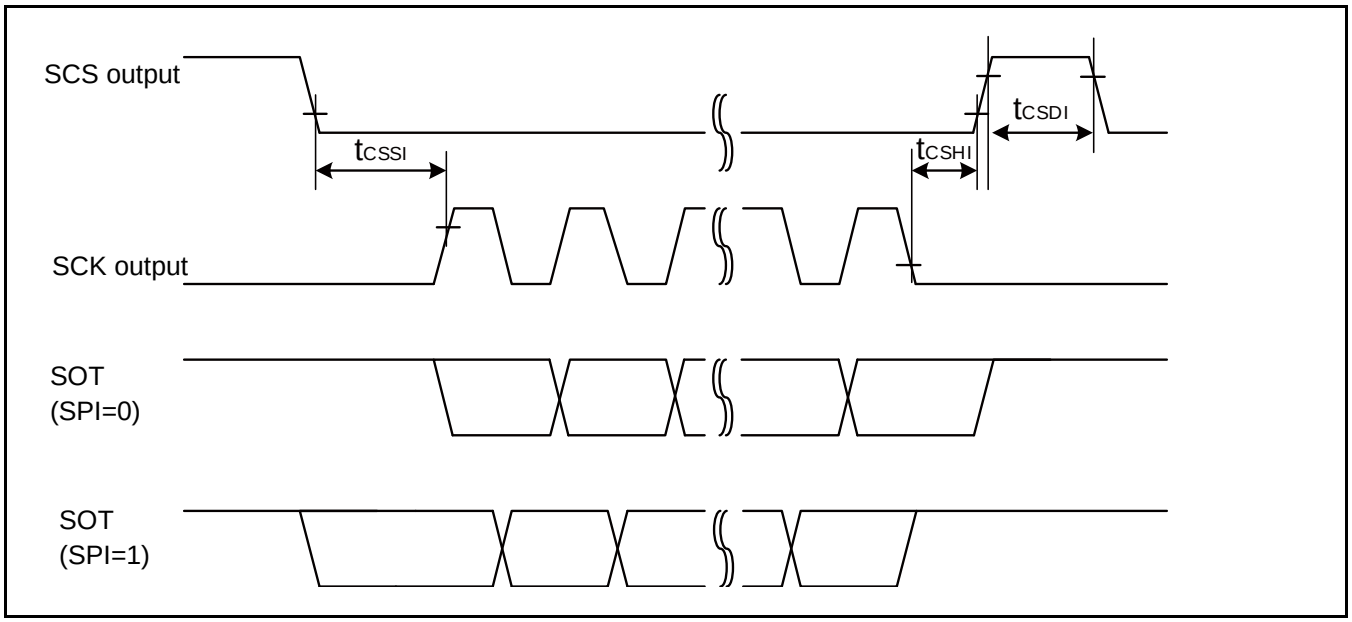
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

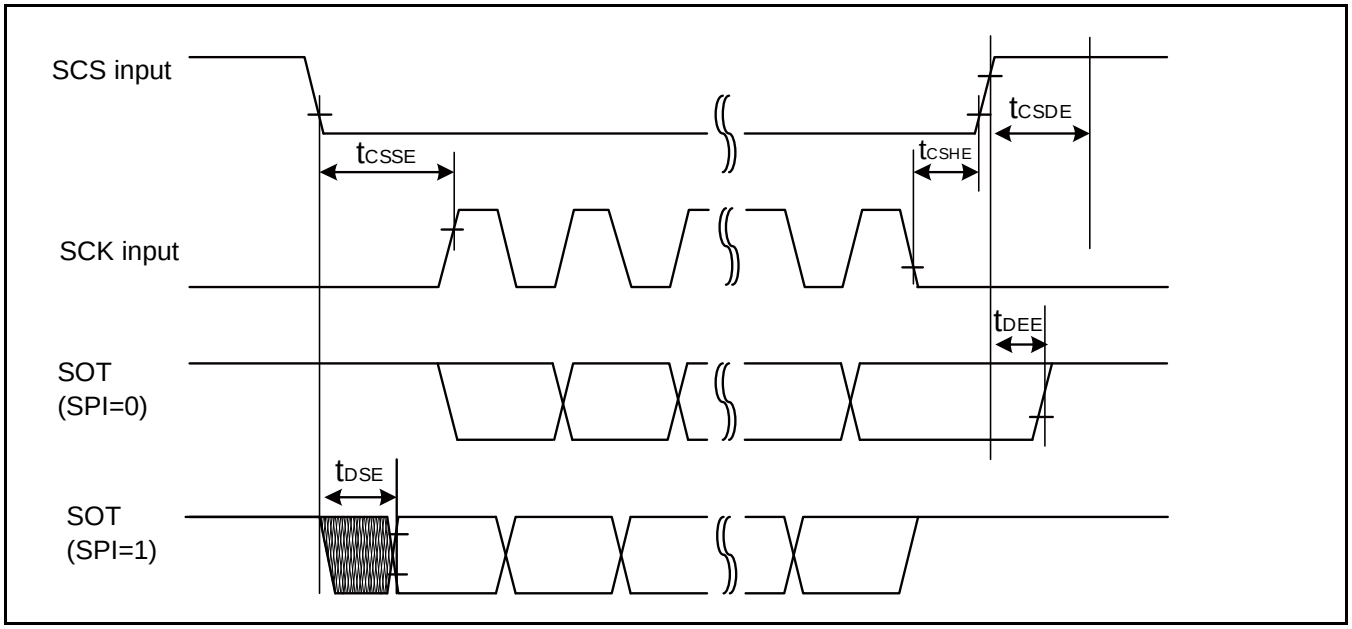
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part(MN709-00001).*
- *When the external load capacitance C_L = 30 pF.*


SCS output
tCSSI
tCSDI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSSE
tCSDE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

When Using Synchronous Serial Chip Select (SPI = 1, SCINV = 1, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

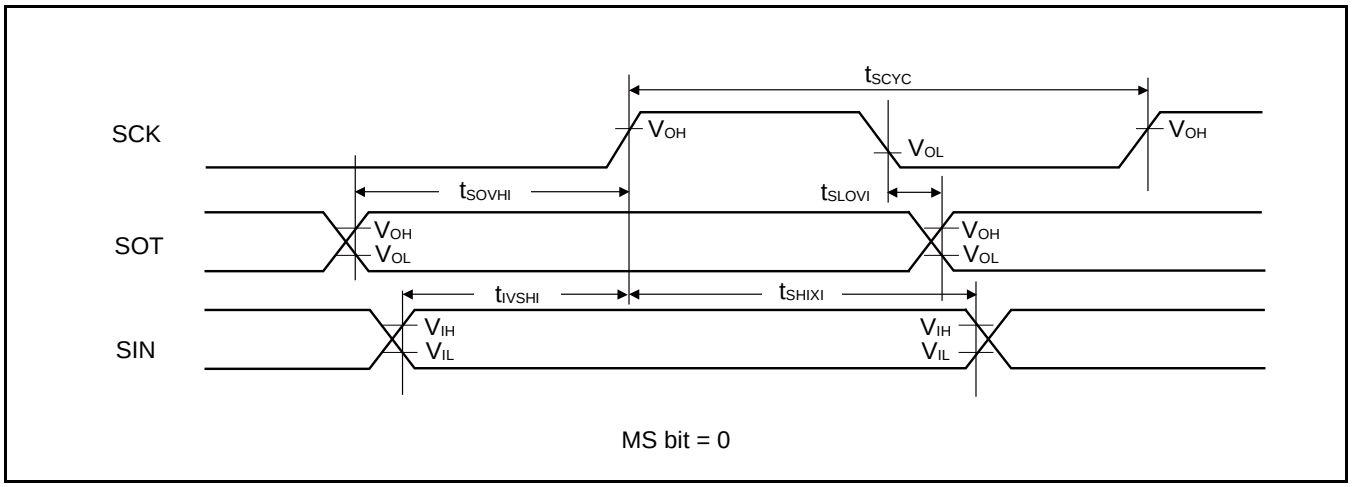
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

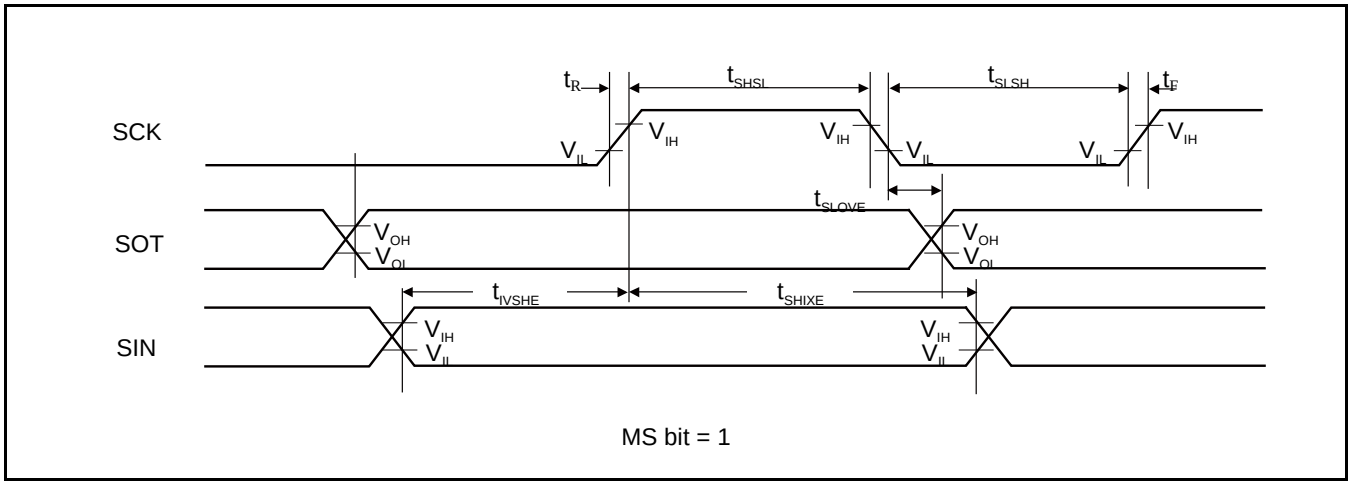
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

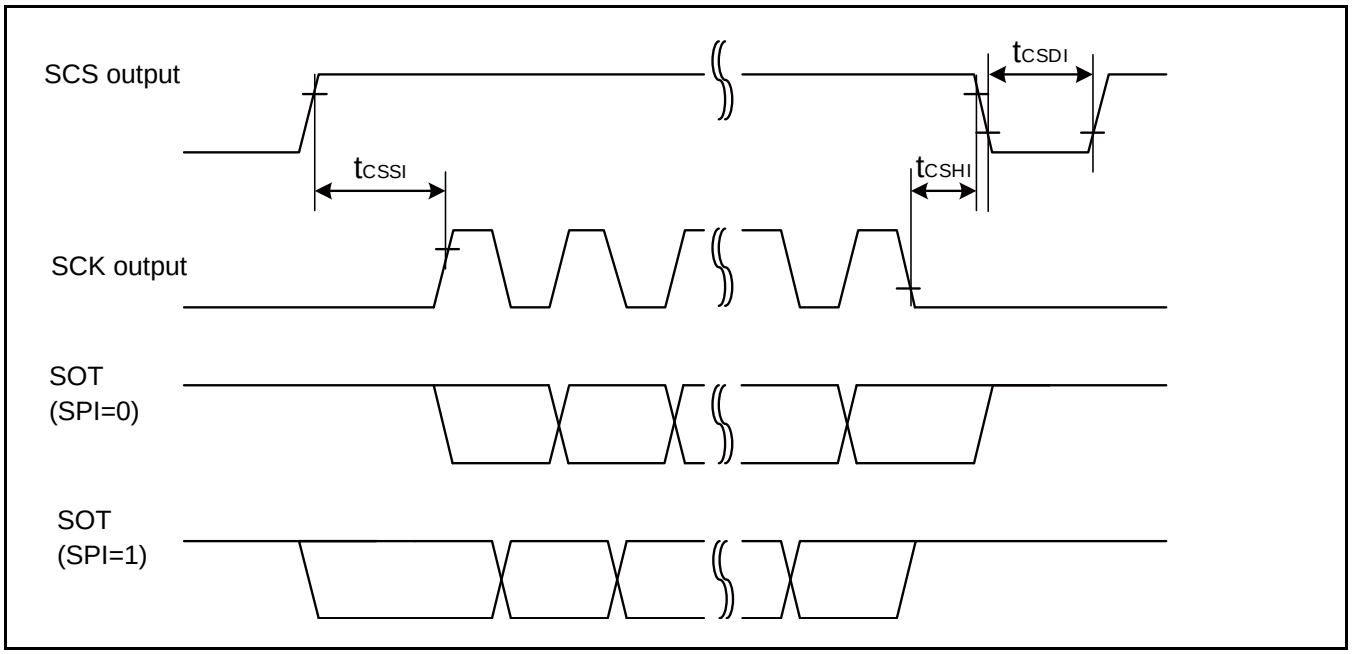
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part(MN709-00001).*
- *When the external load capacitance C_L = 30 pF.*

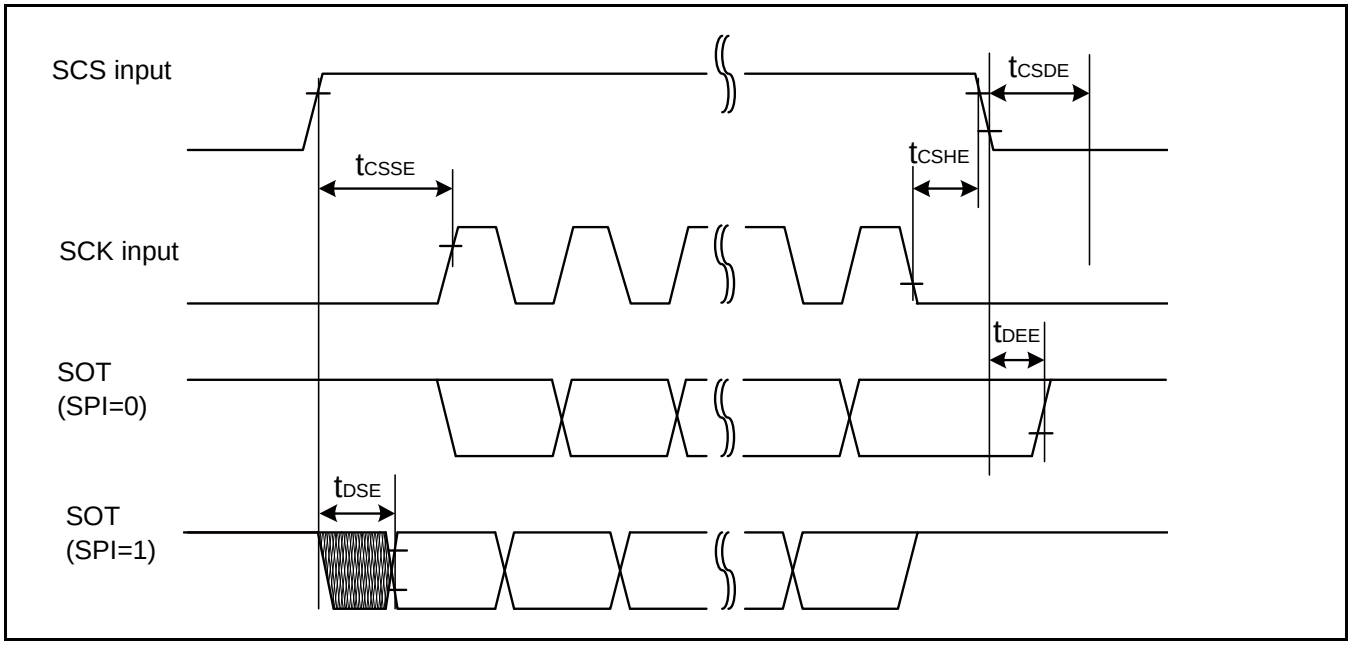


MS bit = 0



MS bit = 1

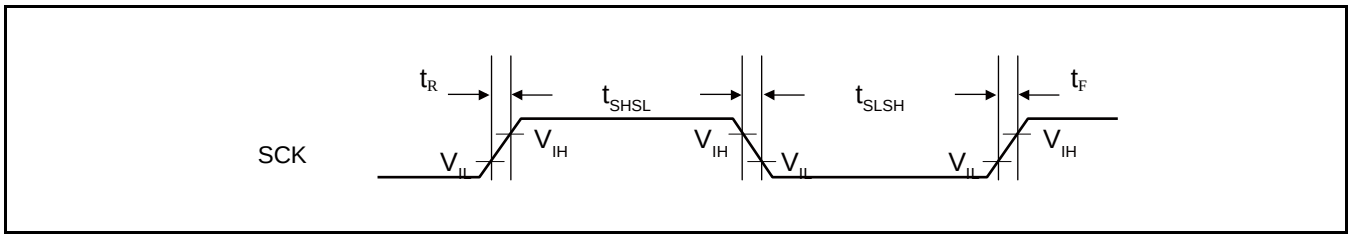

SCS output
tCSDI
tCSSI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSDE
tCSSE
tCSHE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

External Clock (EXT = 1): when in Asynchronous Mode Only

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



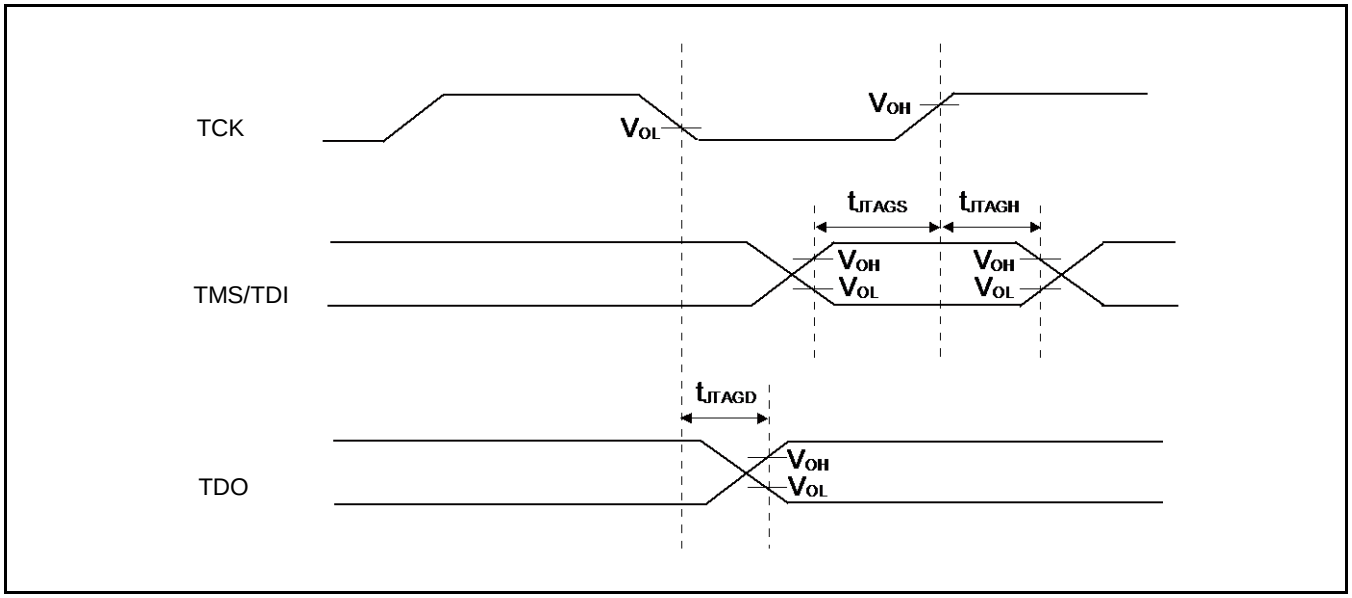
12.4.16 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	25	ns	
			$V_{CC} < 4.5$ V	-	45		

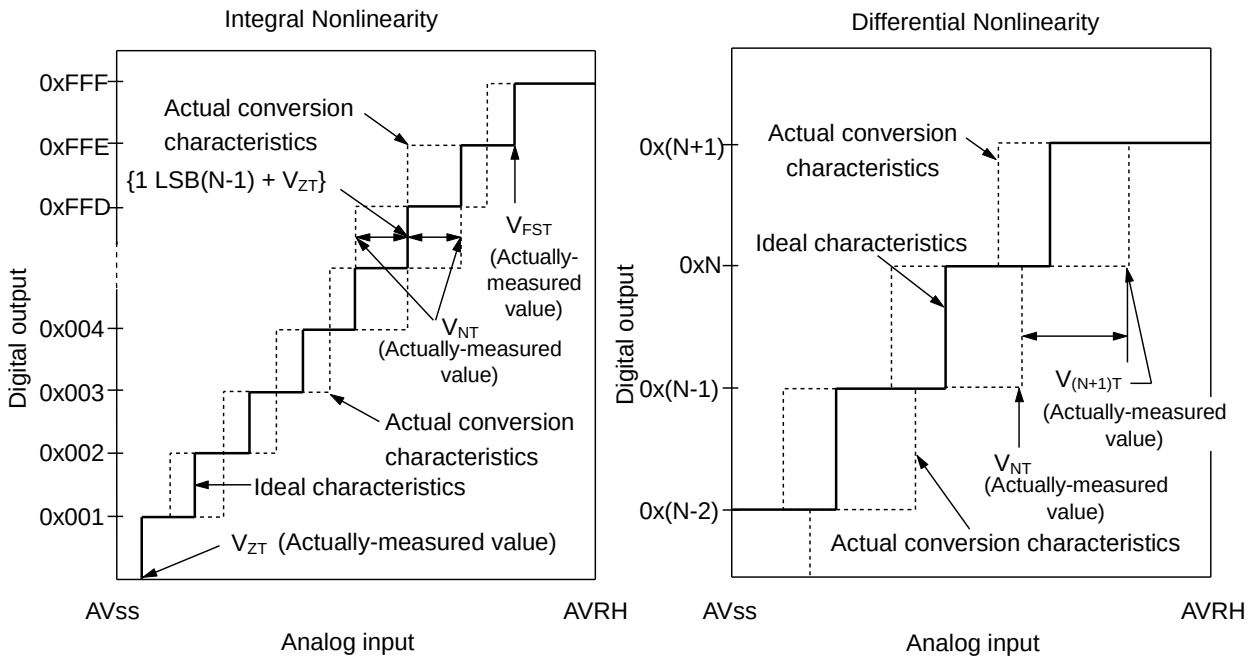
Note:

- *When the external load capacitance C_L= 30 pF.*



Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)}T - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.

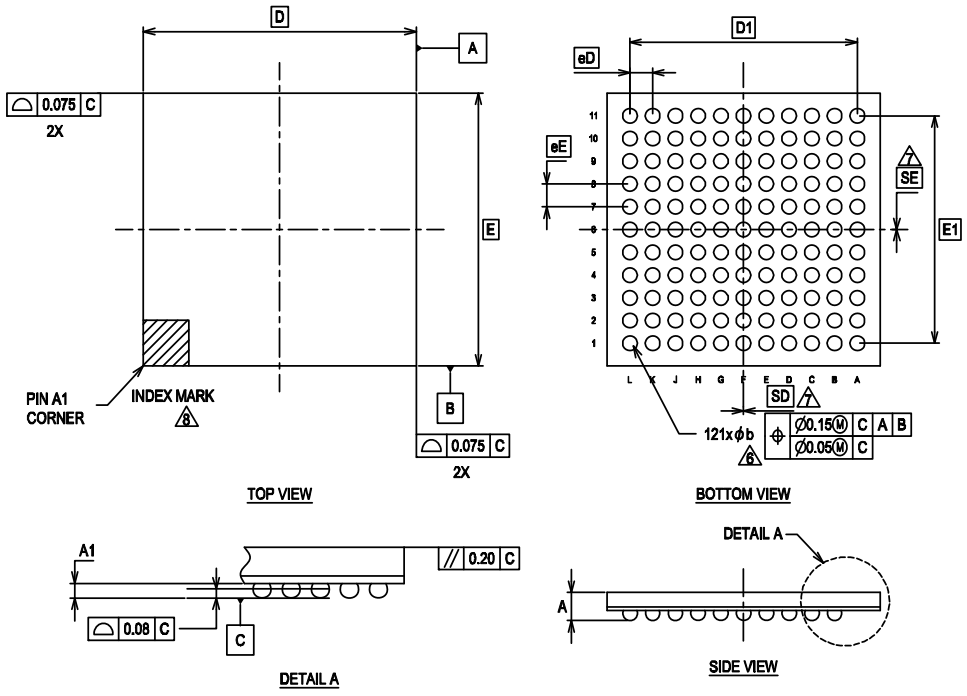
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.

V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

Package Type	Package Code
FBGA 121	FDI121

FDI121 121 ball Low Profile Fine Pitch Ball Grid Array Package



PACKAGE	FDI121			NOTE
SYMBOL	MIN.	NOM.	MAX.	
A	—	—	1.20	PROFILE
A_1	0.20	—	—	TERMINAL HEIGHT
D		6.00 BSC.		BODY SIZE
E		6.00 BSC.		BODY SIZE
D_1		5.00 BSC.		MATRIX FOOTPRINT
E_1		5.00 BSC.		MATRIX FOOTPRINT
MD		11		MATRIX SIZE D DIRECTION
ME		11		MATRIX SIZE E DIRECTION
n		121		BALL COUNT
ϕb	0.27	0.32	0.37	BALL DIAMETER
eD		0.50 BSC.		BALL PITCH
eE		0.50 BSC.		BALL PITCH
SD / SE		0.00		SOLDER BALL PLACEMENT

1. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009.
   THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

⚠6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

⚠7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE=0.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE=e/2

⚠8 A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

Rev. 0B