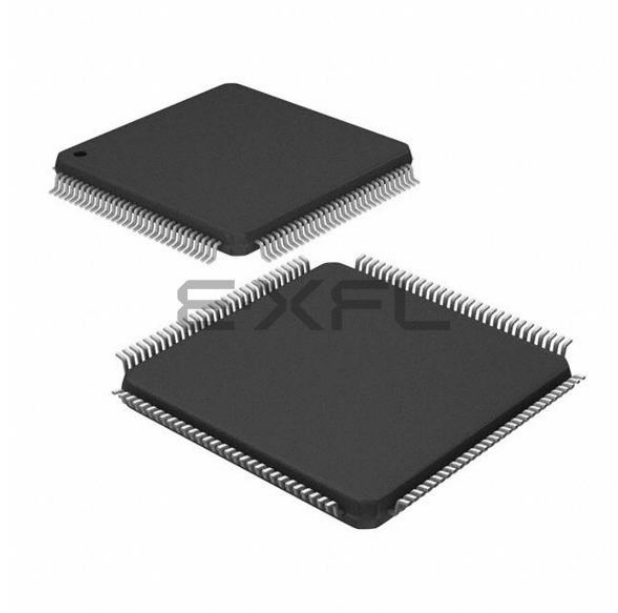


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2h44g0agv20000

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
20	15	-	G2	P36	E	K
				SIN5_2		
				IC02_0		
				INT09_1		
-			-	MADATA13_0		
20	-	-	G2	MNWEX_0		
21	16	-	G3	P37	E	K
				SOT5_2 (SDA5_2)		
				IC01_0		
				INT05_2		
-			-	MADATA14_0		
21	-	-	G3	MNREX_0		
22	17	-	G4	P38	E	K
				SCK5_2 (SCL5_2)		
				IC00_0		
				INT06_2		
-			-	MADATA15_0		
23	18	13	H1	P39	L	I
				ADTG_2		
				DTTI0X_0		
				RTCCO_2		
				SUBOUT_2		
		-		MSDCLK_0		
24	19	14	H2	P3A	G	I
				TIOA0_1		
				AIN0_0		
				RTO00_0 (PPG00_0)		
		-		MSDCKE_0		
25	20	15	H3	P3B	G	I
				TIOA1_1		
				BIN0_0		
				RTO01_0 (PPG00_0)		
		-		MRASX_0		
26	21	16	H4	P3C	G	I
				TIOA2_1		
				ZIN0_0		
				RTO02_0 (PPG02_0)		
		-		MCASX_0		
27	22	17	J1	P3D	G	I
				TIOA3_1		
				RTO03_0 (PPG02_0)		
				MAD00_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
28	23	18	J2	P3E TIOA4_1 RTO04_0 (PPG04_0) MAD01_0	G	I
29	24	19	K2	P3F TIOA5_1 RTO05_0 (PPG04_0) MAD02_0	G	I
30	25	20	L1	VSS	-	-
31	26	-	K1	VCC	-	-
32	27	-	L2	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	K
33	28	-	J3	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1 AIN2_0	G	K
34	29	-	J5	P42 TIOA2_0 RTO12_1 (PPG12_1) MSDWEX_0 BIN2_0	G	I
35	30	-	H5	P43 ADTG_7 TIOA3_0 RTO13_1 (PPG12_1) MCSX8_0 ZIN2_0	G	I
36	31	21	K3	P44 TIOA4_0 RTO14_1 (PPG14_1) DA0	R	J
37	32	22	J4	P45 TIOB0_0 RTO15_1 (PPG14_1) DA1	R	J
38	33	23	L3	INITX	B	C
39	34	24	L4	P46	P	S

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
52	-	-	H7	P71 TIOB4_2 BIN0_1 IC12_1 INT15_1 RX0_0	E	K
53	-	-	G7	P72 TIOA6_0 SIN2_0 ZIN0_1 IC11_1 INT14_2	E	K
54	-	-	H8	P73 TIOB6_0 SOT2_0 (SDA2_0) IC10_1 INT03_2	E	K
55	-	-	J9	P74 SCK2_0 (SCL2_0) DTTI1X_1	E	I
56	46	36	L8	PE0 MD1	C	E
57	47	37	K9	MD0	J	D
58	48	38	L9	PE2 X0	A	A
59	49	39	L10	PE3 X1	A	B
60	50	40	L11	VSS	-	-
61	51	-	K11	VCC	-	-
62	52	41	J10	P10 AN00 SIN1_1 FRCK0_2 INT02_1 MAD07_0 RX1_2	F	M
63	53	42	H10	P11 AN01 SOT1_1 (SDA1_1) IC00_2 MAD08_0 TX1_2	F	L

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
97	82	67	D7	P09	M	N
				AN19		
		-		TRACED0		
		67		TIOA3_2		
				SOT1_0 (SDA1_0)		
				MCSX5_0		
				IC23_1		
98	83	-	C7	P08	F	N
				AN20		
				TRACED1		
				TIOB3_2		
				SCK1_0 (SCL1_0)		
				MCSX4_0		
				IC22_1		
99	84	-	B7	P07	M	N
				AN21		
				TRACED2		
				TIOA0_2		
				SCK7_0 (SCL7_0)		
				MCLKOUT_0		
				IC21_1		
100	85	-	A7	P06	F	N
				AN22		
				TRACED3		
				TIOB0_2		
				SOT7_0 (SDA7_0)		
				MCSX3_0		
				IC20_1		
101	86	-	D6	P05	F	O
				AN23		
				ADTG_0		
				TRACECLK		
				SIN7_0		
				INT01_1		
				MCSX2_0		
				FRCK2_1		
102	87	68	B6	P04	E	G
				TDO		
				SWO		
103	88	69	C6	P03	E	G
				TMS		
				SWDIO		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
115	95	75	B3	P61 TIOB2_2 SOT5_0 (SDA5_0) RTCCO_0 SUBOUT_0 ZIN2_1	E	I
116	96	76	B2	P60 TIOA2_2 SCK5_0 (SCL5_0) NMIX WKUP0 MRDY_0 FRCK2_0	I	F
117	97	77	A4	VCC	-	-
118	98	78	A3	P80 BIN2_1 IC21_0	E *1	I
119	99	79	A2	P81 AIN2_1 IC20_0	E *1	I
120	100	80	A1	VSS	-	-
-	-	-	K10	VSS	-	-

*1 without pullup control register

7. Handling Devices

Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each POWER pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS near this device.

Power Supply Pins

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1 V/µs at a momentary fluctuation such as switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption.
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  - Size: More than 3.2 mm × 1.5 mm
  - Load capacitance: Approximately 6 pF to 7 pF
- Lead type
  - Load capacitance: Approximately 6 pF to 7 pF

Current Explanation Diagram

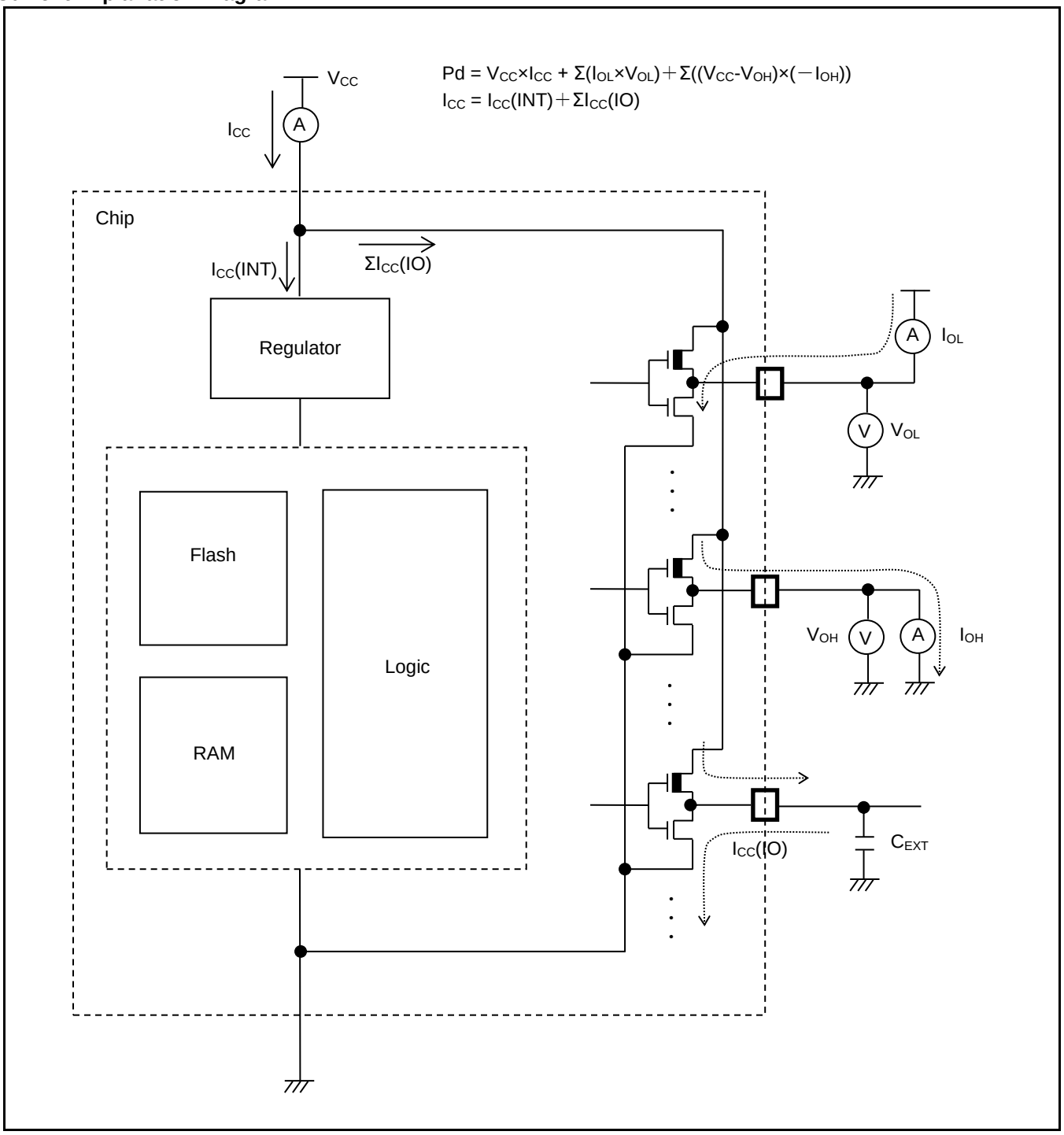


Table 12-6 Typical and Maximum Current Consumption in Sleep Operation(PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency*5	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation *6 (PLL)	72 MHz	23	43	mA	*3 When all peripheral clocks are ON
				60 MHz	19	39		
				48 MHz	16	36		
				36 MHz	12	32		
				24 MHz	8.5	29		
				12 MHz	5.1	25		
				8 MHz	3.9	24		
				4 MHz	2.7	23		
				72 MHz	8.8	29	mA	*3 When all peripheral clocks are OFF
				60 MHz	7.6	28		
				48 MHz	6.3	27		
				36 MHz	5.1	25		
				24 MHz	3.9	24		
				12 MHz	2.7	23		
				8 MHz	2.3	23		
				4 MHz	1.9	22		

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

*6: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-9 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode and VBAT

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCHD}	VCC	Deep standby Stop mode (When RAM is OFF)	-	24	40	µA	*3, *4 T_A=+25°C
					-	640	µA	*3, *4 T_A=+85°C
					-	813	µA	*3, *4 T_A=+105°C
			Deep standby Stop mode (When RAM is ON)		41	146	µA	*3, *4 T_A=+25°C
					-	1616	µA	*3, *4 T_A=+85°C
					-	2059	µA	*3, *4 T_A=+105°C
	I_{CCRD}		Deep standby RTC mode (When RAM is OFF)	32kHz	24	40	µA	*3, *4 T_A=+25°C
					-	640	µA	*3, *4 T_A=+85°C
					-	813	µA	*3, *4 T_A=+105°C
			Deep standby RTC mode (When RAM is ON)		41	146	µA	*3, *4 T_A=+25°C
					-	1616	µA	*3, *4 T_A=+85°C
					-	2059	µA	*3, *4 T_A=+105°C
	I_{CCVBAT}	VBAT	RTC stop	-	0.015	0.14	µA	*3, *4, *5 T_A=+25°C
					-	4.0	µA	*3, *4, *5 T_A=+85°C
					-	9.4	µA	*3, *4, *5 T_A=+105°C
			RTC operation *6		1.3	2.4	µA	*3, *4 T_A=+25°C
					-	6.2	µA	*3, *4 T_A=+85°C
					-	12	µA	*3, *4 T_A=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=5.5 V

*3: When all ports are fixed.

*4: When LVD is OFF

*5: When sub oscillation is OFF

*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

Table 12-10 Typical and Maximum Current Consumption in Low-voltage Detection Circuit, Main Flash Memory Write/erase

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	-	4	7	µA	For occurrence of interrupt
Main flash memory write/erase current	$I_{CCFLASH}$		At Write/Erase	-	13.4	15.9	mA	
Work flash memory write/erase current	$I_{CCWFLASH}$		At Write/Erase	-	11.5	13.6	mA	*1

1: When programming or erase in flash memory, Flash Memory Write/Erase current ($I_{CCFLASH}$) is added to the Power supply current (I_{CC}).

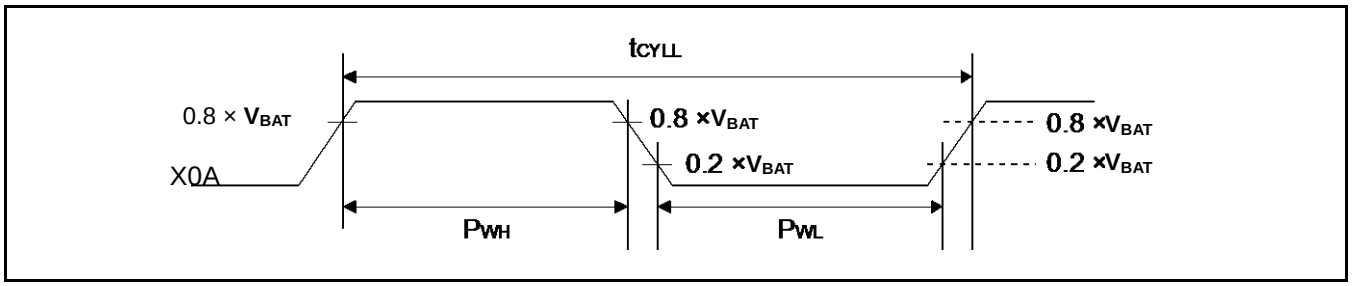
Table 12-11 Peripheral Current Dissipation

Clock System	Peripheral	Unit	Frequency (MHz)			Unit	Remarks
			40	80	160		
HCLK	GPIO	All ports	0.16	0.32	0.62	mA	T_A=+25°C, V_{CC}=3.3 V
	DMAC	-	0.68	1.35	2.63		
	DSTC	-	0.93	1.88	3.65		
	External bus I/F	-	0.17	0.34	0.71		
	CAN	1ch.	0.01	0.02	0.03		
PCLK1	Base timer	4ch.	0.18	0.37	0.73	mA	T_A=+25°C, V_{CC}=3.3 V
	Multi-functional timer/PPG	1unit/4ch.	0.61	1.22	2.43		
	Quadrature position/Revolution counter	1unit	0.04	0.07	0.14		
	A/DC	1unit	0.22	0.44	0.88		
PCLK2	Muli-function serial	1ch.	0.30	0.60	-	mA	T_A=+25°C, V_{CC}=3.3 V

12.4.2 Sub Clock Input Characteristics

(V_{BAT} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	1/ t_{CYLL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



12.4.3 Built-in CR Oscillation Characteristics

Built-in High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_J = -20°C to + 105°C	3.92	4	4.08	MHz	When trimming*1
		T_J = - 40°C to + 125°C	3.88	4	4.12		
Clock frequency	f_{CRH}	T_J = - 40°C to + 125°C	2.9	4	5		When not trimming
Frequency Stabilization time	t_{CRWT}	-	-	-	30	µs	*2

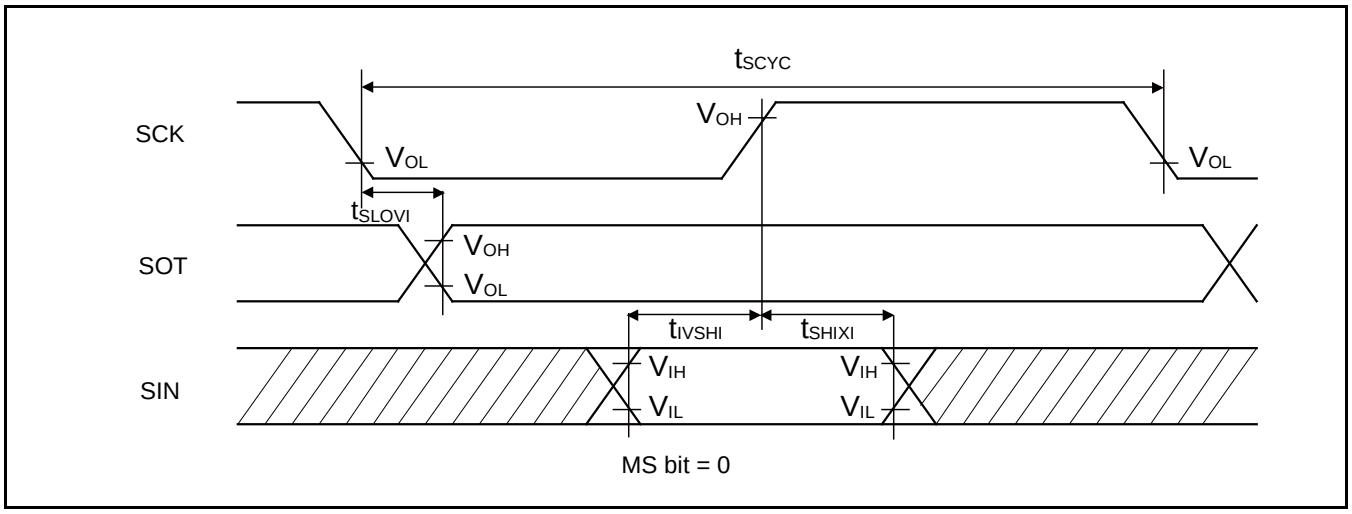
*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency/temperature trimming.

*2: This is the time to stabilize the frequency of high-speed CR clock after setting trimming value. This period is able to use high-speed CR clock as source clock.

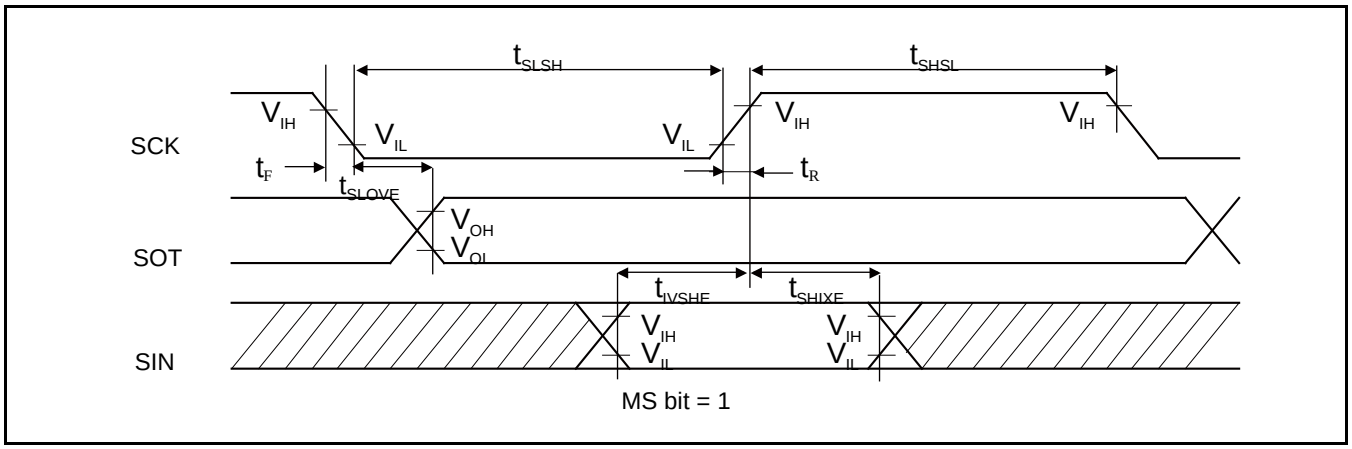
Built-in Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

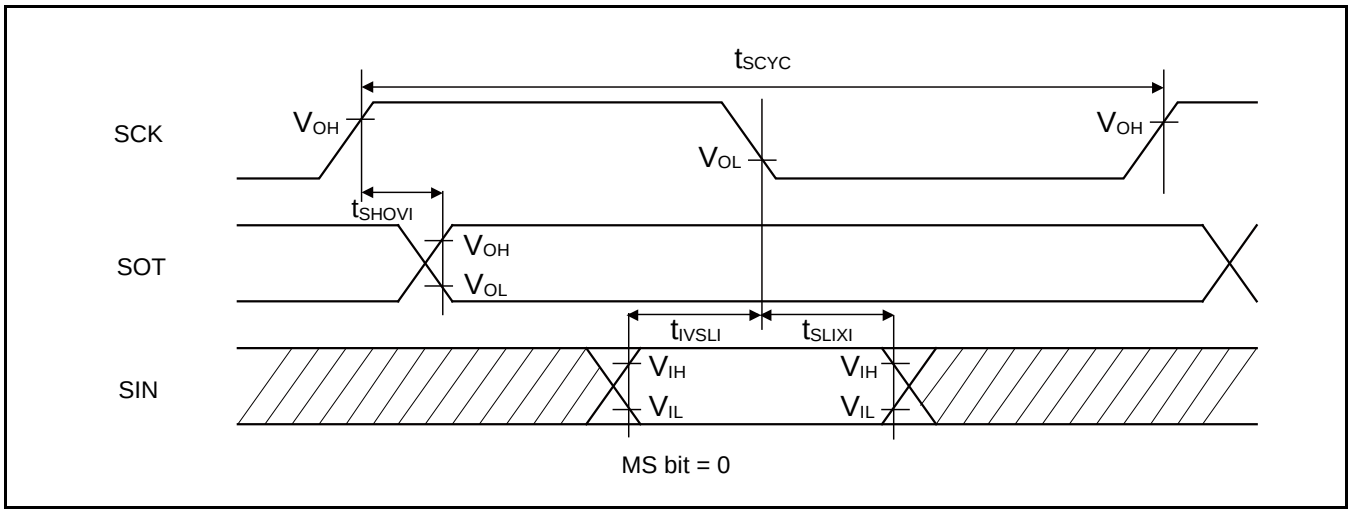
Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	



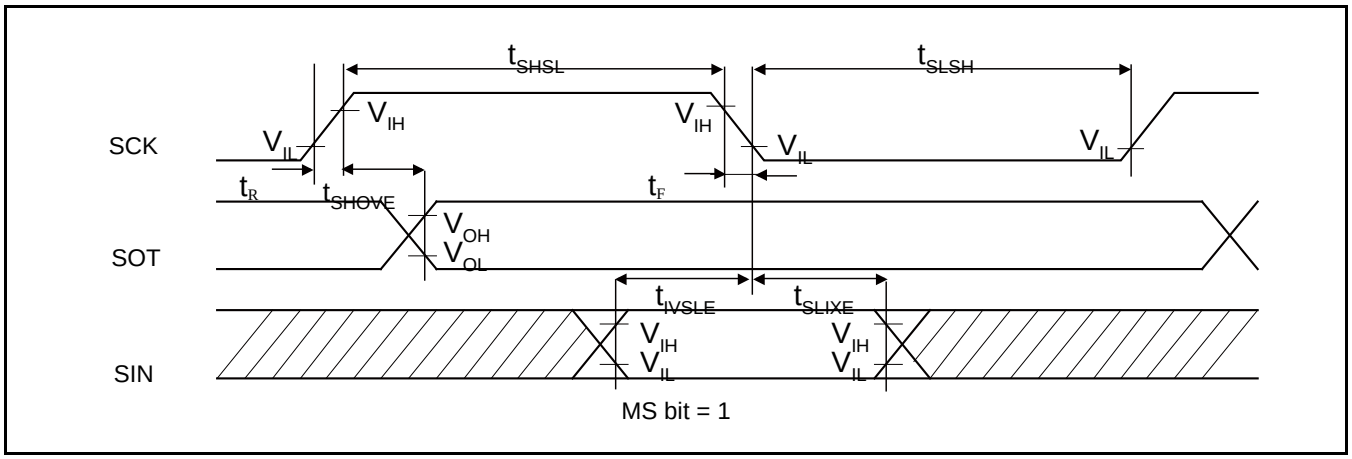
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*

When Using High-speed Synchronous Serial Chip Select (SPI = 1, SCINV = 1, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

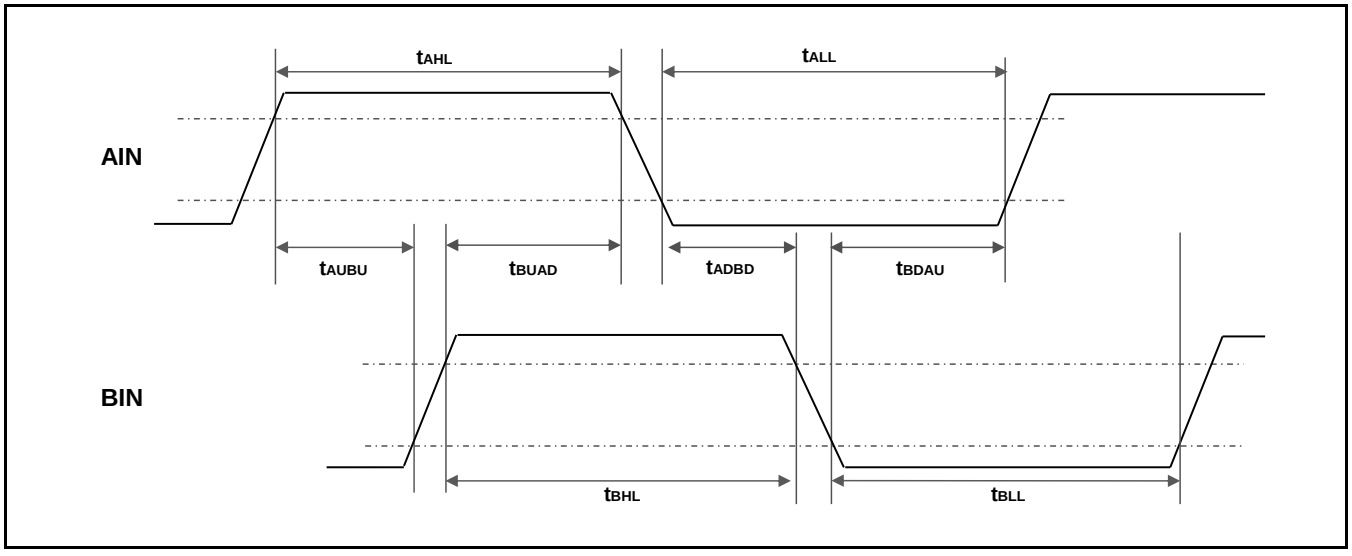
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part(MN709-00001).*
- *When the external load capacitance C_L = 30 pF.*

12.4.13 Quadrature Position/Revolution Counter Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rising time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC="0"			
ZIN pin L width	t_{ZLL}	QCR:CGSC="0"			
AIN/BIN rising and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC="1"			
Determined ZIN level from AIN/BIN rising and falling time	t_{ABEZ}	QCR:CGSC="1"			

*: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see "8. Block Diagram" in this data sheet.



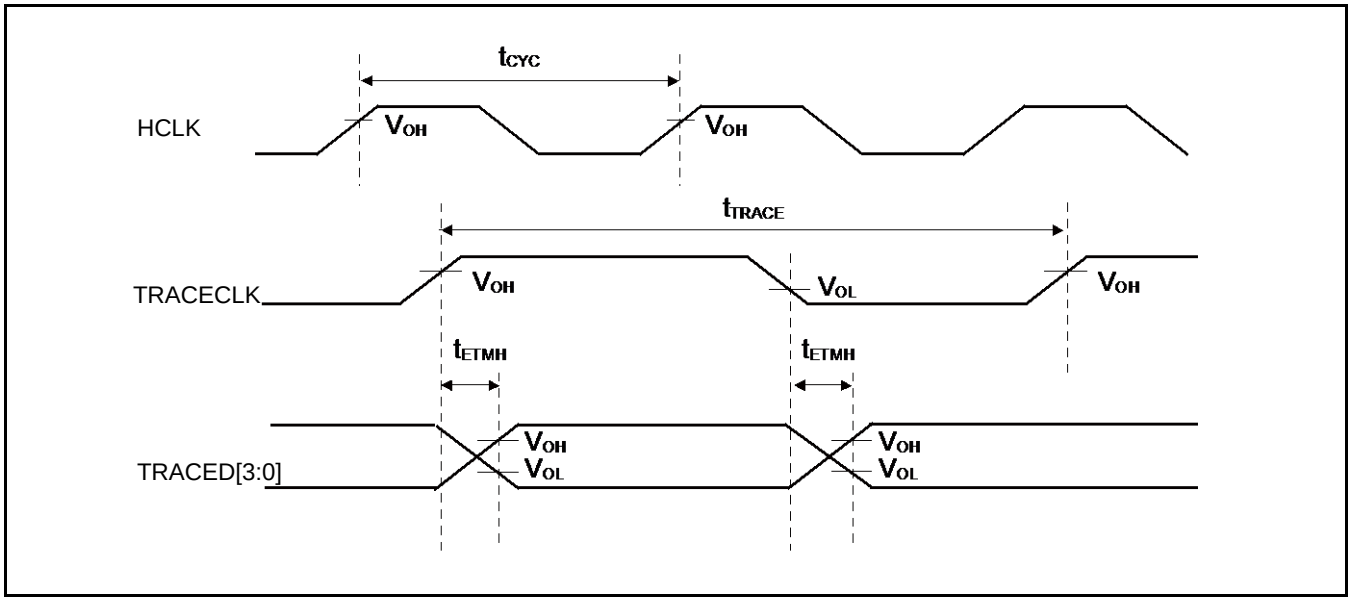
12.4.15 ETM Timing

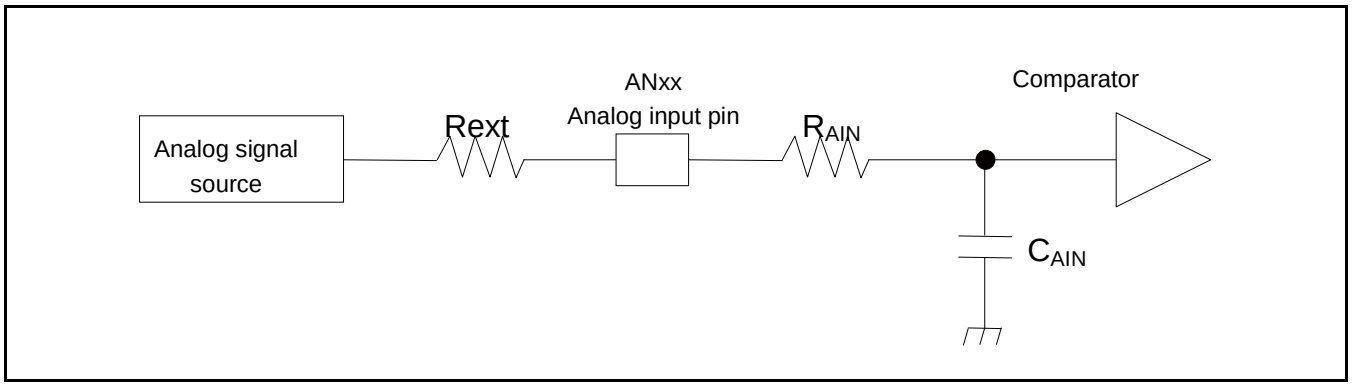
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[3:0]	$V_{CC} \geq 4.5$ V	2	9	ns	
			$V_{CC} < 4.5$ V	2	15		
TRACECLK frequency	1/ t_{TRACE}	TRACECLK	$V_{CC} \geq 4.5$ V	-	50	MHz	
			$V_{CC} < 4.5$ V	-	32	MHz	
TRACECLK clock cycle	t_{TRACE}		$V_{CC} \geq 4.5$ V	20	-	ns	
			$V_{CC} < 4.5$ V	31.25	-	ns	

Note:

- *When the external load capacitance C_L= 30 pF.*





(Equation 1) $t_S \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

t_S:	Sampling time
R_{AIN}:	Input resistance of A/D = 1.2 kΩ at 4.5 V < AV_{CC} < 5.5 V
	Input resistance of A/D = 1.8 kΩ at 2.7 V < AV_{CC} < 4.5 V
C_{AIN}:	Input capacity of A/D = 12.05 pF at 2.7 V < AV_{CC} < 5.5 V
Rext:	Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

t_C:	Compare time
t_{CCK}:	Compare clock cycle

Document History

Document Title: S6E2H4 Series 32-bit ARM® Cortex®-M4F, FM4 Microcontroller
Document Number: 001-98941

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4869576	YUIA	08/18/2015	New Spec.
*A	4932844	YUIA	10/02/2015	Changed status from Preliminary to Final. Updated 12.2 Recommended Operating Conditions: Added the "Smoothing capacitor (C_S)". Added the “Current Value” in “Maximum leak current at operating”. Updated 12.3.1 Current Rating: Updated Table 12-1 ~ 12-9: Added the “MAX” value. Updated Table 12-11: Added voltage and temperature information. Updated 12.10.1 Recovery Cause: Interrupt/WKUP: Updated Recovery Count Time. Updated 12.10.2 Recovery Cause: Reset: Updated Recovery Count Time.
*B	5027946	YUIA	11/26/2015	Updated 2 Packages: Changed FBGA to“Supported” from “Under development”. Updated 4 Pin Description: Added “Note” about TAP pins. Updated 12.5 12-bit A/D Converter: Updated “Zero transition” and “Full-scale transition” value. Added “Total error”.