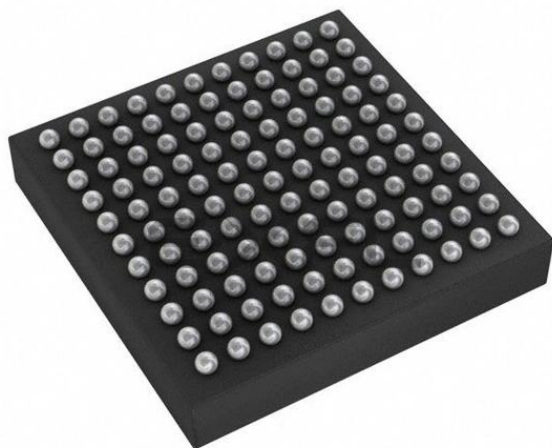




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, CSIO, EBI/EMI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-FBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2h46g0agb3000a

- Various error detect functions available (parity errors, framing errors, and overrun errors)

■ CSIO

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detect function available
- Serial chip select function (ch.6 and ch.7 only)
- Supports high-speed SPI (ch.4 and ch.6 only)
- Data length 5 to 16-bit

■ LIN

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can change to 13 to 16-bit length)
- LIN break delimiter generation (can change to 1 to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

■ I²C

- Standard mode (Max 100 kbps) / High-speed mode (Max 400 kbps) supported
- Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3=ch.A and ch.7=ch.B) supported

DMA Controller (8 channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller) (256 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor which has already been constructed on the memory, can access directly the memory /peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation and the chain activation functions.

A/D Converter (Max 24 channels)
[12-bit A/D Converter]

- Successive Approximation type
- Built-in 3 units
- Conversion time: 0.5 μ s @ 5 V

- Priority conversion available (priority at 2 levels)

- Scanning conversion mode

- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

DA Converter (Max 2 channels)

- R-2R type
- 12-bit resolution

Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer
- Event counter mode (external clock mode)

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 100 high-speed general-purpose I/O ports @ 120 pin Package
- Some pin is 5 V tolerant I/O.
See 4. Pin Description and 5. I/O Circuit Type for the corresponding pins.

Multi-function Timer (Max 3 units)

The Multi-function timer is composed of the following blocks.

Minimum resolution: 6.25 ns

- 16-bit free-run timer $\times$ 3ch./unit
- Input capture $\times$ 4ch./unit
- Output compare $\times$ 6ch./unit
- A/D activation compare $\times$ 6ch./unit
- Waveform generator $\times$ 3ch./unit
- 16-bit PPG timer $\times$ 3ch./unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function



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4. Pin Description

List of Pin Numbers

The number after the underscore (" _") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

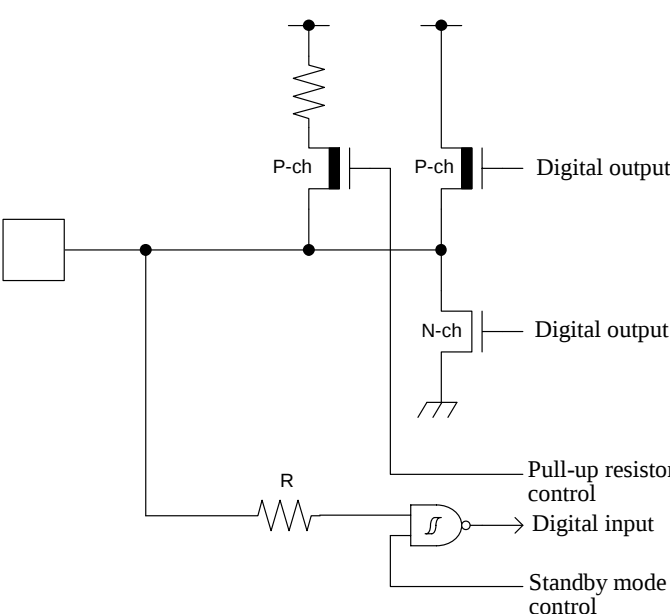
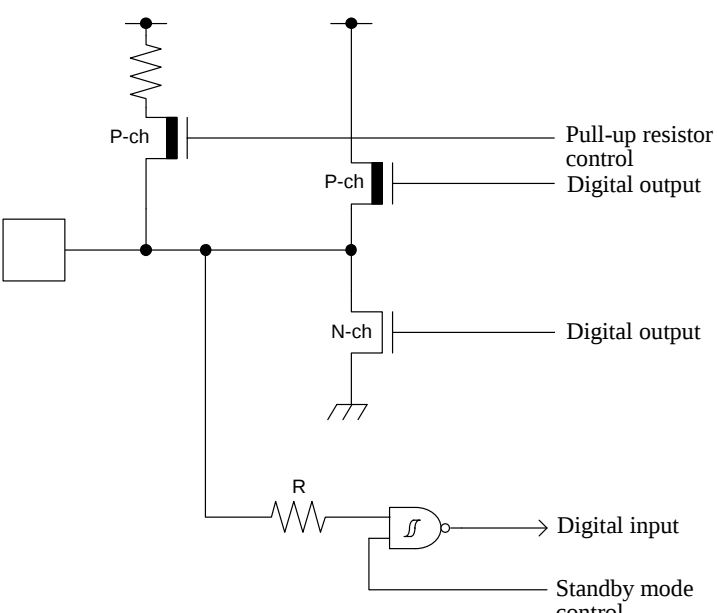
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
1	1	1	B1	VCC	-	-
2	2	2	C1	P50	E	K
				CTS4_0		
				AIN0_2		
				RTO10_0 (PPG10_0)		
				INT00_0		
				MADATA00_0		
3	3	3	C2	P51	E	K
				RTS4_0		
				BIN0_2		
				RTO11_0 (PPG10_0)		
				INT01_0		
				MADATA01_0		
4	4	4	D1	P52	E	I
				SCK4_0 (SCL4_0)		
				ZIN0_2		
				RTO12_0 (PPG12_0)		
				MADATA02_0		
5	5	5	D2	P53	E	I
				TIOA1_2		
				SOT4_0 (SDA4_0)		
				RTO13_0 (PPG12_0)		
				MADATA03_0		
6	6	6	D3	P54	E	K
				TIOB1_2		
				SIN4_0		
				RTO14_0 (PPG14_0)		
				INT02_0		
				MADATA04_0		

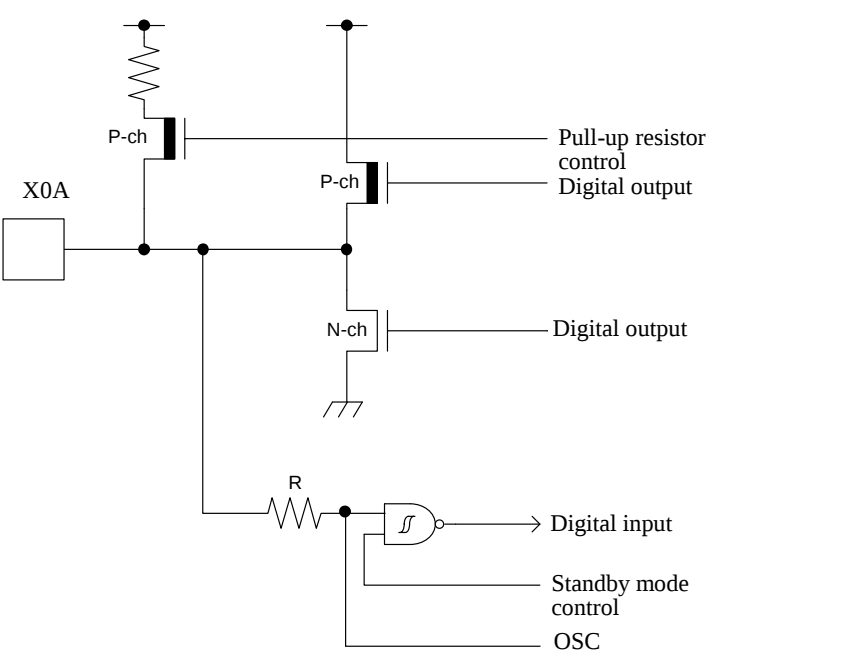
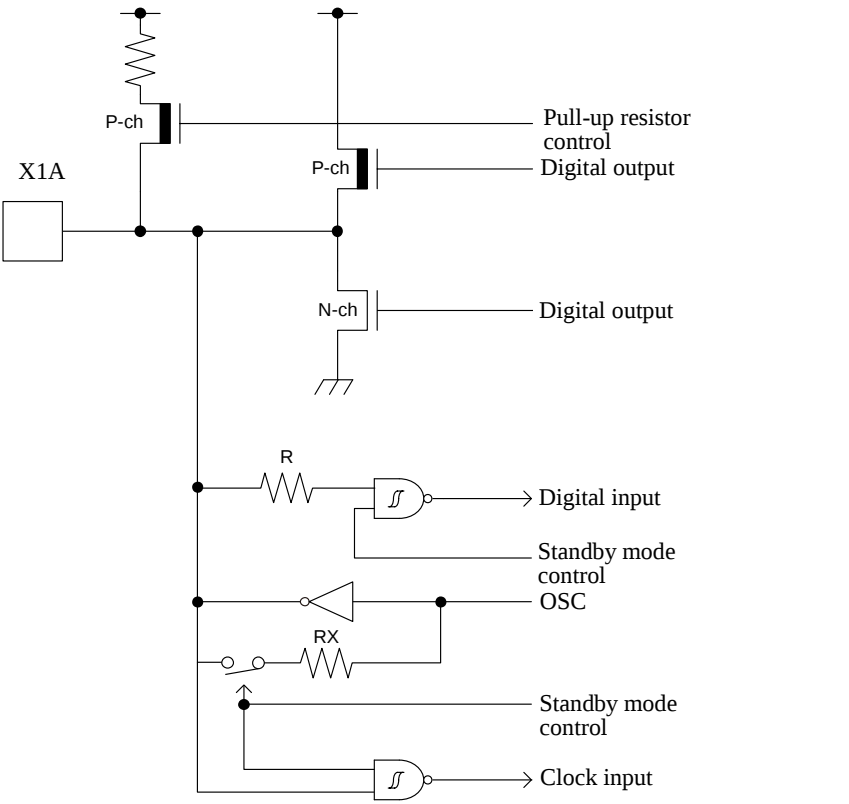
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
89	74	-	B11	P20	F	M
				AN18		
				AIN1_1		
				INT05_0		
				MAD24_0		
				RTO25_0		
90	75	60	A11	VSS	-	-
91	76	61	A10	VCC	-	-
92	77	62	B9	P0E	L	I
				TIOB5_2		
				SCS6_1		
				IC13_0		
				MDQM1_0		
93	78	63	A9	P0D	L	I
				TIOA5_2		
				SCK6_1 (SCL6_1)		
				IC12_0		
				MDQM0_0		
94	79	64	C8	P0C	L	I
				TIOA6_1		
				SOT6_1 (SDA6_1)		
				IC11_0		
				MALE_0		
95	80	65	B8	P0B	L	K
				TIOB6_1		
				SIN6_1		
				IC10_0		
				INT00_1		
				MCSX0_0		
96	81	66	A8	P0A	L	K
				SIN1_0		
				FRCK1_0		
				INT12_2		
				MCSX1_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
104	89	70	C5	P02	E	H
				TDI		
				MCSX6_0		
105	90	71	B5	P01	E	G
				TCK		
				SWCLK		
106	91	72	A5	P00	E	H
				TRSTX		
				MCSX7_0		
107	92	-	A6	VSS	-	-
108	-	-	E6	P68	E	K
				TIOB7_2		
				SCK3_0 (SCL3_0)		
				INT00_2		
109	-	-	E5	P67	E	I
				TIOA7_2		
				SOT3_0 (SDA3_0)		
110	-	-	D5	P66	E	K
				ADTG_8		
				SIN3_0		
				INT11_2		
111	-	-	D4	P65	E	I
				TIOB7_0		
				SCK5_1 (SCL5_1)		
112	-	-	C4	P64	E	K
				TIOA7_0		
				SOT5_1 (SDA5_1)		
				INT10_2		
113	93	73	B4	P63	E	K
	-	-		CROUT_1		
	93	73		SIN5_1		
				INT03_0		
				MWEX_0		
				IC23_0		
				RX0_2		
114	94	74	C3	P62	I	K
				ADTG_3		
				SIN5_0		
				INT04_1		
				MOEX_0		
				IC22_0		
				TX0_2		

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
External Bus	MCSX0_0	External bus interface chip select output pin	95	80	65	B8
	MCSX1_0		96	81	66	A8
	MCSX2_0		101	86	-	D6
	MCSX3_0		100	85	-	A7
	MCSX4_0		98	83	-	C7
	MCSX5_0		97	82	67	D7
	MCSX6_0		104	89	70	C5
	MCSX7_0		106	91	72	A5
	MCSX8_0		35	30	-	H5
	MADATA00_0	External bus interface data bus (Address / data multiplex bus)	2	2	2	C1
	MADATA01_0		3	3	3	C2
	MADATA02_0		4	4	4	D1
	MADATA03_0		5	5	5	D2
	MADATA04_0		6	6	6	D3
	MADATA05_0		7	7	7	E2
	MADATA06_0		8	8	8	E3
	MADATA07_0		9	9	9	E4
	MADATA08_0		10	10	10	F5
	MADATA09_0		11	11	11	F6
	MADATA10_0		12	12	12	G5
	MADATA11_0		13	13	-	G6
	MADATA12_0		14	14	-	E1
	MADATA13_0		15	15	-	F4
	MADATA14_0		16	16	-	F3
	MADATA15_0		17	17	-	F2
	MDQM0_0	External bus interface byte mask signal output pin	93	78	63	A9
	MDQM1_0		92	77	62	B9
	MALE_0	External bus interface Address Latch enable output signal for multiplex	94	79	64	C8
	MRDY_0	External bus interface external RDY input signal	116	96	76	B2
	MCLKOUT_0	External bus interface external clock output pin	99	84	-	B7
	MNALE_0	External bus interface ALE signal to control NAND Flash output pin	18	-	-	F1
	MNCLE_0	External bus interface CLE signal to control NAND Flash output pin	19	-	-	G1
	MNREX_0	External bus interface read enable signal to control NAND Flash	21	-	-	G3
	MNWEX_0	External bus interface write enable signal to control NAND Flash	20	-	-	G2
	MOEX_0	External bus interface read enable signal for SRAM	114	94	74	C3
	MWEX_0	External bus interface write enable signal for SRAM	113	93	73	B4

Pin Function	Pin Name	Function Description	Pin No			
			LQFP 120	LQFP 100	LQFP 80	FBGA 121
External Interrupt	NMIX	Non-Maskable Interrupt input pin	116	96	76	B2
GPIO	P00	General-purpose I/O port 0	106	91	72	A5
	P01		105	90	71	B5
	P02		104	89	70	C5
	P03		103	88	69	C6
	P04		102	87	68	B6
	P05		101	86	-	D6
	P06		100	85	-	A7
	P07		99	84	-	B7
	P08		98	83	-	C7
	P09		97	82	67	D7
	P0A		96	81	66	A8
	P0B		95	80	65	B8
	P0C		94	79	64	C8
	P0D		93	78	63	A9
	P0E		92	77	62	B9
	P10	General-purpose I/O port 1	62	52	41	J10
	P11		63	53	42	H10
	P12		64	54	43	H9
	P13		65	55	44	G10
	P14		66	56	45	G9
	P15		67	57	46	G8
	P16		68	58	47	F10
	P17		69	59	48	F9
	P18		74	64	53	F8
	P19		75	65	54	E11
	P1A		76	66	55	E10
	P1B		77	67	56	E9
	P1C		78	68	-	E8
	P1D		79	69	-	D10
	P1E		80	70	-	D9
	P1F		81	-	-	F7
	P20	General-purpose I/O port 2	89	74	-	B11
	P21		88	73	59	C11
	P22		87	72	58	C10
	P23		86	71	57	D11
	P24		85	-	-	B10
	P25		84	-	-	C9
	P26		83	-	-	D8
	P27		82	-	-	E7

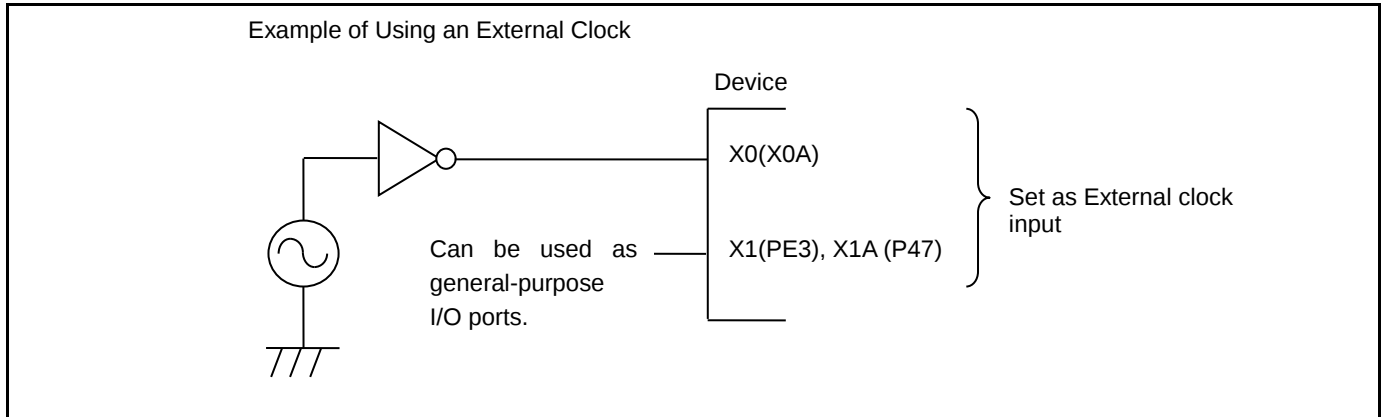
Type	Circuit	Remarks
N		- CMOS level output - CMOS level hysteresis input - With pull-up resistor control - With standby mode control - Pull-up resistor : Approximately 50 kΩ $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ (GPIO) $I_{OL} = 20 \text{ mA}$ (Fast Mode Plus) - When this pin is used as an I²C pin, the digital output P-ch transistor is always off.
O		- CMOS level output - CMOS level hysteresis input 5 V tolerant - With pull-up resistor control - With standby mode control - Pull-up resistor : Approximately 50 kΩ $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ - For I/O setting, refer to VBAT Domain in the Peripheral Manual

Type	Circuit	Remarks
P	 Pull-up resistor control Digital output Digital output Digital input Standby mode control OSC	- CMOS level output - CMOS level hysteresis input - With pull-up resistor control - With standby mode control - Pull-up resistor : Approximately 50 kΩ $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ - For I/O setting, refer to VBAT Domain in the Peripheral Manual
Q	 Pull-up resistor control Digital output Digital output Digital input Standby mode control OSC Standby mode control Clock input	It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. - Oscillation feedback resistor : Approximately 10 MΩ - With Standby mode control When the GPIO is selected. - CMOS level output. - CMOS level hysteresis input - With pull-up resistor control - With standby mode control - Pull-up resistor : Approximately 50 kΩ $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ - For I/O setting, refer to VBAT Domain in the Peripheral Manual

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.

Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.



Handling when Using Multi-function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled.

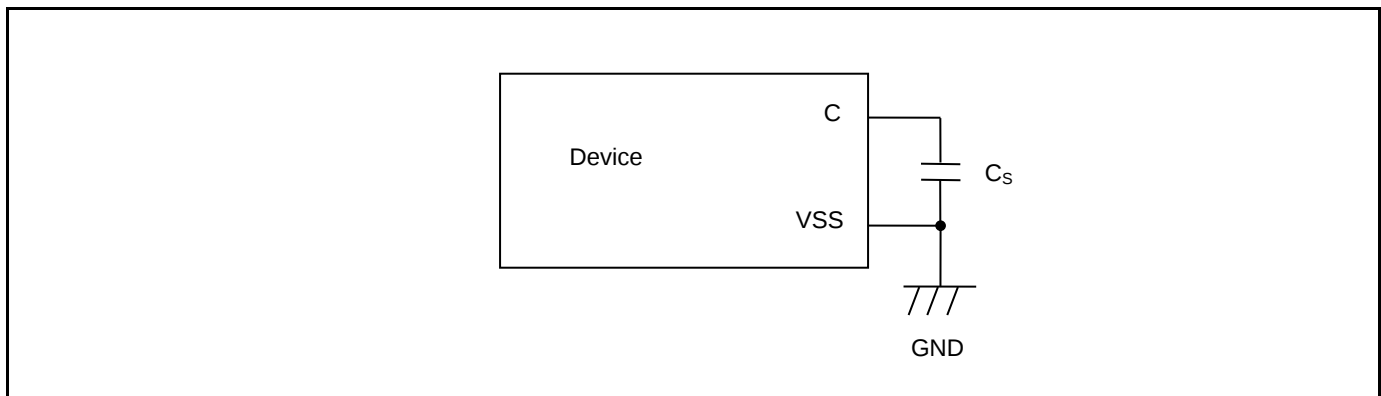
However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.

However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.

A smoothing capacitor of about 4.7 μ F would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4002_2FFF		Multi-function timer unit2
0x4002_3000	0x4003_FFFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_4FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A Converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low Voltage Detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		CAN prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		RTC/Port Ctrl
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_2FFF		CAN ch.0
0x4006_3000	0x4006_3FFF		CAN ch.1
0x4006_4000	0x4006_EFFF		Reserved
0x4006_F000	0x4006_FFFF		GPIO
0x4006_7000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		WorkFlash I/F register

Pin status Type	Function Group	Power-on Reset or Low-voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
J	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*2	*3	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Maintain previous state		Hi-Z / Internal input fixed at 0				
	GPIO selected									
K	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Internal input fixed at 0						
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected		Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation(other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency ^{*4}	Value		Unit	Remarks
					Typ ^{*1}	Max ^{*2}		
Power supply current	I _{ccs}	VCC	Sleep operation ^{*5} (main oscillation)	4MHz	2.1	22	mA	^{*3} When all peripheral clocks are ON
					1.3	22	mA	^{*3} When all peripheral clocks are OFF
			Sleep operation (built-in high-speed CR)	4 MHz	1.3	22	mA	^{*3} When all peripheral clocks are ON
					0.8	21	mA	^{*3} When all peripheral clocks are OFF
			Sleep operation (sub oscillation)	32 kHz	0.28	21	mA	^{*3} When all peripheral clocks are ON
					0.27	21	mA	^{*3} When all peripheral clocks are OFF
			Sleep operation (built-in low-speed CR)	100 kHz	0.29	21	mA	^{*3} When all peripheral clocks are ON
					0.28	21	mA	^{*3} When all peripheral clocks are OFF

^{*1}: T_A=+25°C, V_{CC}=3.3 V

^{*2}: T_J=+125°C, V_{CC}=5.5 V

^{*3}: When all ports are fixed.

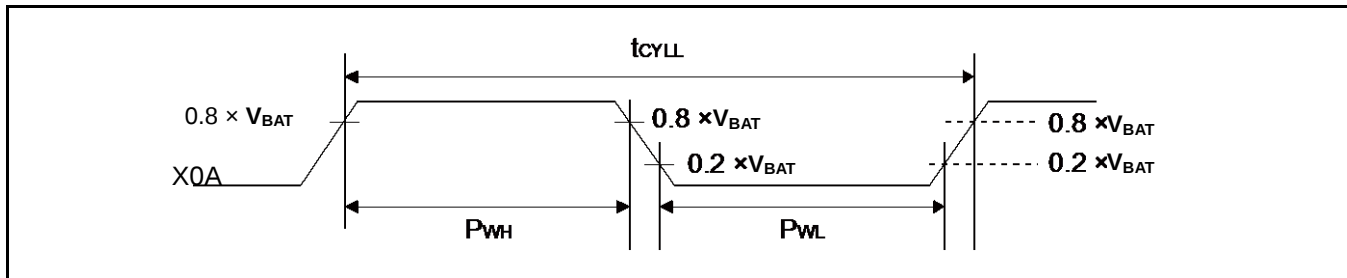
^{*4}: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

^{*5}: When using the crystal oscillator of 4 M Hz (including the current consumption of the oscillation circuit)

12.4.2 Sub Clock Input Characteristics

($V_{BAT} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	μs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL} , P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



12.4.3 Built-in CR Oscillation Characteristics

Built-in High-speed CR

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	$T_J = -20^{\circ}C$ to $+105^{\circ}C$	3.92	4	4.08	MHz	When trimming*1
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	3.88	4	4.12		
Clock frequency	f_{CRH}	$T_J = -40^{\circ}C$ to $+125^{\circ}C$	2.9	4	5		When not trimming
Frequency Stabilization time	t_{CRWT}	-	-	-	30	μs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency/temperature trimming.

*2: This is the time to stabilize the frequency of high-speed CR clock after setting trimming value.

This period is able to use high-speed CR clock as source clock.

Built-in Low-speed CR

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

Separate Bus Access Synchronous SRAM Mode

 (V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Address delay time	t _{AV}	MCLK, MAD[24:0]	V _{CC} ≥ 4.5 V	1	9	ns
			V _{CC} < 4.5 V		12	
MCSX delay time	t _{CSL}	MCLK, MCSX[7:0]	V _{CC} ≥ 4.5 V	1	9	ns
			V _{CC} < 4.5 V		12	
	t _{CSH}		V _{CC} ≥ 4.5 V	1	9	ns
			V _{CC} < 4.5 V		12	
MOEX delay time	t _{REL}	MCLK, MOEX	V _{CC} ≥ 4.5 V	1	9	ns
			V _{CC} < 4.5 V		12	
	t _{REH}		V _{CC} ≥ 4.5 V	1	9	ns
			V _{CC} < 4.5 V		12	
Data set up →MCLK↑ time	t _{DS}	MCLK, MADATA[15:0]	V _{CC} ≥ 4.5 V	19	-	ns
			V _{CC} < 4.5 V	37		
MCLK↑→ Data hold time	t _{DH}	MCLK, MADATA[15:0]	V _{CC} ≥ 4.5 V	0	-	ns
			V _{CC} < 4.5 V			
MWEX delay time	t _{WEL}	MCLK, MWEX	V _{CC} ≥ 4.5 V	1	9	ns
			V _{CC} < 4.5 V		12	
	t _{WEH}		V _{CC} ≥ 4.5 V	1	9	ns
			V _{CC} < 4.5 V		12	
MDQM[1:0] delay time	t _{DQML}	MCLK, MDQM[1:0]	V _{CC} ≥ 4.5 V	1	9	ns
			V _{CC} < 4.5 V		12	
	t _{DQMH}		V _{CC} ≥ 4.5 V	1	9	ns
			V _{CC} < 4.5 V		12	
MCLK↑→ Data output time	t _{ODS}	MCLK, MADATA[15:0]	V _{CC} ≥ 4.5 V	MCLK+1	MCLK+18	ns
			V _{CC} < 4.5 V		MCLK+24	
MCLK↑→ Data hold time	t _{OD}	MCLK, MADATA[15:0]	V _{CC} ≥ 4.5 V	1	18	ns
			V _{CC} < 4.5 V		24	

Note:

- When the external load capacitance C_L = 30 pF

12.4.11 CSIO Timing

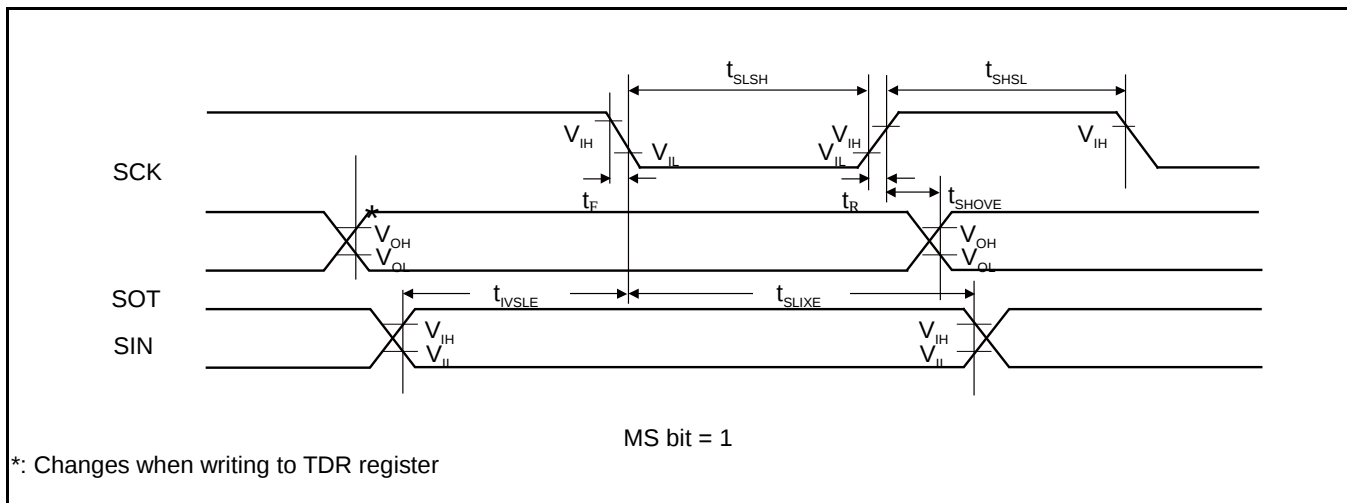
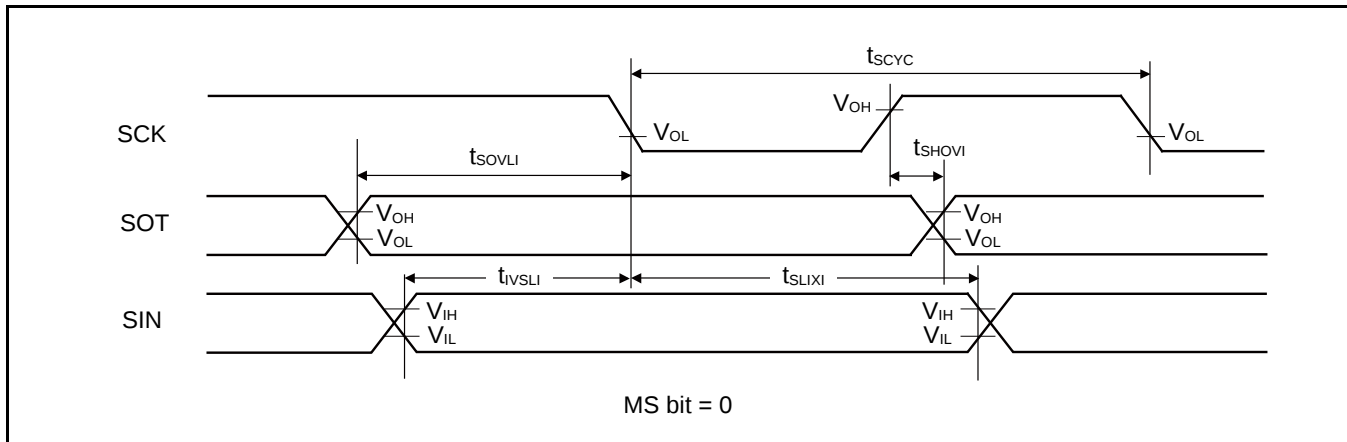
Synchronous Serial (SPI = 0, SCINV = 0)

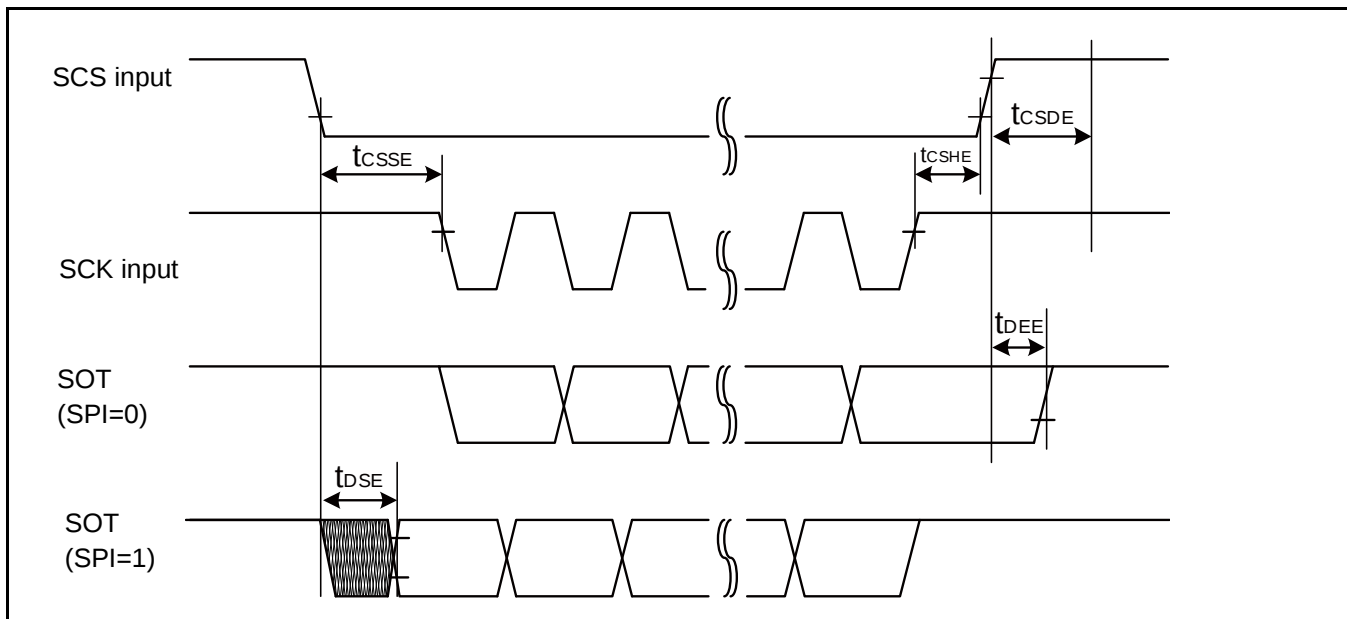
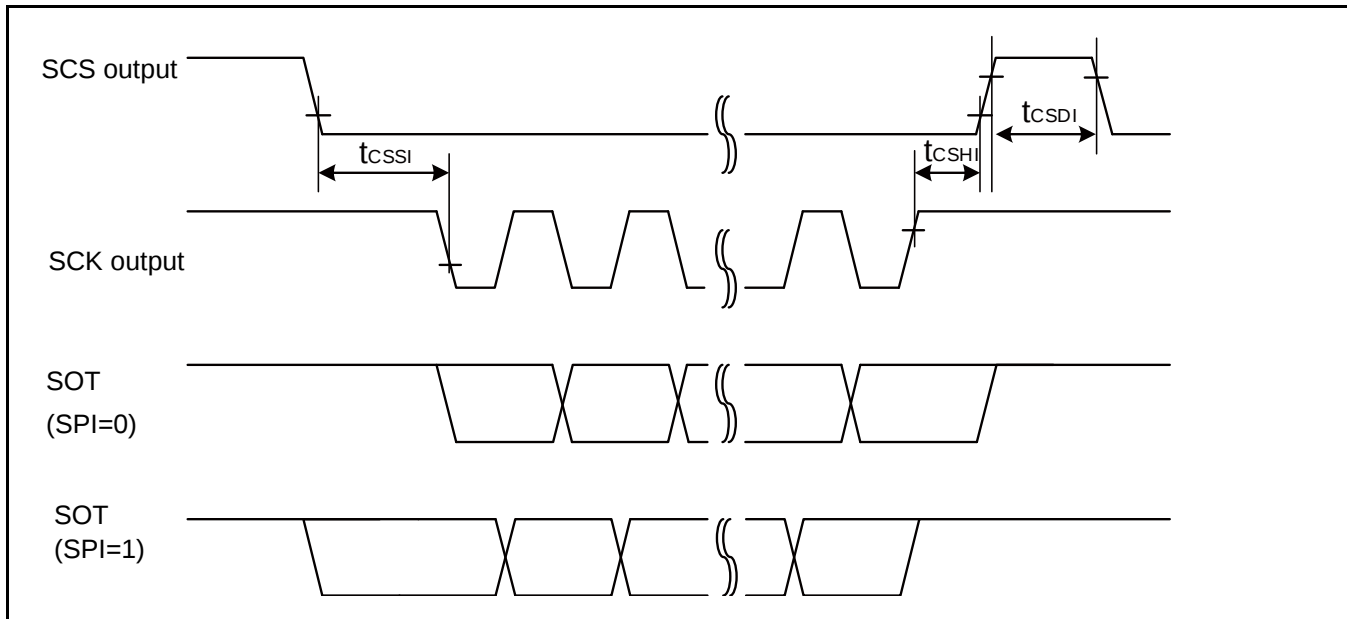
($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK $\downarrow$ →SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK $\uparrow$ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK $\uparrow$ →SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK $\downarrow$ →SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK $\uparrow$ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK $\uparrow$ →SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number.
For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance $C_L = 30 pF$.





13. Ordering Information

Part Number	Package
S6E2H46G0A GV20000	Plastic LQFP (0.5-mm pitch), 120 pin (LQM120)
S6E2H44G0A GV20000	
S6E2H46F0A GV20000	Plastic LQFP (0.5-mm pitch), 100 pin (LQI100)
S6E2H44F0A GV20000	
S6E2H46E0A GV20000	Plastic LQFP (0.5-mm pitch), 80 pin (LQH080)
S6E2H44E0A GV20000	
S6E2H46G0A GB30000	Plastic FBGA (0.5-mm pitch), 121 pin (FDI121)
S6E2H44G0A GB30000	

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